The TURBOchannel Interface ASIC (TcIA)

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Digital's TRI/ADD Program

Overview

- Introduction to the TcIA
- Characteristics
- Some Definitions
- Functions
- Block Diagram
- Registers
- Simple DMA and Scatter/Gather
- Support for 8/16-bit DMA
- Wrap-up

Goals

To give hardware designers a

- **"known-good"**
- **low-cost**
- **small real-estate**
- **high performance**
- **general purpose**

interface to the TURBOchannel to help in the development of new options.

How are the goals achieved?

- Designed and tested by experienced TURBOchannel engineers
- Single plastic quad flat pack
- Single package of 28 mm x 28 mm
- Designed for and tested with 25 MHz TURBOchannel
- Tested with other speed TURBOchannel implementations
- Support for PIO, Simple DMA and Intelligent DMA

What does this do for you?

- Guarantees correct TURBOchannel implementation
- Option designer can focus on option functionality
- Small footprint leaves room for more features on board
- Potential for additional features (e.g. DMA) at equivalent cost to a simple interface to the TURBOchannel (22V10s, transceivers)
- Faster time to market

TcIA Characteristics

Physical

- Plastic Quad Flat Pack
- 160 pins
- 0.65 mm pin pitch
- 28 mm x 28 mm
- CMOS gate array
- Under 3 Watts at full TURBOchannel speed (25Mhz)

TcIA Characteristics

Logical

- Separate "transmit" and "receive" DMA engines
- 20 bit address latch for option-side decoding
- TURBOchannel and option sides may run in separate time domains
  - FIFOs and latches separate the two sides
  - Option side may be significantly slower than the TURBOchannel clock
  - Option side may be faster than the TURBOchannel clock with a maximum of just over 25 MHz.
  - Option side may run at the TURBOchannel clock speed
- Byte packing and unpacking for DMA data

Some important definitions

- A transaction is the movement of data on the TURBOchannel.
- An I/O transaction takes place when the system writes to or reads from an option.
- A DMA transaction takes place when an option writes to or reads from system memory.
- **Transmit** is the movement of data **from** the **system to** the **option**, as to a serial line. Thus a transmit DMA operation uses TURBOchannel DMA read transactions.
- **Receive** is the movement of data **from** the **option to** the **system**, as from a serial line. Thus a receive DMA operation uses TURBOchannel DMA write transactions.
- A word is 32 bits wide.
- A half-word is 16 bits wide.

TcIA Functions

Support for Programmed I/O (only) Devices

Represent a large portion of TURBOchannel option applications

PIO also used by DMA-driven options

- Option may be synchronous or asynchronous with respect to TURBOchannel clock
- Provides 8 read/write general-purpose outputs (bits)
- Provides 4 readable inputs that can be used to generate a TURBOchannel interrupt
- Optional TURBOchannel parity generation and checking
- I/O address latching

TcIA Functions

Support for Simple DMA Devices

Simple DMA defined as: data transfer to or from sequential memory locations with addresses supplied by the TcIA

Represents the majority of TURBOchannel DMA applications

- Word-addressable transmit and receive pointers
- 15-word transmit and receive FIFOs
- Transmit and receive scatter/gather tables (more on this later)
- Byte and half-word data with unpacking and packing of data

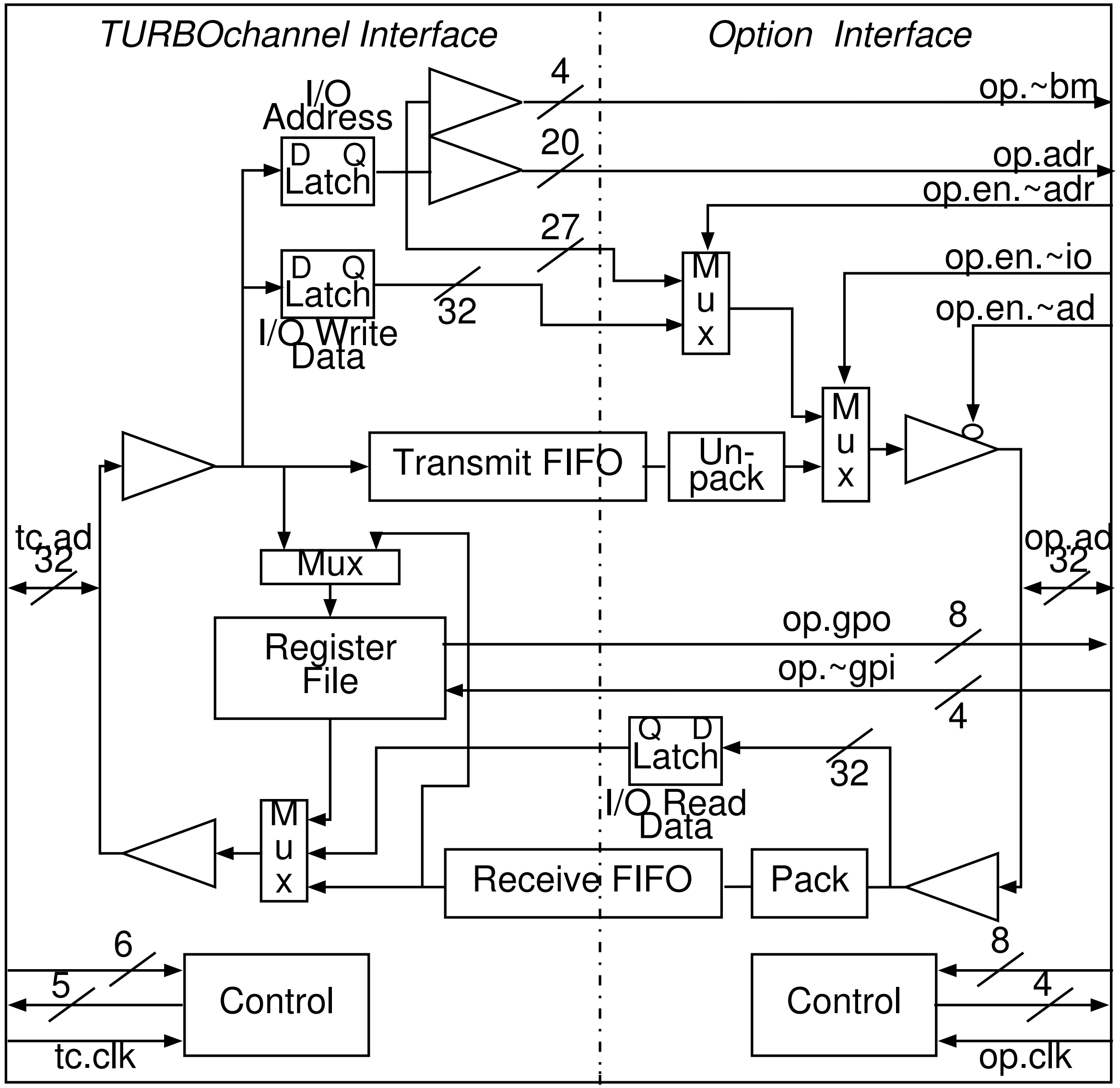
TcIA Functions

Support for Intelligent Controllers

Intelligent DMA defined as: options that execute their own instructions and supply DMA addresses to the TcIA

- External addresses are supplied by the option for DMA reads and writes
- Option addresses may be up to 32 bits
  - Mask register controls width of option-supplied address
  - Remainder of address supplied by system software
- Word count and burst size supplied by the option
- Byte and half-word data with unpacking and packing of data

TcIA Block Diagram



Major Features of TcIA Block Diagram

Register file block

- Control and status registers, including GPO and GPI bits
- DMA "transmit" and "receive" pointers and word counters

Latch blocks

- I/O address
- I/O write data
- I/O read data

Major Features of TcIA Block Diagram

Transmit FIFO and Unpack blocks

- 15 word FIFO
- Byte and half-word data unpacking

Packer and receive FIFO blocks

- Byte and half-word data packing
- 15 word FIFO

MUX blocks (4)

- Data source in 2 from TURBOchannel to option selected by option hardware
- Data source in 1 from option to TURBOchannel and in 1 from TURBOchannel to register file selected by the TcIA

Register list (grouped by function)

All are word-wide and word-access only

Control and Status registers

- OCR1 Option Control Register 1
- OCR2 Option Control Register 2
- OIR Option Interrupt Register
- OIMR Option Interrupt Mask Register

Data access register

- FAR FIFO Access Register

DMA registers

- Transmit DMA group
- Receive DMA group
- DPM Data Pointer Mask

Registers

Control and Status registers

- OCR1 Option Control Register 1 (32 bits used)
  - DMA enables for transmit and receive
  - FIFO enables for transmit and receive
  - Transmit unpacker and receive packer size and byte counters
  - DMA burst controls for transmit
- OCR2 Option Control Register 2 (31 bits used)
  - FIFO counter access for transmit and receive
  - Little-endian/Big-endian control bit
  - Receive FIFO flush counter (timeout) and threshold
  - TURBOchannel slot size (controls address decoding)
  - Receive DMA burst control
  - System page size control
  - "intelligent mode" bits for transmit and receive

Registers

Control and Status registers

- OIR Option Interrupt Register (26 bits used)
  - DMA error status for transmit and receive
  - DMA word count expired status for transmit and receive
  - Parity error status
  - FIFO empty/not-empty status for transmit and receive
  - FIFO counter readouts for transmit and receive
  - General Purpose Inputs readout
- OIMR Option Interrupt Mask Register
  - Each bit of the OIMR is an enable bit for the corresponding bit of the OIR. When set to 1, that OIR bit is enabled to request an interrupt.

Registers

Data Access Register

- FAR FIFO Access Register (32 bits)
  - Read: Reads from head of receive FIFO without changing FIFO counter. If FIFO is empty, reads contents of packer.
  - Write: Writes to tail of transmit FIFO without changing FIFO counter. Can be used to write un-aligned data to the FIFO for non-word-oriented DMA cleanup.

Registers

DMA registers

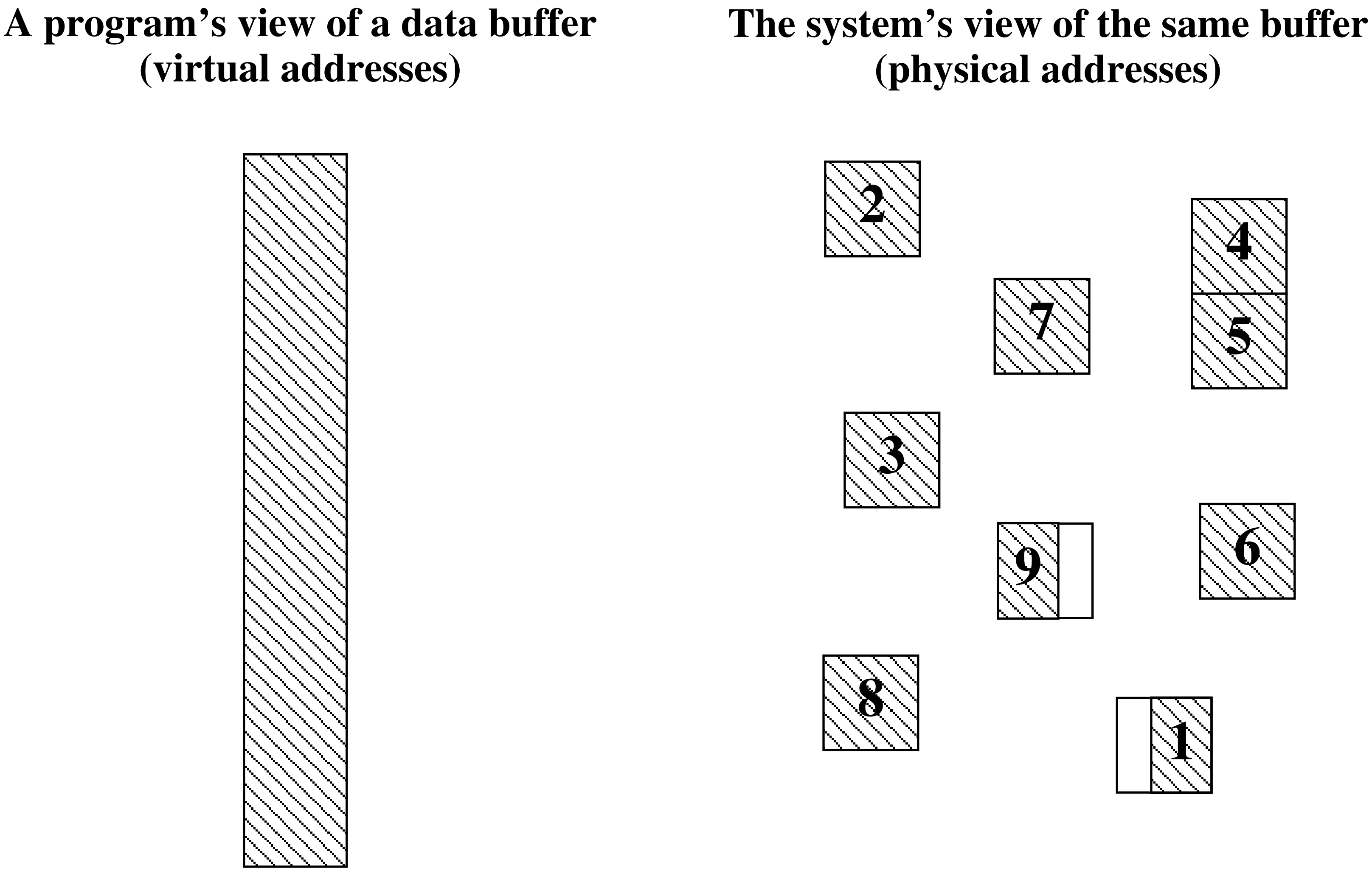
- Transmit DMA group
- Receive DMA group
  - TDP/RDP Transmit/Receive DMA Pointer (Simple and Intelligent DMA)
    . High 32 bits of 34-bit TURBOchannel physical memory address
    . Points to next word for DMA operation
  - TSGP/RSGP Transmit/Receive Scatter/Gather Pointer (Simple DMA)
    . High 32 bits of 34-bit TURBOchannel physical memory address
    . Points to next word in scatter/gather table
  - TWC/RWC Transmit/Receive DMA Word Counter (Simple DMA)
    . 24 bits wide
- DPM Data Pointer Mask
  - Intelligent mode transmit and receive address mask for options that do not supply full 32-bit TURBOchannel physical word addresses

Simple DMA and Scatter/Gather Issues

For Simple DMA operations, software needs to handle

- Sequential DMA memory accesses
- Paged system memory

Simple DMA and Scatter/Gather Issues



Simple DMA and Scatter/Gather Issues

The TcIA resolves these issues for simple DMA operations with its automatic scatter/gather function.

How is Scatter/Gather implemented?

TcIA registers

TDP/RDP Transmit/Receive DMA Pointer

- Points to the next word for the DMA operation
- Loaded from next word of scatter/gather table when page boundary crossed
- Page size determined by OCR2 field

TSGP/RSGP Transmit/Receive Scatter/Gather Pointer

- Points to the next word in scatter/gather table
- Incremented after table entry read (via DMA transaction) from system memory

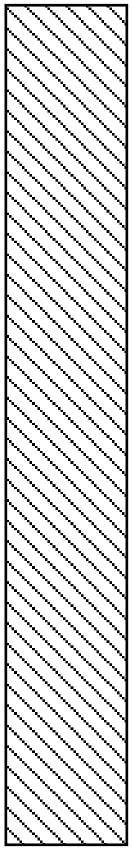
How is Scatter/Gather implemented?

Scatter/Gather table

- An array of words in system memory
- The array MUST be contiguous in physical memory
- One word for each page to be entered during the DMA operation
  NOTE: The first page is NOT included!
- Usually the starting address of the next page of the transfer
- The high 32 bits of a 34-bit TURBOchannel physical address

What Scatter/Gather does for Simple DMA

A program's view of a data buffer (virtual addresses)

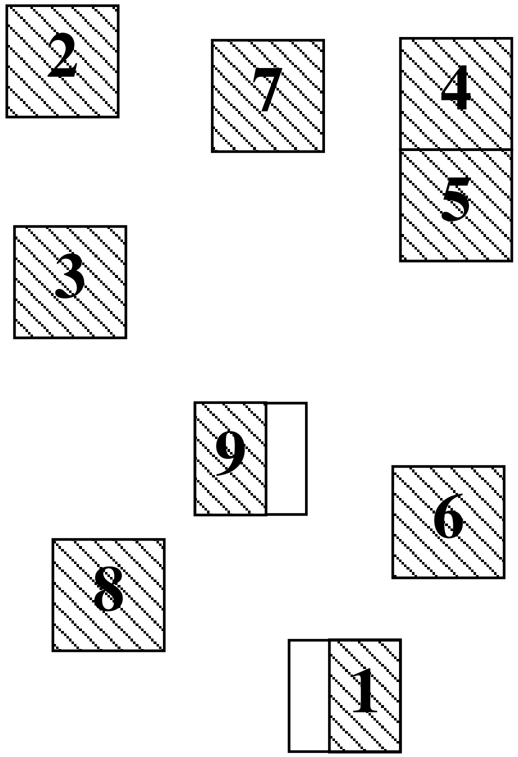


The scatter/gather table

PA(2)
PA(3)
PA(4)
PA(5)
PA(6)
PA(7)
PA(8)
PA(9)

PA = Physical Address

The system's view of the same buffer (physical addresses)



Support for 8/16-bit DMA Data

Features

- Option-side data width controlled by OCR1
- Data width is the same for transmit and receive
- Transmit unpacker and receive packer counters
  - Set by software through OCR1
  - Read by software through OIR
- Data alignment support
  - TcIA directly supports word-aligned start and end
  - Software support required for data-size-aligned start or end
  - No direct support (even with software) for odd-byte aligned word or half-word

DMA Setup for 8/16-bit Data Alignment

Transmit buffer not word-aligned

- Buffer start: Set unpack counter to ignore first bytes or half-word
- Buffer end: Software (or added hardware) must help pass last bytes or half-word

Receive buffer not word-aligned

- Buffer start: Set pack counter position first bytes or half-word; software MUST save and restore bytes/half-word not part of the buffer
- Buffer end: Software must help pass last bytes or half-word

Final Comments

- Only some features and modes have been presented
- TcIA is Pass 2 silicon
- Has been designed into a Test Board
  - All modes tested
  - Tested with multiple TURBOchannel speeds
  - Tested with varying option-side clock
- Fully functional with one design flaw:
  - Simultaneous transmit and receive Simple DMA crossing a page boundary will hang the chip
  - Only work-around is external circuitry
  - Otherwise must be avoided

Availability

Information on the TURBOchannel Interface ASIC is available from:

Integrated Test Solutions
2352 Main Street, Suite 201
Concord Office Park
Concord, MA 01742

Telephone: (508) 897-0028
FAX: (508) 897-0171