CS20 Technical Reference Manual

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Trademarks

Preliminary Product Information

The information in this publication is preliminary, and is believed to be accurate at the time of publication. API makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication or the information contained herein, and reserves the right to make changes at any time, without notice.

Revision History

Date	Rev	Description
Nov 2000	1.0	Initial Release
Jan 2001	1.1	Engineering and product updates.
April 2001	1.11	CE compliance notification and installation requirements added.
May 2001	1SP	TMorris rev.

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European Community Customers

The CS20 is designed for professional use in cluster applications.

CS20 clusters deployed in European Community (EC) countries must be configured with a minimum of four (4) CS20s to meet the requirements of EN61000-3-2.

API NetWorks has certified and labeled the CS20 as European Conforming (CE) compliant based on the minimum four (4) node installation requirement.

CS20 installation procedures also require that the CS20 power supply is connected to a properly grounded, single-phase AC power outlet.

Please email any questions regarding this issue to:

customer.support@api-networks.com

Or, contact your API NetWorks sales representative.

Preface

Overview

This reference manual describes the API NetWork's CS20 system, including the motherboard, the PCI riser, and the chassis for computing systems in a high-density 1U form factor with dual or uni-processor Alpha 21264 microprocessors and the Compaq 21272 core logic chipset.

Note: *For the sake of simplicity in this document, the designation "21264" refers to 21264B processor.*

Audience

This reference manual is intended for system designers and others to evaluate and use computer systems based on the CS20 system.

Scope

This reference manual describes the functional operation, firmware platform, and memory interfaces of the CS20 system. Specific details on industry standards (for example, on PCI or ISA bus specifications) are not included here. However, additional information is available in the appropriate vendor and IEEE specifications. See Appendix A for information on related documentation.

Conventions and Definitions

This section defines product-specific terminology, abbreviations, and other conventions used throughout this manual.

Typographic Conventions

This manual uses the following type conventions:

- Variable information and document titles appear in *italic* type.
- Text that you type is shown in **`bold Courier font`**.
- Type that appears on a screen, such as an example of computer output, is shown in `Courier font`.

- Two key names joined with a forward slash are simultaneous keystrokes. Press down the first key while you type the second key, as in press Ctrl/S.

Signals and Bits

- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by API NetWorks, Inc. for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes to these registers, it must first read the register and change only the non-reserved bits before writing back to the register.

Data

The following list defines data terminology:

- Units
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo—K, as in 4-Kbyte page (2^{10})
  - Mega—M, as in 4 Mbits/sec (2^{20})
  - Giga—G, as in 4 Gbytes of memory space (2^{30})

Acronyms

The following is a list of the acronyms used in this document and their definitions.

Acronym	Definition
BIST	Built-In Self Test
CE	European Conforming
CLI	Command Line Interface
CSR	Control/Status Register
CPU	Central Processing Unit
cUL	Canadian Underwriters Laboratory
DBM	Debug Monitor
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
DQM	Data Input/Output Mask
EIDE	Enhanced Integrated Device Electronics
EMI	Electromagnetic Interference
EPLD	Electrically Programmable Logic Device
ESBGA	Enhanced Super Ball Grid Array
FCC	Federal Communications Commission
FDC	Floppy Disk Controller
FDD	Floppy Disk Drive
FID	Frequency Identification
FIFO	First In, First Out
FPGA	Field Programmable Gate Array
HDD	Hard Disk Drive
I^2C	Inter-integrated Circuit
IDE	Integrated Device Electronics
I/O	Input/Output
ISA	Industry Standard Architecture
ISP	In-system Programmability
LED	Light Emitting Diode
LVD	Low Voltage Differential
LVTTL	Low Voltage Transistor-Transistor Logic
NDA	Non-disclosure Agreement
OEM	Original Equipment Manufacturer
OS	Operating System
PAL	Privileged Architecture Library

Acronym	Definition
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PIO	Programmed Input/Output
PLL	Phase Locked Loop
ROM	Read-only Memory
RTC	Real-time Clock
SCSI	Small Computer System Interface
SDRAM	Synchronous Direct Random Access Memory
SE	Single-ended
SPD	Serial Presence Detect
SROM	Serial Read-only Memory
SRAM	Static Random Access Memory
SRM	System Reference Manual
SSRAM	Synchronous SRAM
TIG	TTL Integrated Glue Logic
UL	Underwriters Laboratory
USB	Universal Serial Bus
VRM	Voltage Regulator Module

Chapter 1 Introduction

The CS20 is a rack-mount, Alpha Processor system designed for optimal performance in a cluster application.

CAUTION: Always take appropriate electrostatic discharge safety measures when handling boards or modules.

1.1 Features

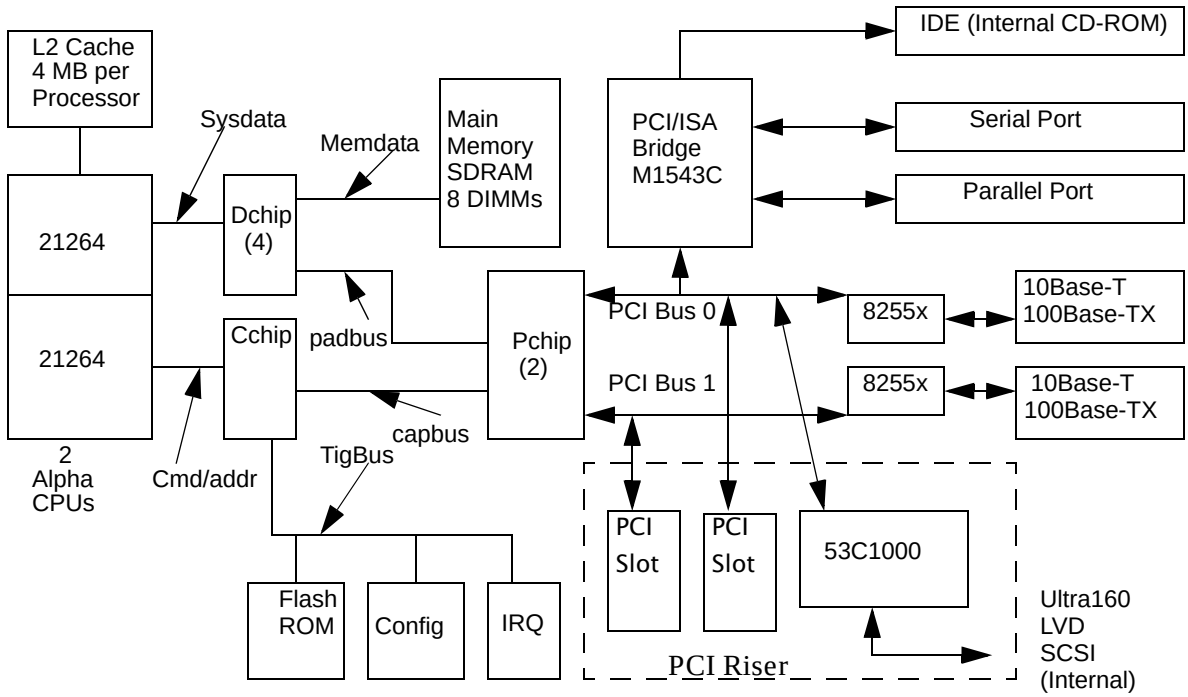

Figure 1-1 CS20 Logical Block Diagram

Table 1-1 summarizes the CS20 product features.

Table 1-1 CS20 Product Features

Feature	Description
Physical Form Factor:	• High-Density (1.75 inch x 17 inches x 20 inches). • Alpha 21264B at speeds of 833 MHz.
Chipset:	21272 (Tsunami)—One Cchip, four Dchips, and two Pchips provide the following: • Maximum 166 MHz system bus with Double Data Rate (DDR) transfers, maximum bandwidth of 2.67 GBytes/second. • One 256-bit memory bus. • Two 64-bit, 33 MHz PCI buses.
Cache:	External L2 cache with 128-bit data path supports: • 4 MB cache per processor, DDR SRAMs.
Main Memory:	• Eight 168-pin Dual Inline Memory Module (DIMM) sockets, up to 2 GB (256 MB per DIMM). • Supports Phase Locked Loop (PLL) or Register-based Synchronous Direct Random Access Memory (SDRAM) Serial Presence Detect (SPD) modules of 64 MB, 128 MB, and 256 MB. • Low-Voltage Transistor/Transistor Logic (LVTTL) compatible memory I/O.
Power:	500W PSU: (+) 12 Vdc and standby (+) 5 Vdc. Supplies all integrated devices and memory, 25W PCI slots, and internal 25W disk drive.
On-board I/O:	• M1543C-B1E PCI/ISA Bridge (PCI Local Bus Specification Revision 2.2 compliant) and Enhanced Integrated Device Electronics (EIDE) controller. • Ultra160 SCSI Controller (Adaptec AIC-7892 on current revision, Symbios 53C1000 on earlier revisions) • Dual 10/100 Fast Ethernet network controllers.
I/O Slots:	• Two 64-bit, 33 MHz PCI Slots, PCI Local Bus Specification Revision 2.1 compliant.
Firmware:	• SROM, Alpha Diagnostics, and SRM.

Table 1-1 CS20 Product Features (Continued)

Feature	Description
System Management (via PCI-ISA Bridge I^2C Controller):	• Monitoring of processor and motherboard voltages. • Processor and system thermal monitors. • Detection of processor and motherboard presence, versions, and asset record. • Detection of system and power-supply status and power-supply inhibiting. • Indication of system error for both hardware- and software-detected problems • Monitoring of system fan speeds.

1.2 System Components

The CS20 system is implemented in industry-standard parts and uses two 21264 central processing units (CPUs)..

1.2.1 Enclosure

- Physical Dimensions. The system enclosure measures 1.75 inches high by 17 inches wide by 20 inches deep.
- Fans. There is a total of 11 fans in the CS20 system: five on the front of the system connected by cables to the system motherboard, and six mounted internally. Two of the six internal fans are cabled onto the PCI riser and cool the PCI card assembly; one fan cabled onto the PCI riser cools the I/O. Three internal fans on the back of the system cool the power supply.
- Bezel. The system has a removable front bezel. See the *CS20 Quick Start Installation Guide*, 51-0062, for information on removing and replacing the bezel.
- Power Supply. The CS20 system is equipped with a 500-Watt AC Power 100-120/200-240VAC 60/50 Hz power supply.
- Disk Carrier. The system includes a custom mounting kit that allows the installation of a one-inch-high SCA SCSI disk drive.

1.2.2 Front View of the System

The front panel of the CS20 system contains five fans with connectors to the motherboard, a Slimline CDROM drive, a hard disk drive bay, and three LEDs.

Note: *See Table 1-2 for information on interpreting the system front LEDs and Table 1-3 for information on interpreting the system rear LEDs..*

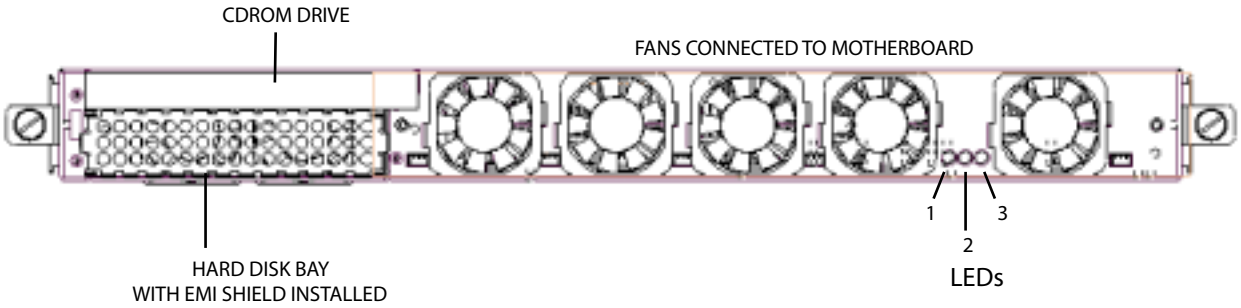

Figure 1-2 Front View of the CS20 System

There are two push-button switches on the motherboard: Halt and Reset. Halt and is accessible through an opening on the front panel of the system. Reset (at J32) is accessible when the system cover is removed.

1.2.3 Rear Panel of the System

The I/O rear panel contains the Dual Ethernet connectors and the parallel and dual serial connectors.

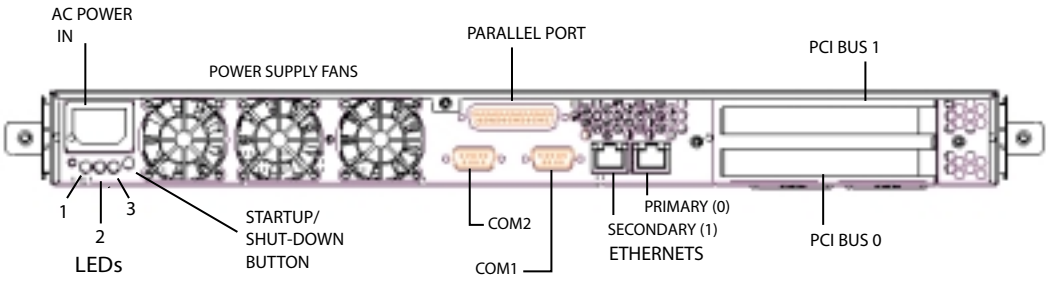

Figure 1-3 Rear View of the CS20 System

The CS20 has front and rear LED status indicators.

Table 1-2 Front LED Status Indicators

LED	Function
1	• Steady Red when system failure needs attention. • Off when the system is functioning properly.
2	Blinks Amber to indicate system activity.
3	• Blinks Green when the system is in Standby mode. • Glows Green to indicate that system power is on.

Table 1-3 Rear LED Status Indicators

LED	Function
1	• Steady Red when a system failure needs attention. • Off when the system is functioning properly.
2	Blinks Amber to indicate system activity.
3	• Blinks Green when the system is in Standby mode. • Glows Green to indicate that system power is on. • Glows Red when the system power has failed.

1.2.4 Memory

The CS20 system motherboard has two 833MHz Alpha 21264 processors. There are 4MB of DDR L2 cache per processor. L2 cache bandwidth is 7.1 GB/s @ 667 MHz and 8.9 GB/s @ 833 MHz.

The CS20 motherboard has eight DIMM sockets arranged in two banks: Bank 0 and Bank 1. Each bank has four sockets and provides a 256-bit wide data path. DIMMs in the same bank must be the same type, size, and speed; DIMMs in different banks may differ in type, size, and speed. Bank 0 must be filled for the CS20 motherboard to work.

Note: *For detailed information on DIMM installation and removal, refer to the CS20 Quick Start Guide, 51-0064.*

1.2.5 Alpha 21264 Processors

The processors are soldered into place on the motherboard. The Alpha processors have a heat sink attached with an integral heat pipe for maximum heat dissipation.

1.2.6 PCI Riser

PCI expansion capabilities include dual independent peer-to-peer 64-bit PCI buses providing a total of 528 MB/s I/O bandwidth. There are two 64-bit 33-MHz PCI slots, each on a separate PCI bus. Internal Ultra160 SCSI and PCI fans are connected to the PCI riser.

The riser also contains

- the Ultra160 controller on bus 0
- a connector for the SCSI cable
- a multi-function environmental monitor
- fan connections for the PCI area

1.2.7 I/O Board

I/O integrated capabilities include two serial ports with modem control, two 10/100 Mb/s Ethernet connectors with integrated LEDs, and one parallel port connector.

Chapter 2 System Memory and Address Mapping

The following sections describe the CS20 system memory and include a list of valid memory configurations. Mapping information for system addresses is also provided.

2.1 Memory Subsystem

The CS20 has eight DIMM sockets arranged in two banks: Bank 0 and Bank 1. Each bank has four sockets and provides a 256-bit wide data path.

The minimum memory size is 256 MB (four 64 MB DIMMs), and the maximum size is 2 GB (eight 256 MB DIMMs). The system clock is 83.3 MHz, yielding a maximum bandwidth of 2.67 GB/sec. System firmware automatically detects memory type and size.

The CS20 supports the following:

- 168-pin, 100 MHz SDRAM, PLL or registered SPD DIMMs
- LVTTL-compatible inputs and outputs
- 3.3V +- 0.3V power supply

Each 168-pin DIMM should have eight Data Input/Output Mask (DQM) signals for each DIMM. Because there is no guarantee of all 32 loadings with DQM from the Cchip, API NetWorks, Inc. uses a 200 psec Quick switch, part number PI3B3244.

Note: *DIMMs installed in one memory bank must be of the same type, size, and speed. DIMMs installed in different memory banks may differ between banks, but not within a bank.*

2.2 Configuring SDRAM Memory

The CS20 supports memory sizes from 256 MB to 2 GB. Table 2-1 lists some of the SDRAM memory configurations available.

Note: *For a list of tested DIMMs, see the Hardware Compatibility List on API's web site at www.api-networks.com.*

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Table 2-1 CS20 SDRAM Memory Configurations

Total Memory	Bank 0	Bank 1
256 MB	64 MB x 4	
512 MB	128 MB x 4	
	64 MB x 4	64 MB x 4
768 MB	128 MB x 4	64 MB x 4
1 GB	256 MB x 4	
	128 MB x 4	128 MB x 4
1.5 GB	256 MB x 4	128 MB x 4
2 GB	256 MB x 4	256 MB x 4

2.3 System Address Mapping

This section describes the mapping of the processor physical address space into memory and I/O space addresses. It includes the translations of the processor-initiated address into a PCI address and PCI-initiated addresses into physical memory addresses.

2.3.1 CPU Address Mapping to PCI Space

The physical system data bus address space is composed of the following:

- Memory address space
- Local I/O space (for registers in the Cchip, Dchips, and Pchips)
- PCI space

The PCI defines four physical address spaces, as follows:

- PCI memory space (for memory residing on the PCI)
- PCI I/O space
- PCI configuration space
- PCI interrupt acknowledge cycles/PCI special cycles

2.3.2 TIGbus Address Mapping

Refer to the *Compaq Functional Specification* for the 21272 core logic chipset for details on the PCI space mapping.

Chapter 3 Electrical and Physical Data

This chapter describes the CS20 power requirements, environmental and enclosure specifications, and physical parameters.

3.1 Power Specifications

3.1.1 Power Connectors

Two power connectors are shown in Figure 3-1. The power connectors are the

- Main Power Connector: One 7 x 2 (14-pin)
- Disk Power Connector: One 4 x 1 (4-pin)

The main power connector provides single 12VDC power and 5V standby power. The main power connector pinout is non-standard. There are several voltage regulators on the motherboard to generate various voltages required by the system.

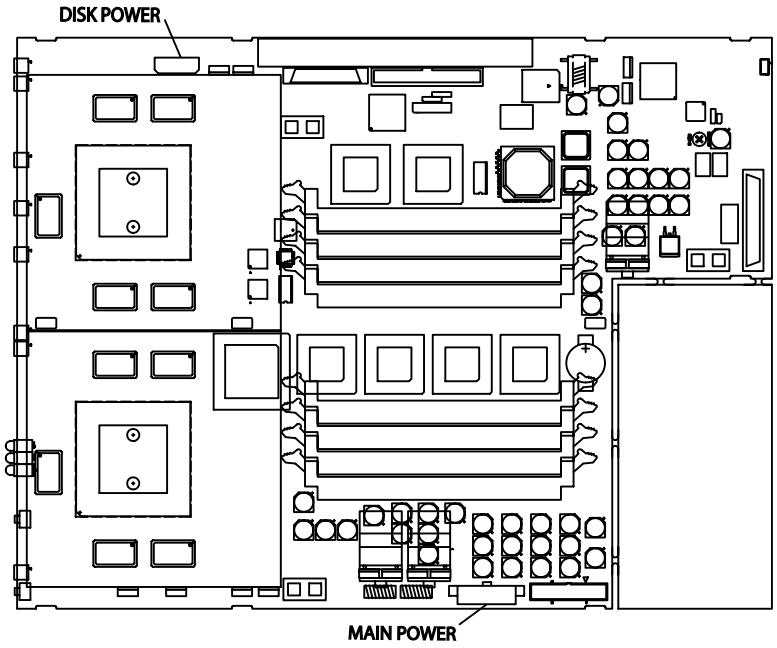

Figure 3-1 CS20 power connectors

3.1.2 Estimated Maximum Power Consumption

The CS20 system estimated maximum total power consumption is 325 W.

3.1.3 Environmental Specifications

The CS20 motherboard and processor are specified to run within the environment listed in Table 3-1.

Table 3-1 Environmental Requirements

Parameter	Specification
Operating Temperature	+5 to +35° C (+41 to +95° F)
Storage Temperature	-35 to +85° C (-31 to +185° F)
Rate of (dry bulb) Temperature Change	11° C/hr. ±2° C/hr. (20° F/hr. ±4° F/hr.)

3.1.4 Safety

The CS20 system meets registered product-safety certification for the U.S. and Canadian Underwriters Laboratories (UL and cUL).

CS20 installation procedures also require that the CS20 power supply is connected to a properly grounded, single-phase AC power outlet.

3.1.5 EMI

Note: *API NetWorks, Inc. recommends the use of high-quality, shielded cables for all external I/O.*

The CS20 meets electro-magnetic interference (EMI) emission certification for the following:

- Federal Communications Commission (FCC) 47 CFR Part 15 Class A (USA)
- EN 55022:1998 / A1:1995 / A2:1997 Class A ITE emissions requirements (EU)
- VCCI Class A ITE (Japan)
- AS / NZS 3548:1995 / Class A ITE (Australia)

- The CS20 is designed for professional use in cluster applications. CS20 clusters deployed in European Community (EC) countries must be configured with a minimum of four (4) CS20s to meet the requirements of EN61000-3-2. API NetWorks has certified and labeled the CS20 as European Conforming (CE) compliant based on the minimum four (4) node installation requirement.

The CS20 also meets the EMI immunity certification *EN 50082-1:1992; EMC Residential, Commercial and Light Industrial Generic Immunity Standard.*

3.1.6 Thermal

The CS20 is designed with a high performance cooling system to maintain internal component temperatures within desired operating ranges. Proper operation of the cooling system requires the front of the CS20 receives an adequate supply of air. If the CS20 is installed behind a grill or other obstruction, it should be no more restrictive than the CS20 bezel: approximately 50% open with no shadows.

3.2 Physical Parameters

3.2.1 Chassis

Table 3-2 CS20 Chassis Physical Parameters

Dimension	Value
Length	20 in.
Width	17 in.
Height	1U

3.2.2 I/O

The rear-panel connectors are integral to the CS20 chassis. The CS20 uses a custom I/O board to provide connections for two serial ports, one parallel port, and two Ethernet RJ45 ports.

The CS20 external rear-panel connectors are shown in the following figure.

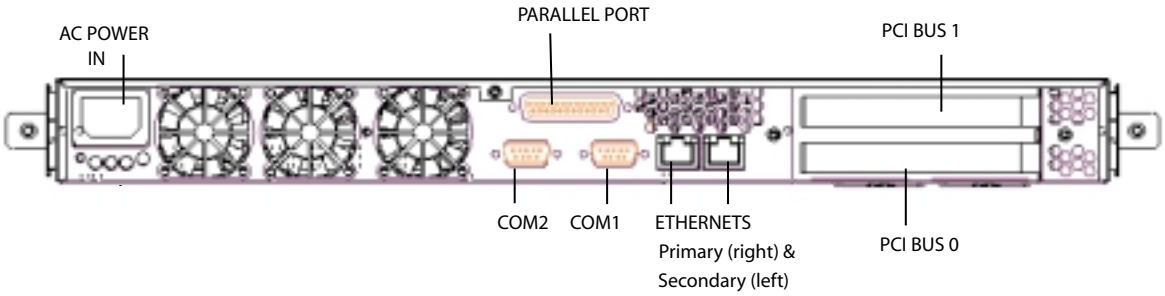

Figure 3-2 Rear Panel Connectors

Chapter 4 System Configuration

This chapter describes the layout and configuration of the CS20 components.

4.1 System Layout and Components

CS20 system on-board connectors are listed in Table 4-1.

Table 4-1 CS20 Components and Connectors

Feature	Description
Memory Modules	256MB to 2GB RAM with ECC Up to 8 168-Pin PC100 SDRAM PLL Registered/Buffered-Based SPD DIMMs
PCI Riser	• Two 64-Bit 33MHz PCI Slots • Ultra160 SCSI
Rear-Panel I/O	Two Serial Ports With Modem Control Parallel Port Dual 10/100 Ethernet
IDE	ATA /66 EIDE
System Power	500-Watt AC Power 100-120 / 200-240 VAC, 60 / 50 Hz

4.1.1 Configuration Requirements

The CS20 automatically configures the L2 cache size and the clock frequencies for the 21272 chipset and the 21264 CPU.

Jumper block J2 makes use of manually inserted two-pin shunts to configure the

CS20 for upgrade or error-recovery functions.

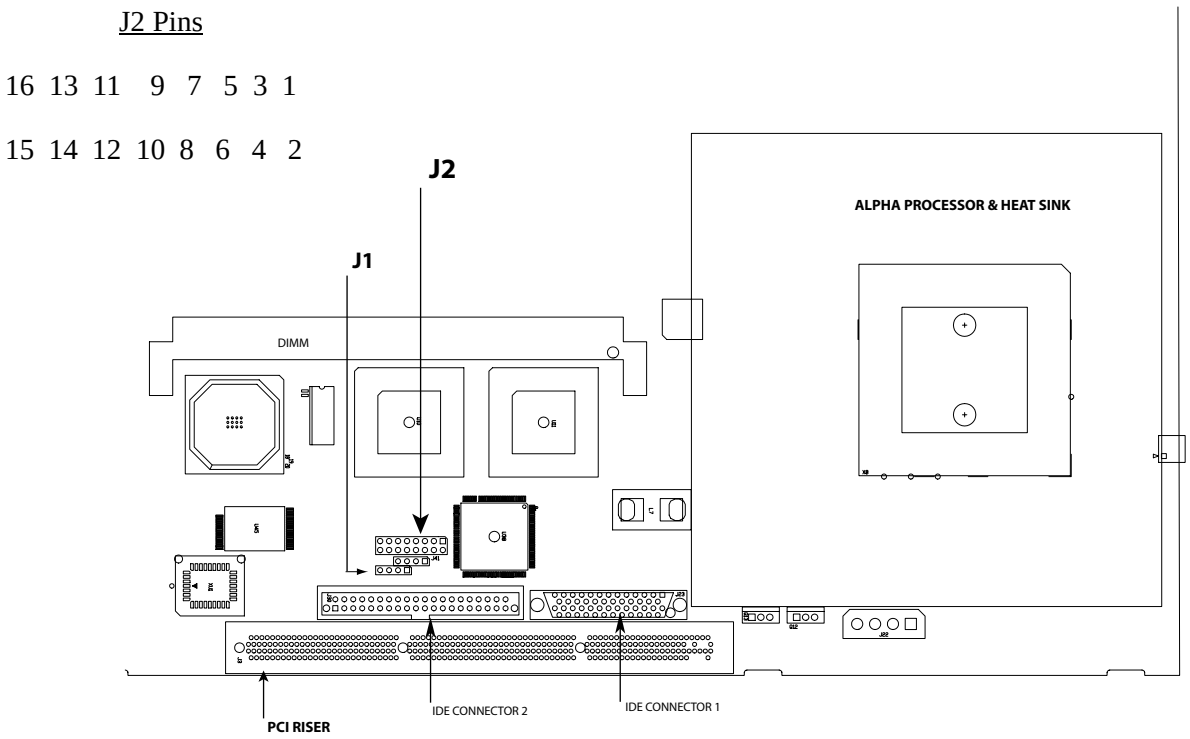

Figure 4-1 J2 Firmware Configuration Jumper Block

- J1 allows manual disabling of either or both processors on the CS20 system. J1 shunts are factory installed and are not user configurable.
- J2 pins 13-14 are the auxiliary I2C bus connector. The auxiliary I2C bus connector on the CS20 motherboard is not used in the CS20 system; it is reserved for factory or FRU testing.
- J2 pins 15-16 are factory set and are not user configurable.
- J2 pins 11-12, 9-10, and 7-8 are reserved.

See Table 4-2 for J2 pin functions.

Table 4-2 J2 Pin Functions

Function	Install Jumper on Pins		
	5/6	**3/4**	**1/2**
Normal operations; execute firmware and boot to operating system using current or default environment settings.	0	0	0
Restore factory default environment settings.	0	0	1
Upgrade or recover firmware (COM1).	0	1	0
Failsafe reflash from CDROM (COM1).	0	1	1
Field installation and test mode.	1	*****	*

Note: 0 = No jumper installed; 1= Jumper installed
****** incicates reserved pins*

There are other pin headers that are unused in the CS20 system. They are provided for factory testing only:

- J7 EPLD power override switch. A shunt is factory installed on pins 2-3 of J7 and is not user configurable.
- J13 EPLD programming port

See Figure 4-2.

4.1.2 Memory Configuration

The memory subsystem consists of two DIMM banks, designated Bank 0 and Bank 1. Each bank has four slots (sockets) that accept 168-pin, PC100 SDRAM PLL Register-based SPD DIMM modules. See Figure 4-2 for slot locations.

Use the following rules for installing memory in the CS20:

- Populate Bank 0 first.
- A bank must be fully populated (all four slots in a bank must be utilized).
- A bank must contain the same type, size, and speed DIMMs.
- Bank 0 and Bank 1 can have different type, size, and speed DIMMs.
- Memory size can range from 256 MB (minimum) to 2 GB (maximum).

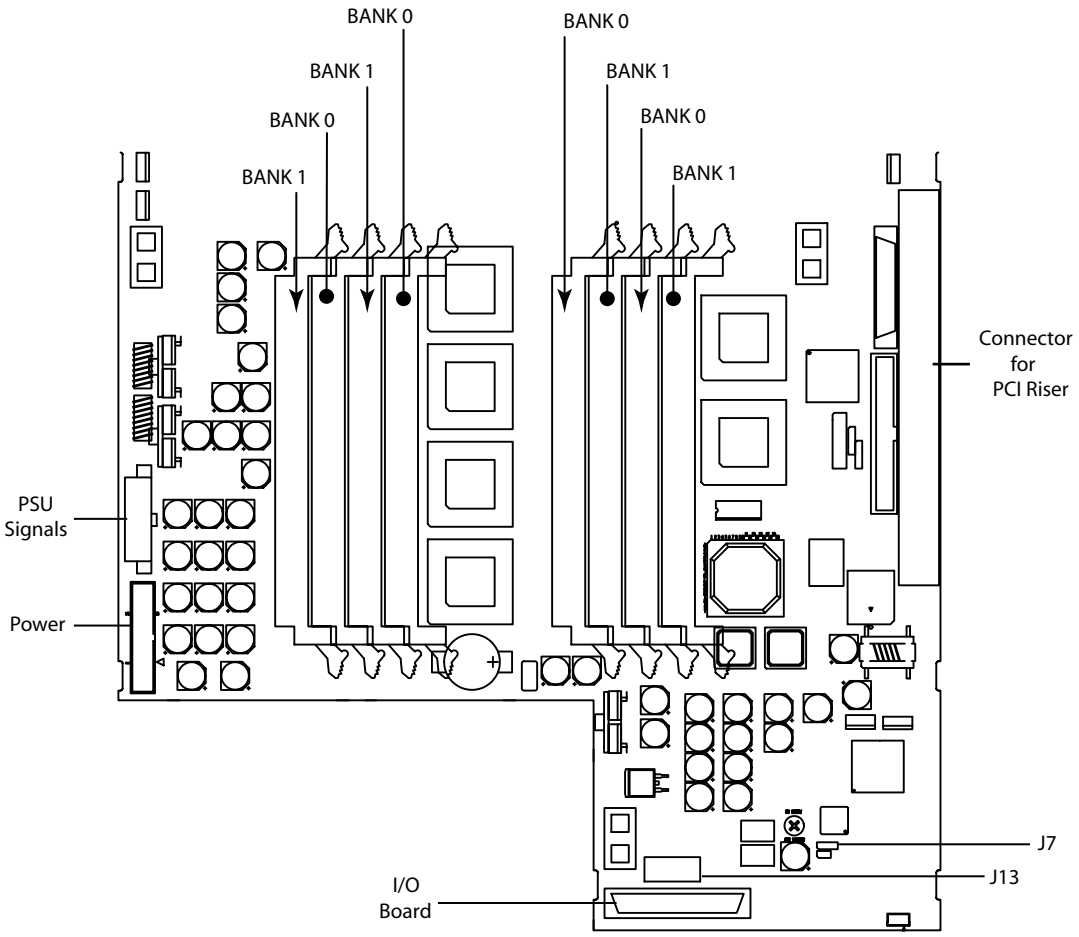

Figure 4-2 Memory subsystem

4.1.3 PCI Riser

The PCI riser includes dual independent peer-to-peer 64-bit PCI buses, 528MB/s total I/O bandwidth, and two 64-bit 33MHz PCI slots. The SCSI Ultra160 sits on the PCI riser.

4.1.4 Rear-Panel I/O

The CS20 system rear I/O includes serial and parallel connections including: Dual Ethernet 10/100; 10-Base T and 100-Base T.

Appendix A

Documentation

A.1 Customer Support

API NetWorks, Inc. provides online product assistance at:

`www.api-networks.com`.

Alpha Original Equipment Manufacturers (OEMs) provide the following online resources for customer support:

URL	Description
`www.compaq.com`	Contains links for the 21272 chipset.
`www.samsungsemi.com`	Contains links for the 21264 CPU.

A.2 Supporting Products

For components and accessories not included with the CS20 system, API NetWorks, Inc. maintains an online Hardware Compatibility List at:

`www.api-networks.com`

Compatibility for items such as memory, power supplies, and enclosure are listed. Our site also includes a Product Information list for peripherals.

A.3 Alpha Products

API NetWorks, Inc. provides up-to-date information about other Alpha products at:

`www.api-networks.com`

A.4 Documentation

A.4.1 Alpha Documentation

Title	Vendor
Alpha Architecture Reference Manual, Third Edition	Compaq Computer Corporation, Digital Press order# EQ-W938E-DP
Alpha Architecture Handbook, Version 4	Compaq Computer Corporation Digital Press order# EC-QD2KC-TE
AlphaPC 264DP Technical Reference Manual	Compaq Computer Corporation, Digital Press order# EC-RBODA-TE

A.4.2 Third-Party Documentation

You can order the following associated documentation directly from the vendor:

Title	Vendor
• ***PCI Local Bus Specification, Revision 2.1*** • ***PCI Multimedia Design Guide, Revision 1.0*** • ***PCI System Design Guide*** • ***PCI-to-PCI Bridge Architecture Specification, Revision 0*** • ***PCI BIOS Specification, Revision 2.1***	PCI Special Interest Group U.S. 1-800-433-5177 International1-503-797-4207 FAX 1-503-234-6762
Computer Architecture	John L. Hennessy and David A. Patterson, Morgan Kaufman Publishers, San Mateo, CA, 1990

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