AlphaPC 264DP

Technical Reference Manual

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Preface

Overview

This manual describes the COMPAQ AlphaPC 264DP, including the mainboard and the daughtercard, for computing systems based on COMPAQ's Alpha 21264 microprocessor and the COMPAQ 21272 core logic chipset.

Audience

This manual is intended for system designers and others who use the AlphaPC 264DP to design or evaluate computer systems based on the Alpha 21264 microprocessor and the 21272 core logic chipset.

Scope

This manual describes the features, configuration, functional operation, and interfaces of the AlphaPC 264DP. This manual does not include specific bus specifications (for example, PCI or ISA buses). Additional information is available in the AlphaPC 264DP schematics, program source files, and the appropriate vendor and IEEE specifications. See Appendix A for information on how to order related documentation and obtain additional technical support.

Manual Organization

This manual includes the following chapters, an appendix, and an index.

- Chapter 1, AlphaPC 264DP Introduction, is an overview of the AlphaPC 264DP, including its components, features, and uses.
- Chapter 2, System Configuration and Connectors, describes the user-environment configuration, board connectors and functions, and switch functions. It also identifies switch settings and connector locations.
- Chapter 3, Power and Environmental Requirements, describes the AlphaPC 264DP power and environmental requirements and provides board dimensions.
- Chapter 4, Functional Description, provides a functional description of the AlphaPC 264DP mainboard, including the 21272 core logic chipset, L2 backup cache (Bcache) and memory subsystems, system interrupts, clock and power subsystems, and peripheral component interconnect (PCI) and Industry Standard Architecture (ISA) devices.
- Chapter 5, System Memory and Address Mapping, describes how to upgrade the AlphaPC 264DP mainboard's SDRAM memory.
- Appendix A, Support, Products, and Documentation, lists sources for components and accessories not included with the AlphaPC 264DP, describes how to obtain COMPAQ information and technical support, and how to order COMPAQ products and associated literature.

Conventions

This section defines product-specific terminology, abbreviations, and other conventions used throughout this manual.

Abbreviations

- Register Access

  The following list describes the register bit and field abbreviations:

Bit/Field Abbreviation	Description
RO (read only)	Bits and fields specified as RO can be read but not written.
RW (read/write)	Bits and fields specified as RW can be read and written.
WO (write only)	Bits and fields specified as WO can be written but not read.

- Binary Multiples

  The abbreviations K, M, and G (kilo, mega, and giga) represent binary multiples and have the following values:

K	=	2^{10} (1024)
M	=	2^{20} (1,048,576)
G	=	2^{30} (1,073,741,824)

  For example:

2KB	=	2 kilobytes	=	2×2^{10} bytes
4MB	=	4 megabytes	=	4×2^{20} bytes
8GB	=	8 gigabytes	=	8×2^{30} bytes

Addresses

Unless otherwise noted, all addresses and offsets are hexadecimal.

Bit Notation

Multiple-bit fields can include contiguous and noncontiguous bits contained in brackets ([]). Multiple contiguous bits are indicated by a pair of numbers separated by a colon (:). For example, [9:7,5,2:0] specifies bits 9,8,7,5,2,1, and 0. Similarly, single bits are frequently indicated with brackets. For example, [27] specifies bit 27.

Caution

Cautions indicate potential damage to equipment, software, or data.

Data Field Size

The term INT*nn*, where *nn* is one of 2, 4, 8, 16, 32, or 64, refers to a data field of *nn* contiguous NATURALLY ALIGNED bytes. For example, INT4 refers to a NATURALLY ALIGNED longword.

Data Units

The following data-unit terminology is used throughout this manual.

Term	Words	Bytes	Bits	Other
Byte	½	1	8	—
Word	1	2	16	—
Longword/Dword	2	4	32	Longword

Term	Words	Bytes	Bits	Other
Quadword	4	8	64	2 Longwords
Octaword	8	16	128	2 Quadwords
Hexword	16	32	256	2 Octawords

Note

Notes emphasize particularly important information.

Numbering

All numbers are decimal or hexadecimal unless otherwise indicated. The prefix 0x indicates a hexadecimal number. For example, 19 is decimal, but 0x19 and 0x19A are hexadecimal (also see Addresses). Otherwise, the base is indicated by a subscript; for example, 100_2 is a binary number.

Ranges and Extents

Ranges are specified by a pair of numbers separated by two periods (..) and are inclusive. For example, a range of integers 0..4 includes the integers 0, 1, 2, 3, and 4.

Extents are specified by a pair of numbers in brackets ([]) separated by a colon (:) and are inclusive. Bit fields are often specified as extents. For example, bits [7:3] specifies bits 7, 6, 5, 4, and 3.

Register and Memory Figures

Register figures have bit and field position numbering starting at the right (low order) and increasing to the left (high order).

Memory figures have addresses starting at the top and increasing toward the bottom.

Signal Names

All signal names are printed in boldface type. Signal names that originate in an industry-standard specification, such as PCI or IDE, are printed in the case as found in the specification (usually uppercase). Active-high signals are indicated by the **_h** suffix. Active-low signals have the **_l** suffix, a pound sign "#" appended, or a "not" overscore bar. Signals with no suffix are considered high-asserted signals. For example, signals **data_h[127:0]** and **cia_int** are active-high signals. Signals **mem_ack_l**, **FRAME#**, and **RESET** are active-low signals.

UNPREDICTABLE and UNDEFINED

Throughout this manual the terms UNPREDICTABLE and UNDEFINED are used. Their meanings are quite different and must be carefully distinguished.

In particular, only privileged software (that is, software running in kernel mode) can trigger UNDEFINED operations. Unprivileged software cannot trigger UNDEFINED operations. However, either privileged or unprivileged software can trigger UNPREDICTABLE results or occurrences.

UNPREDICTABLE results or occurrences do not disrupt the basic operation of the processor. The processor continues to execute instructions in its normal manner. In contrast, UNDEFINED operations can halt the processor or cause it to lose information.

The terms UNPREDICTABLE and UNDEFINED can be further described as follows:

- UNPREDICTABLE
  - Results or occurrences specified as UNPREDICTABLE might vary from moment to moment, implementation to implementation, and instruction to instruction within implementations. Software can never depend on results specified as UNPREDICTABLE.
  - An UNPREDICTABLE result might acquire an arbitrary value that is subject to a few constraints. Such a result might be an arbitrary function of the input operands or of any state information that is accessible to the process in its current access mode. UNPREDICTABLE results may be unchanged from their previous values.

    Operations that produce UNPREDICTABLE results might also produce exceptions.

- An occurrence specified as UNPREDICTABLE may or may not happen based on an arbitrary choice function. The choice function is subject to the same constraints as are UNPREDICTABLE results and must not constitute a security hole.

  Specifically, UNPREDICTABLE results must not depend upon, or be a function of, the contents of memory locations or registers that are inaccessible to the current process in the current access mode.

  Also, operations that might produce UNPREDICTABLE results must not write or modify the contents of memory locations or registers to which the current process in the current access mode does not have access. They must also not halt or hang the system or any of its components.

  For example, a security hole would exist if some UNPREDICTABLE result depended on the value of a register in another process, on the contents of processor temporary registers left behind by some previously running process, or on a sequence of actions of different processes.

- UNDEFINED
  - Operations specified as UNDEFINED can vary from moment to moment, implementation to implementation, and instruction to instruction within implementations. The operation can vary in effect from nothing, to stopping system operation.
  - UNDEFINED operations can halt the processor or cause it to lose information. However, UNDEFINED operations must not cause the processor to hang, that is, reach an unhalted state from which there is no transition to a normal state in which the machine executes instructions. Only privileged software (that is, software running in kernel mode) can trigger UNDEFINED operations.

1 AlphaPC 264DP Introduction

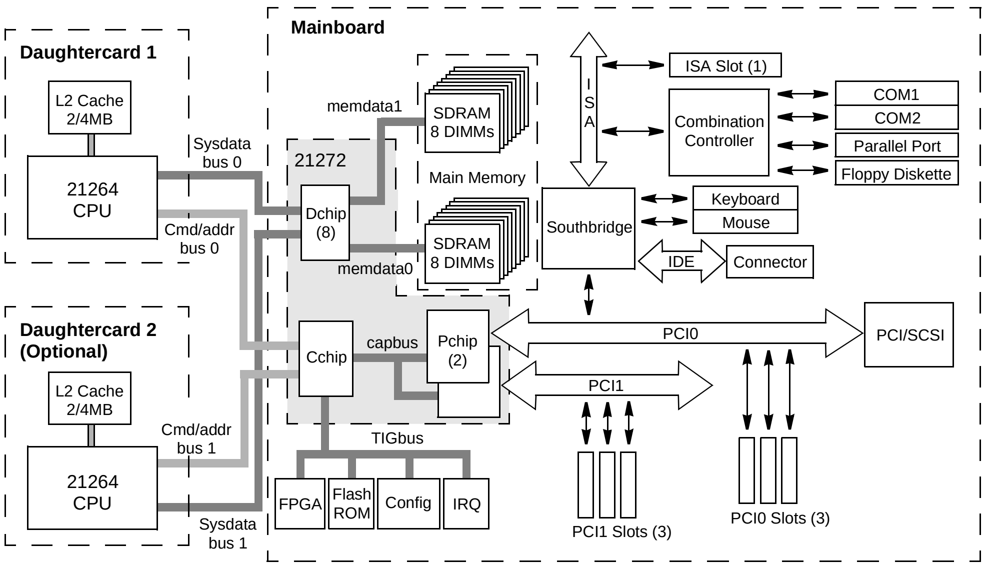
This chapter provides an overview of the AlphaPC 264DP system, including its components, features, and uses.

The AlphaPC 264DP system consists of an AlphaPC 264DP mainboard (mainboard) and one or two AlphaPC 264DP daughtercards (daughtercards). The daughtercard consists of the 21264 microprocessor, L2 cache, reset field programmable gate array (reset FPGA), and power converters for 2.2 volts and 1.5 volts.

1.1 System Components and Features

The AlphaPC 264DP is implemented in industry-standard parts and uses one or two 21264 CPUs running at 500 MHz. The functional components are shown in Figure 1–1 and introduced in the following subsections.

Figure 1–1 AlphaPC 264DP Functional Block Diagram



1.1.1 Memory Subsystem

The DRAM memory subsystem on the AlphaPC 264DP consists of sixteen 200-pin buffered DIMM slots, which are organized as four arrays of memory. The 21272 core logic chipset (21272) supports two 256-bit memory buses (288-bit including ECC) with two arrays on each bus.

The 72-bit, 100-MHz DIMMs consist of 64 bits of data and 8 bits of ECC, and can be 32MB, 64MB, 128MB, or 256MB. The minimum configuration (one array populated with four 32MB DIMMs) is 128MB. The maximum configuation (four arrays each populated with four 256MB DIMMs) is 4GB.

The memory cycle time is 83 MHz, identical to the 21272 cycle time.

Note: Although the memory cycle time is 83 MHz, qualified 100-MHz DIMMs are required.

1.1.2 21272 Core Logic Chipset

The 21264 is supported by the 21272, with a 256-bit memory interface. The 21272 consists of the following three chips:

- The Cchip provides the interface from the CPU and main memory, and includes a general-purpose interface for the flash ROM and interrupts (TIGbus Interface). One Cchip is used per system.
- The Dchip provides the data path from the CPU to memory and I/O. Two, four, or eight Dchips can be used in a system configuration. Eight Dchips provide two 256-bit memory bus interfaces on the AlphaPC 264DP.
- The Pchip provides an interface to the peripheral component interconnect (PCI). One or two Pchips can be used in a system configuration. Two Pchips can be used to provide two independent 64-bit PCI buses. AlphaPC 264DP uses two Pchips to support two 64-bit PCI buses running at 33 MHz.

The chipset includes the majority of functions required to develop a high-performance PC or workstation, requiring minimum discrete logic on the module. It provides flexible and generic functions to allow its use in a wide range of systems.

1.1.3 CPU Daughtercard

The 21264 microprocessor and level 2 cache reside on a separate daughtercard that plugs into the mainboard. One or two daughtercards can be used in an AlphaPC 264DP system. The daughtercard is a 10-layer printed-circuit board with dimensions of approximately 14.99 cm × 30.48 cm (5.905 in × 12.0 in). The daughtercard consists of the following:

- 21264 CPU
- Synchronous level 2 cache (2MB or 4MB cache, using late-write cache SSRAMs)
- A linear regulator, providing 3.3 volts to 1.5 volts conversion for SSRAMs
- dc-to-dc converter for 5 volts to 2.2 volts for 21264 core power
- Reset and configuration FPGA
- Presence detect for cache configuration and CPU speed
- 512KB flash ROM used as SROM
- SROM test port
- 270-pin interface to mainboard (system clock forwarding interface and miscellaneous signals)

1.1.3.1 Level 2 Cache Subsystem Overview

The external level 2 (L2) cache subsystem on the daughtercard supports 2MB or 4MB cache sizes using a 128-bit data bus.

The AlphaPC 264DP supports L2 cache using the synchronous SRAM (SSRAM) sizes shown in Table 1–1. Nine SSRAMs are required per daughtercard for 4MB L2 cache and five SSRAMs are required per daughtercard for 2MB L2 cache. In a dual-processor system, cache sizes must be the same across the two daughtercards. The first implementation of the daughtercard uses late-write SSRAMs.

Table 1–1 L2 Cache Size

L2 Cache Size	SRAM Type
2MB	Four 128KB × 36 data SSRAMs and one 128KB × 36 tag SSRAM
4MB	Eight 256KB × 18 data SSRAMs and one 128KB × 36 tag SSRAM

1.1.3.2 21264 DC-to-DC Converter

The dc-to-dc converter is a 3.0 × 2.2 × 1.4-inch module that is mounted on the daughtercard. It delivers 2.2 volts to the 21264. The features include:

- Programmable voltage between 1.5 volts and 2.5 volts
- Remote sense
- Overvoltage protection
- Current limit and short circuit protection
- Thermal shutdown

1.1.4 Clock Subsystem

The clock subsystem provides clocks to the CPU, 21272, SDRAM DIMMs, and PCI devices. A PC clock generator provides clocks for the SCSI, ISA, and combination chip functions.

1.1.5 PCI Interface

The PCI interface provides a PCI speed of 33 MHz. The Cypress CY82C693UB (southbridge) provides the following:

- PCI-to-ISA bridge
- PCI to IDE interface
- Real-time clock support
- Mouse and keyboard controller

The PCI to SCSI interface is derived from the Adaptec AIC7895 controller (AIC7895). The AIC7895 supports two separated ultrawide SCSI ports.

The PCI has five dedicated 64-bit slots and one shared 64-bit slot. The one shared slot also provides a 16-bit ISA expansion slot. Six expansion slots in total are supported—six PCI, or five PCI and one ISA.

The two PCI buses are configured as follows:

- PCI bus 0: contains Pchip0, southbridge, Adaptec SCSI, and three 64-bit expansion slots
- PCI bus 1: contains Pchip1 and three 64-bit expansion slots

1.1.6 ISA Interface

The ISA bus provides an expansion bus and the following system support functions:

- The ISA bus has one shared expansion slot with the PCI.
- An SMC FDC37C669 super I/O controller chip is used as the combination controller chip that provides a diskette controller, two universal, asynchronous receiver/transmitters (UARTs) for com ports, and a parallel port.

1.1.7 IDE Interface

The integrated drive electronics (IDE) provides an additional expansion bus, with one connector on the mainboard.

Note: Only CD-ROMs with an IDE cable length of 12 inches or less are supported.

2

System Configuration and Connectors

2.1 Board Layouts and Components

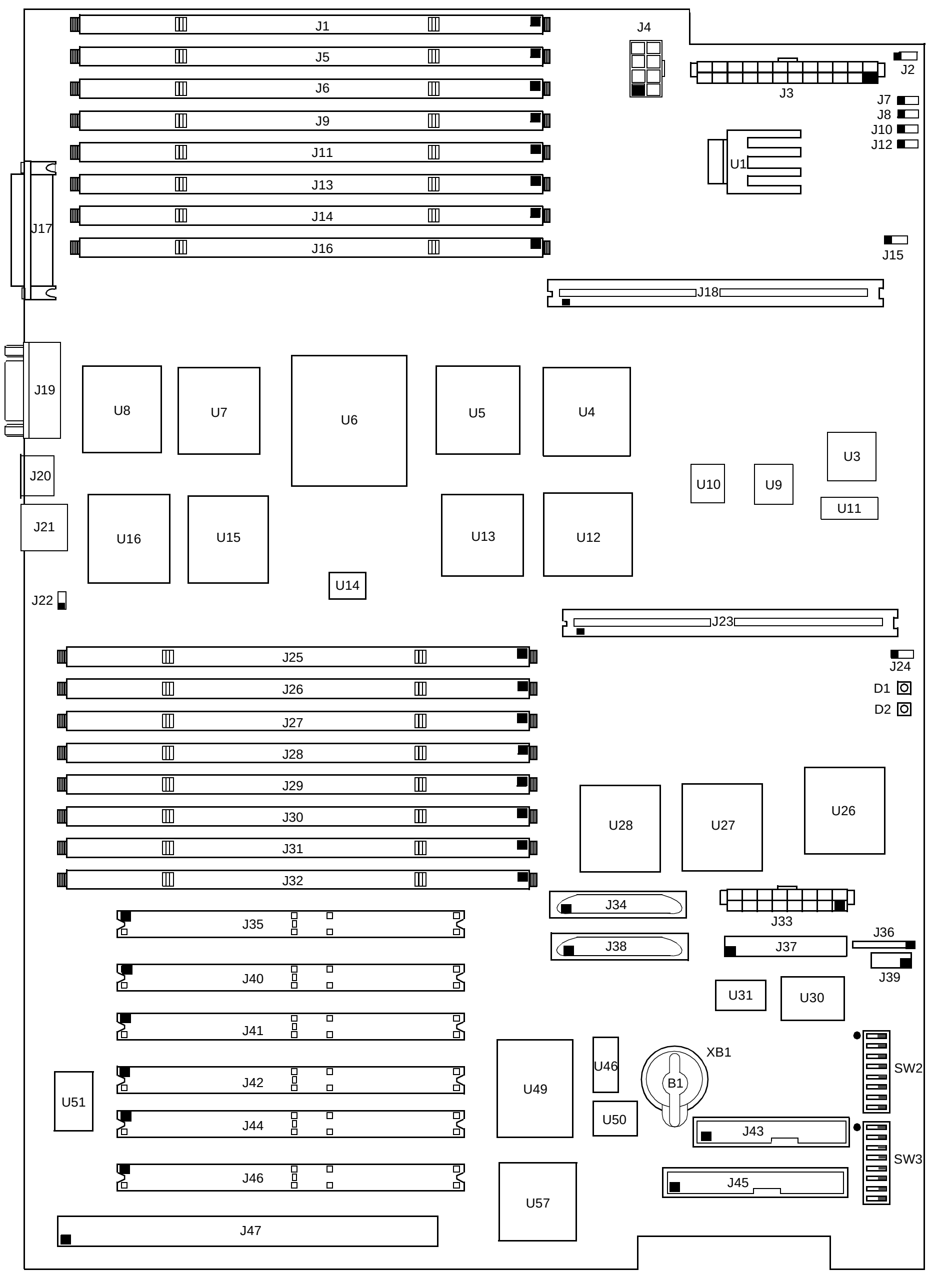
The AlphaPC 264DP uses switches to implement variations in clock frequency (21272 and 21264) and L2 cache configuration. Note that the switches for the 21264 speed and L2 cache configuration are on the daughtercard. The switches for the 21272 speed are on the mainboard. These switches must be configured for the user's environment. Onboard connectors are provided for the I/O, memory DIMMs, serial and parallel peripherals, and IDE devices.

After the board is configured, you can apply power and start up the firmware that is loaded in the flash ROM.

Figure 2–1 shows the AlphaPC 264DP mainboard and its components.

Board Layouts and Components

Figure 2–1 AlphaPC 264DP Mainboard Switch/Connector/Component Location



■ indicates pin 1. ● indicates switch 1.

Board Layouts and Components

Table 2–1 describes AlphaPC 264DP mainboard components.

Table 2–1 AlphaPC 264DP Mainboard Switch/Connector/Component List

Item No.	Description	Item No.	Description
XB1	RTC battery (CR2032)	J45	IDE bus connector
J1, J5, J6, J9 J11, J13, J14, J16, J25-J32	Memory connectors	J47	ISA bus connector
J2, J15, J22, J24	Fan box power connector	D1, D2	LEDs
J3	+3-V power connector	SW2, SW3	Switchpacks
J4	Reserved	U1	MIC29502
J7	Power button connector	U3	MC12439
J8	Reset button connector	U4, U5, U7, U8, U12, U13, U15, U16	DC4047 Dchips
J10	SCSI LED connector	U6	DC1046 Cchip
J12	Halt button connector	U9, U10	100LVE222
J17	Parallel I/O connector	U11	MC100LVEL37
J18, J23	Daughtercard connectors	U14	MPC951
J19	COM1/COM2 (DB9) connectors[1]	U26	TIGbus FPGA
J20	Reserved	U27, U28	DC1048 Pchips
J21	Keyboard/mouse connector[2]	U30	AlphaBIOS flash ROM
J33	+5-V power connector	U31	I^2C bus controller
J34, J38	SCSI connectors	U46	SRAM for SCSI
J35, J40-J42, J44, J46	PCI connectors	U49	AIC7895
J36	Power LED connector	U50	SCSI BIOS flash ROM
J37	Reserved	U51	Super I/O (FDC37C669)
J39	Speaker connector	U57	Southbridge (CY82C693UB)
J43	Floppy drive connector		

[1] COM1 is the top connector, COM2 is the bottom one.
[2] Mouse connector is on the top, keyboard connector is on the bottom.

Board Layouts and Components

Figure 2–2 shows the AlphaPC 264DP daughtercard and its components, and Table 2–2 describes these components.

Figure 2–2 AlphaPC 264DP Daughtercard Switch/Connector/Component Location

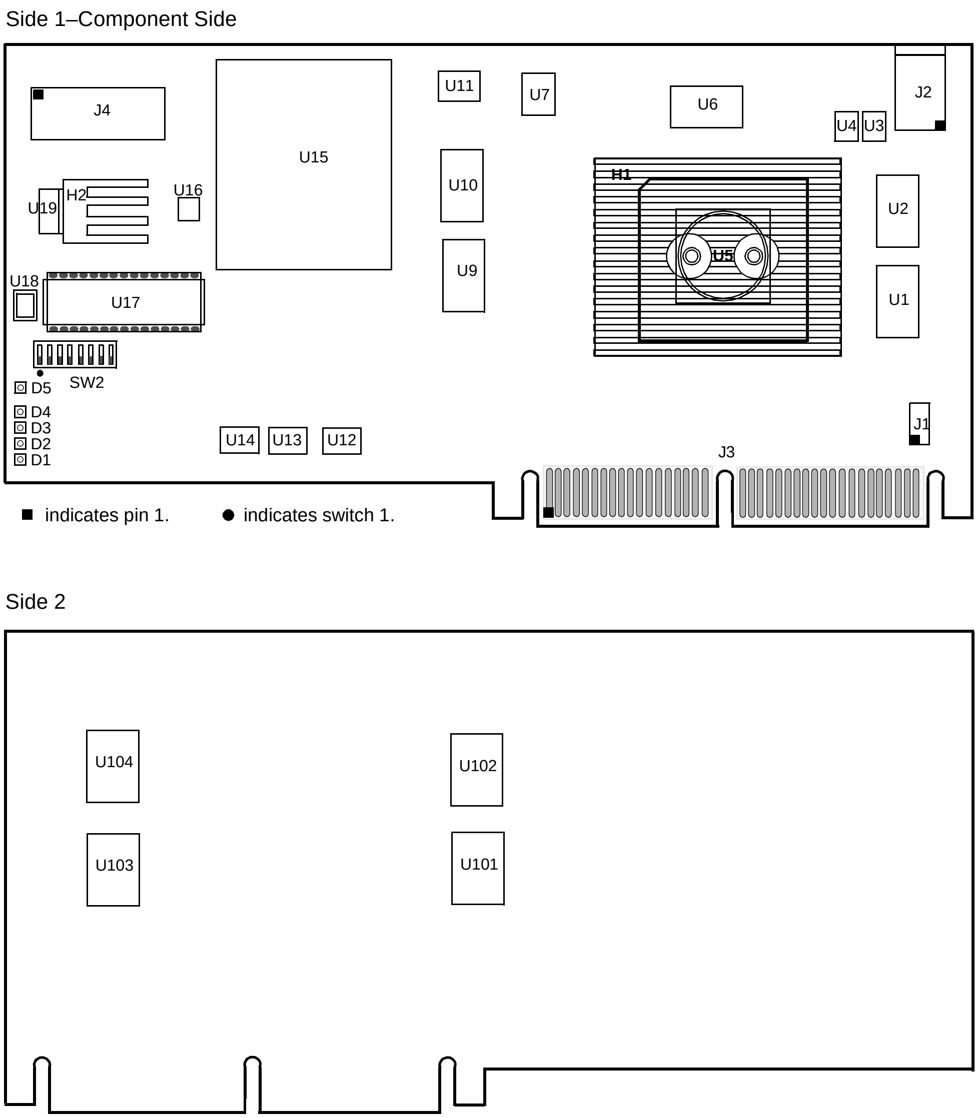


Table 2–2 AlphaPC 264DP Daughtercard Switch/Connector/Component List

Item No.	Description	Item No.	Description
J1	Fan power	U5	Microprocessor, socketed (Alpha 21264)
J2	SROM debug connector	U6	Bcache tag SSRAM
J3	Daughtercard data connector	U7	Reset FPGA
J4	Daughtercard power connector	U11, U13, U14	lcx38
H1	21264 heat sink	U12	8582 EEPROM
H2	+1.5-V regulator heat sink	U15	5-V to 2.2-V converter
D1-D5	LEDs	U16	tl7702b supervisor
SW2	Switchpack	U17	512K×8 flash ROM, socketed
U1, U2, U9, U10, U101-104	Bcache data SSRAMs	U18	74f151 multiplexer
U3	1489	U19	mic29302 3.3-V to 1.5-V regulator
U4	1488		

2.2 AlphaPC 264DP Mainboard Configuration Switches

The AlphaPC 264DP mainboard has two sets of programmable switches located at SW2 and SW3, as shown in Figure 2–1. These switches set the hardware configuration.

Note: There is no switchpack SW1 on production mainboards.

Figures 2–3 and 2–4 reflect the mainboard switches.

AlphaPC 264DP Mainboard Configuration Switches

Figure 2–3 Mainboard Switchpack 2

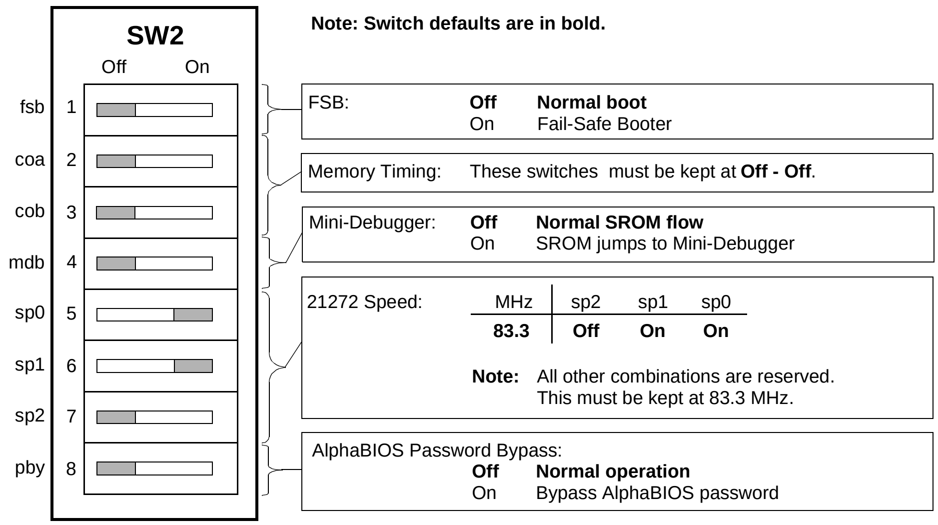
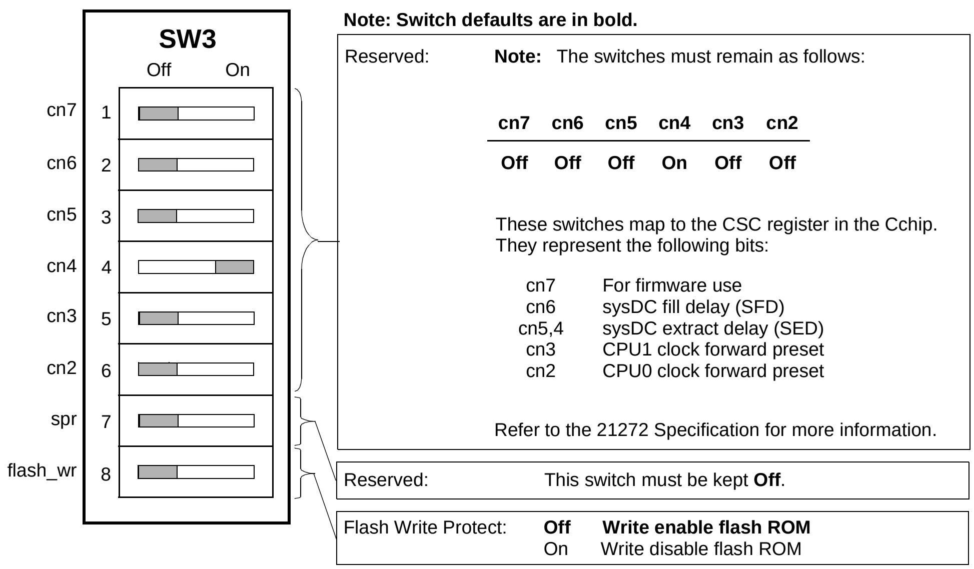


Figure 2–4 Mainboard Switchpack 3



2.2.1 Fail-Safe Booter

The Fail-Safe Booter (FSB) utility provides an emergency recovery mechanism when the primary firmware image contained in flash memory has been corrupted. When flash memory has been corrupted, and no image can be loaded safely from the flash ROM, you can run the FSB and boot another image from a diskette that is capable of reprogramming the flash ROM.

2.2.2 Memory Timing

The memory bus timing is controlled by switches 2 and 3 of SW2 on the mainboard (see Figure 2–3). Both switches are off by default, and they must be kept off.

2.2.3 Mini-Debugger

The Alpha SROM Mini-Debugger is stored in the flash ROM and is enabled/ disabled by switch 4 of SW2 on the mainboard (see Figure 2–3). The default position for this switch is off. When this switch is on, it causes the SROM initialization to trap to the Mini-Debugger after all initialization is complete, but before starting the execution of the system flash ROM code.

2.2.4 Password Bypass

AlphaBIOS provides password protection. However, if the use of passwords has been enabled and you have forgotten the current password, password bypass is provided through the use of switch 8 (pby) of SW2 on the mainboard.

Normal operation, with switch 8 in the off position (see Figure 2–3), requires a password. The password bypass function is enabled by setting the switch to the on position. This disables the AlphaBIOS password verification and enables the user to set up or start up their system without the AlphaBIOS password. Password bypass also clears the password.

After this function has been enabled, to disable it and require a password, set switch 8 to the off position.

2.2.5 Flash Write Protection

The AlphaPC 264DP provides write protection for the firmware flash ROM. By default, writing to the flash ROM is allowed, that is, switch 8 (flash_wr) of SW3 on the mainboard is off (see Figure 2–4).

Note: The AlphaPC 264DP will not function if switch 8 is in the on position.

2.2.6 21272 Speed

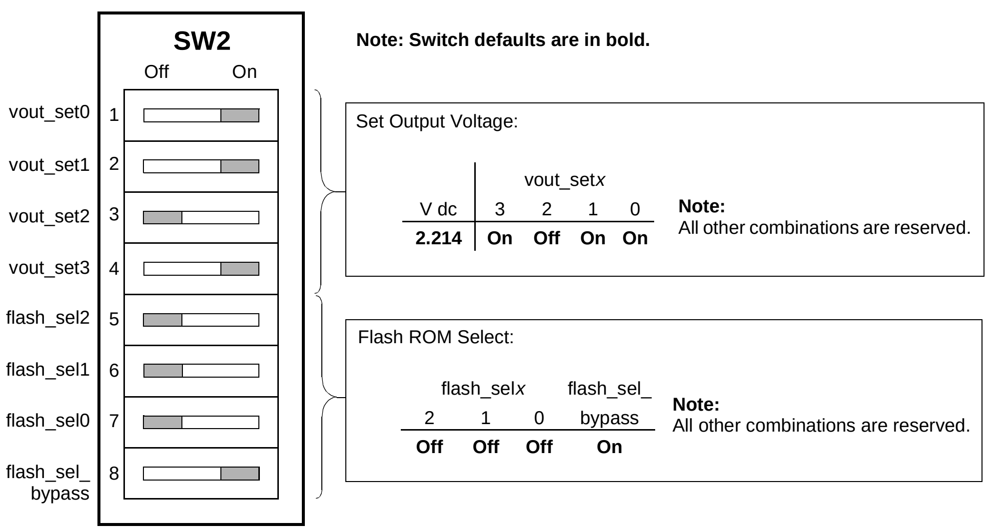
The speed of the 21272 core logic chipset is determined by switches 5–7 of SW2. The default positions are 5 and 6 on, 7 off. These switches must be kept in the default position.

2.3 AlphaPC 264DP Daughtercard Configuration Switches

The AlphaPC 264DP daughtercard has one switchpack, located at SW2, as shown previously in Figure 2–2. These switches set the hardware configuration. Figure 2–5 shows these switch configurations.

Note: There is no switchpack SW1 on production daughtercards. Onboard resistors set the configuration (cache size, CPU speed, and flash ROM use) to the default state.

Figure 2–5 Daughtercard Configuration Switches



2.4 AlphaPC 264DP Mainboard Connector Pinouts

This section lists the pinouts of the mainboard connectors (see Table 2–3 through Table 2–21). See Figure 2–1 for connector locations.

2.4.1 Daughtercard Connector Pinouts

Table 2–3 shows the daughtercard connector pinouts.

Table 2–3 Daughtercard Connector Pinouts (J18, J23)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	**vdd_3v**	2	**vdd_3v**	3	**vdd_3v**	4	**vdd_3v**
5	**vdd_3v**	6	**vdd_3v**	7	**vdd_3v**	8	**vdd_3v**
9	**sysdata2_l**	10	**sysdata0_l**	11	**sysdata5_l**	12	**sysdata3_l**
13	**syscheck0_l**	14	**sysdata9_l**	15	**sysdata10_l**	16	**sysdata13_l**
17	**sysdata14_l**	18	**sysdataoutclk1_l**	19	**sysdata16_l**	20	**syscheck20_l**
21	**sysdata17_l**	22	**sysdata18_l**	23	**sysdataoutclk2_l**	24	**sysdata21_l**
25	**sda**	26	**Gnd**	27	**Gnd**	28	**cpu_slot**
29	**sysdata26_l**	30	**sysdata25_l**	31	**sysdatainclk3_l**	32	**sysdata28_l**
33	**sysdata30_l**	34	**syscheck3_l**	35	**clkfwdreset_h**	36	**irq_0_h**
37	**irq_2_h**	38	**irq_4_h**	39	**2v_pwrgood_h**	40	**tsu_speed0**
41	**tsu_speed1**	42	**clk_rdy_h**	43	**tsu_speed2**	44	**sysfillvalid_l**
45	**sysaddin13_l**	46	**sysaddin8_l**	47	**sysaddin9_l**	48	**sysaddinclk_l**
49	**sysaddout13_l**	50	**sysaddin7_l**	51	**sysaddin1_l**	52	**sysaddin3_l**
53	**sysaddout14_l**	54	**sysaddout12_l**	55	**sysaddout10_l**	56	**sysaddoutclk_l**
57	**sysaddout6_l**	58	**sysaddout0_l**	59	**sysaddout2_l**	60	**syscheck7_l**
61	**sysaddout1_l**	62	**sysdata60_l**	63	**sysdatainclk7_l**	64	**sysdata52_l**
65	**sysdata54_l**	66	**sysdata57_l**	67	**sysdataoutclk6_l**	68	**sysdata51_l**
69	**sysdata49_l**	70	**syscheck5_l**	71	**sysdata46_l**	72	**sysdata47_l**
73	**sysdata45_l**	74	**sysdata42_l**	75	**sysdatainclk5_l**	76	**sysdata41_l**
77	**sysdataoutclk4_l**	78	**sysdata37_l**	79	**sysdata36_l**	80	**sysdata35_l**
81	**sysdata32_l**	82	**Gnd**	83	**bc_config1**	84	**bc_config3**
85	**cpu_speed1**	86	**+12v_mod**	87	**vdd_2v_term**	88	**vdd_2v_term**
89	**vdd_2v_term**	90	**vdd_2v_term**	91	**vdd_3v**	92	**vdd_3v**
93	**vdd_3v**	94	**vdd_3v**	95	**vdd_3v**	96	**vdd_3v**
97	**vdd_3v**	98	**vdd_3v**	99	**sysdatainclk0_l**	100	**sysdata6_l**
101	**sysdata1_l**	102	**sysdataoutclk0_l**	103	**sysdata4_l**	104	**sysdata7_l**
105	**sysdata8_l**	106	**sysdatainclk1_l**	107	**sysdata11_l**	108	**sysdata12_l**

Table 2–3 Daughtercard Connector Pinouts (J18, J23) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
109	**sysdata15_l**	110	**sysdata19_l**	111	**sysdatainclk2_l**	112	**sysdata20_l**
113	**sysdata22_l**	114	**sysdata23_l**	115	**pllbypass_h**	116	**srom_en_l**
117	**sclk**	118	**syscheck2_l**	119	**sysdata24_l**	120	**sysdata27_l**
121	**sysdataoutclk3_l**	122	**sysdata29_l**	123	**sysdata31_l**	124	**sysdataoutvalid_l**
125	**Gnd**	126	**Gnd**	127	**fan_ok_l**	128	**irq_1_h**
129	**irq_3_h**	130	**irq_5_h**	131	**mod_reset_l**	132	**sysaddin11_l**
133	**sysaddin14_l**	134	**sysdatainvalid_l**	135	**sysaddin10_l**	136	**sysaddin12_l**
137	**sysaddin4_l**	138	**sysaddin5_l**	139	**sysaddin2_l**	140	**sysaddin6_l**
141	**sysaddout11_l**	142	**sysaddin0_l**	143	**sysaddout7_l**	144	**sysaddout9_l**
145	**sysaddout8_l**	146	**sysaddout5_l**	147	**sysaddout4_l**	148	**sysaddout3_l**
149	**sysdata63_l**	150	**sysdata62_l**	151	**sysdata61_l**	152	**sysdata59_l**
153	**sysdataoutclk7_l**	154	**sysdata53_l**	155	**syscheck6_l**	156	**sysdata55_l**
157	**sysdata56_l**	158	**sysdata58_l**	159	**sysdatainclk6_l**	160	**sysdata50_l**
161	**sysdata48_l**	162	**sysdata44_l**	163	**sysdataoutclk5_l**	164	**sysdata43_l**
165	**sysdata40_l**	166	**sysdata38_l**	167	**syscheck4_l**	168	**sysdata39_l**
169	**sysdata34_l**	170	**sysdatainclk4_l**	171	**sysdata33_l**	172	**bc_config0**
173	**bc_config2**	174	**cpu_speed0**	175	**cpu_speed2**	176	**–12v_mod**
177	**vdd_2v_term**	178	**vdd_2v_term**	179	**vdd_2v_term**	180	**vdd_2v_term**
181 to 211	**Gnd**	212	**pecl_clkin_h**	213	**pecl_clkin_l**	214	**Gnd**
215	**frameclk_h**	216	**frameclk_l**	217 to 270	**Gnd**		

2.4.2 PCI Bus Connector Pinouts

Table 2–4 shows the PCI bus connector pinouts.

Table 2–4 PCI Bus Connector Pinouts (J35, J40–J42, J44, J46)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	**TRST#**	A2	**+12V**	A3	**TMS**	A4	**TDI**
A5	**Vdd**	A6	**INTA**	A7	**INTC**	A8	**Vdd**
A9	—	A10	**Vdd**	A11	—	A12	**Gnd**
A13	**Gnd**	A14	—	A15	**RST#**	A16	**Vdd**
A17	**GNT#**	A18	**Gnd**	A19	—	A20	**AD[30]**
A21	**+3V**	A22	**AD[28]**	A23	**AD[26]**	A24	**Gnd**
A25	**AD[24]**	A26	**IDSEL**	A27	**+3V**	A28	**AD[22]**
A29	**AD[20]**	A30	**Gnd**	A31	**AD[18]**	A32	**AD[16]**
A33	**+3V**	A34	**FRAME#**	A35	**Gnd**	A36	**TRDY#**
A37	**STOP#**	A38	**STOP#**	A39	**+3V**	A40	**SDONE**
A41	**SBO#**	A42	**Gnd**	A43	**PAR**	A44	**AD[15]**
A45	**+3V**	A46	**AD[13]**	A47	**AD[11]**	A48	**Gnd**
A49	**AD[09]**	A50	Not used	A51	Not used	A52	**C/BE#[0]**
A53	**+3V**	A54	**AD[06]**	A55	**AD[04]**	A56	**Gnd**
A57	**AD[02]**	A58	**AD[00]**	A59	**Vdd**	A60	**REQ64#**
A61	**Vdd**	A62	**Vdd**	B1	**-12V**	B2	**TCK**
B3	**Gnd**	B4	**TDO**	B5	**Vdd**	B6	**Vdd**
B7	**INTB**	B8	**INTD**	B9	**PRSNT1#**	B10	—
B11	**PRSNT2#**	B12	**Gnd**	B13	**Gnd**	B14	—
B15	**Gnd**	B16	**CLK**	B17	**Gnd**	B18	**REQ#**
B19	**Vdd**	B20	**AD[31]**	B21	**AD[29]**	B22	**Gnd**
B23	**AD[27]**	B24	**AD[25]**	B25	**+3V**	B26	**C/BE#[3]**
B27	**AD[23]**	B28	**Gnd**	B29	**AD[21]**	B30	**AD[19]**
B31	**+3V**	B32	**AD[17]**	B33	**C/BE#[2]**	B34	**Gnd**
B35	**IRDY#**	B36	**+3V**	B37	**DEVSEL#**	B38	**Gnd**
B39	**LOCK#**	B40	**PERR#**	B41	**+3V**	B42	**SERR#**
B43	**+3V**	B44	**C/BE#[1]**	B45	**AD[14]**	B46	**Gnd**
B47	**AD[12]**	B48	**AD[10]**	B49	**Gnd**	B50	Not used
B51	Not used	B52	**AD[08]**	B53	**AD[07]**	B54	**+3V**
B55	**AD[05]**	B56	**AD[03]**	B57	**Gnd**	B58	**AD[01]**
B59	**Vdd**	B60	**ACK64#**	B61	**Vdd**	B62	**Vdd**

Table 2–4 PCI Bus Connector Pinouts (J35, J40–J42, J44, J46) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A63	**Gnd**	A64	**C/BE#[7]**	A65	**C/BE#[5]**	A66	**Vdd**
A67	**PAR64**	A68	**D[62]**	A69	**Gnd**	A70	**D[60]**
A71	**D[58]**	A72	**Gnd**	A73	**D[56]**	A74	**D[54]**
A75	**Vdd**	A76	**D[52]**	A77	**D[50]**	A78	**Gnd**
A79	**D[48]**	A80	**D[46]**	A81	**Gnd**	A82	**D[44]**
A83	**D[42]**	A84	**Vdd**	A85	**D[40]**	A86	**D[38]**
A87	**Gnd**	A88	**D[36]**	A89	**D[34]**	A90	**Gnd**
A91	**D[32]**	A92	—	A93	**Gnd**	A94	—
B63	—	B64	**Gnd**	B65	**C/BE#[6]**	B66	**C/BE#[4]**
B67	**Gnd**	B68	**D[63]**	B69	**D[61]**	B70	**Vdd**
B71	**D[59]**	B72	**D[57]**	B73	**Gnd**	B74	**D[55]**
B75	**D[53]**	B76	**Gnd**	B77	**D[51]**	B78	**D[49]**
B79	**Vdd**	B80	**D[47]**	B81	**D[45]**	B82	**Gnd**
B83	**D[43]**	B84	**D[41]**	B85	**Gnd**	B86	**D[39]**
B87	**D[37]**	B88	**Vdd**	B89	**D[35]**	B90	**D[33]**
B91	**Gnd**	B92	—	B93	—	B94	**Gnd**

2.4.3 ISA Expansion Bus Connector Pinouts

Table 2–5 shows the ISA expansion bus connector pinouts.

Table 2–5 ISA Expansion Bus Connector Pinouts (J47)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	**Gnd**	2	**IOCHCK#**	3	**RSTDRV**	4	**SD7**
5	**Vdd**	6	**SD6**	7	**IRQ9**	8	**SD5**
9	**–5V**	10	**SD4**	11	**DRQ2**	12	**SD3**
13	**–12V**	14	**SD2**	15	**ZEROWS#**	16	**SD1**
17	**+12V**	18	**SD0**	19	**Gnd**	20	**IOCHRDY**
21	**SMEMW#**	22	**AEN**	23	**SMEMR#**	24	**SA19**
25	**IOW#**	26	**SA18**	27	**IOR#**	28	**SA17**
29	**DACK3#**	30	**SA16**	31	**DRQ3**	32	**SA15**
33	**DACK1#**	34	**SA14**	35	**DRQ1**	36	**SA13**
37	**REFRESH#**	38	**SA12**	39	**SYSCLK**	40	**SA11**
41	**IRQ7**	42	**SA10**	43	**IRQ6**	44	**SA9**
45	**IRQ5**	46	**SA8**	47	**IRQ4**	48	**SA7**
49	**IRQ3**	50	**SA6**	51	**DACK2#**	52	**SA5**
53	**TC**	54	**SA4**	55	**BALE**	56	**SA3**
57	**Vdd**	58	**SA2**	59	**OSC**	60	**SA1**
61	**Gnd**	62	**SA0**	63	**MEMCS16#**	64	**SBHE#**
65	**IOCS16#**	66	**LA23**	67	**IRQ10**	68	**LA22**
69	**IRQ11**	70	**LA21**	71	**IRQ12**	72	**LA20**
73	**IRQ15**	74	**LA19**	75	**IRQ14**	76	**LA18**
77	**DACK0#**	78	**LA17**	79	**DRQ0**	80	**MEMR#**
81	**DACK5#**	82	**MEMW#**	83	**DRQ5**	84	**SD8**
85	**DACK6#**	86	**SD9**	87	**DRQ6**	88	**SD10**
89	**DACK7#**	90	**SD11**	91	**DRQ7**	92	**SD12**
93	**Vdd**	94	**SD13**	95	**MASTER#**	96	**SD14**
97	**Gnd**	98	**SD15**	—	—	—	—

2.4.4 IDE Drive Bus Connector Pinouts

Table 2–6 shows the IDE drive bus connector pinouts.

Table 2–6 IDE Drive Bus Connector Pinouts (J45)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	**DRST**	2	**Gnd**	3	**IDE_D7**	4	**IDE_D8**
5	**IDE_D6**	6	**IDE_D9**	7	**IDE_D5**	8	**IDE_D10**
9	**IDE_D4**	10	**IDE_D11**	11	**IDE_D3**	12	**IDE_D12**
13	**IDE_D2**	14	**IDE_D13**	15	**IDE_D1**	16	**IDE_D14**
17	**IDE_D0**	18	**IDE_D15**	19	**Gnd**	20	NC (key pin)
21	**IDE_REQ0**	22	**Gnd**	23	**IDE_IOW1#**	24	**Gnd**
25	**IOR#**	26	**Gnd**	27	**CHRDY**	28	**BALE**
29	**MACK**	30	**Gnd**	31	**IRQ**	32	**IOCS16#**
33	**ADDR1**	34	NC	35	**ADDR0**	36	**ADDR2**
37	**CS0#**	38	**CS1#**	39	**ACT#**	40	**Gnd**

2.4.5 Ultra SCSI Bus Connector Pinouts

Table 2–7 shows the Ultra SCSI bus connector pinouts.

Table 2–7 Ultra SCSI Bus Connector Pinouts (J34, J38)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	**Gnd**	2	**Gnd**	3	**Gnd**	4	**Gnd**
5	**Gnd**	6	**Gnd**	7	**Gnd**	8	**Gnd**
9	**Gnd**	10	**Gnd**	11	**Gnd**	12	**Gnd**
13	**Gnd**	14	**Gnd**	15	**Gnd**	16	**Gnd**
17	**termpwr**	18	**termpwr**	19	NC	20	**Gnd**
21	**Gnd**	22	**Gnd**	23	**Gnd**	24	**Gnd**
25	**Gnd**	26	**Gnd**	27	**Gnd**	28	**Gnd**
29	**Gnd**	30	**Gnd**	31	**Gnd**	32	**Gnd**
33	**Gnd**	34	**Gnd**	35	**scd12**	36	**scd13**
37	**scd14**	38	**scd15**	39	**scdph**	40	**scd0**
41	**scd1**	42	**scd2**	43	**scd3**	44	**scd4**
45	**scd5**	46	**scd6**	47	**scd7**	48	**scdpl**
49	**Gnd**	50	**Gnd**	51	**termpwr**	52	**termpwr**
53	NC	54	**Gnd**	55	**atn**	56	**Gnd**

Table 2–7 Ultra SCSI Bus Connector Pinouts (J34, J38) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
57	**bsy**	58	**ack**	59	**reset**	60	**msg**
61	**sel**	62	**cd**	63	**req**	64	**io**
65	**scd8**	66	**scd9**	67	**scd10**	68	**scd11**

2.4.6 SDRAM DIMM Connector Pinouts

Table 2–8 shows the SDRAM DIMM connector pinouts.

Table 2–8 SDRAM DIMM Connector Pinouts (J1, J5, J6, J9, J11, J13, J14, J16, J25–J32)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	**Vdd**	2	NC	3	NC	4	NC
5	NC	6	NC	7	NC	8	**Vss**
9	**dq67**	10	**dq66**	11	**Vdd**	12	**dq65**
13	**dq64**	14	**Vss**	15	**dq63**	16	**dq62**
17	NC	18	**dq61**	19	**dq60**	20	**Vdd**
21	NC	22	NC	23	**Vss**	24	NC
25	NC	26	**Vdd**	27	**dq51**	28	**dq50**
29	**Vss**	30	**dq49**	31	**dq48**	32	**Vdd**
33	**dq43**	34	**dq42**	35	**Vss**	36	**dq41**
37	**dq40**	38	**Vdd**	39	**a4**	40	**a5**
41	**Vss**	42	**a8**	43	**a9**	44	**Vdd**
45	NC	46	**cke0**	47	**Vss**	48	**cas#**
49	NC	50	**Vdd**	51	**Vss**	52	**ras#**
53	**Vss**	54	**cs2#**	55	**a11**	56	**Vdd**
57	**a0**	58	**a1**	59	**Vss**	60	**dq35**
61	**dq34**	62	**Vdd**	63	**dq33**	64	**dq32**
65	**Vss**	66	**dq27**	67	**dq26**	68	**Vdd**
69	**dq25**	70	**dq24**	71	**Vss**	72	**dq19**
73	**dq18**	74	**Vdd**	75	**dq17**	76	**dq16**
77	**Vss**	78	NC	79	NC	80	**Vdd**
81	**dq15**	82	**dq14**	83	**Vss**	84	**dq13**
85	**dq12**	86	**Vdd**	87	**dq7**	88	**dq6**
89	**Vss**	90	**dq5**	91	**dq4**	92	**Vdd**
93	NC	94	NC	95	NC	96	NC
97	NC	98	**scl**	99	NC	100	**Vss**

Table 2–8 SDRAM DIMM Connector Pinouts (J1, J5, J6, J9, J11, J13, J14, J16, J25–J32) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
101	NC	102	NC	103	**Vss**	104	**rege**
105	**rfu**	106	**rfu**	107	NC	108	**dq71**
109	**dq70**	110	**Vss**	111	**dq69**	112	**dq68**
113	**Vdd**	114	NC	115	**Vss**	116	NC
117	**dq59**	118	**dq58**	119	**Vss**	120	**dq57**
121	**dq56**	122	**Vdd**	123	**dq55**	124	**dq54**
125	**Vss**	126	**dq53**	127	**dq52**	128	**Vdd**
129	**dq47**	130	**dq46**	131	**Vss**	132	**dq45**
133	**dq44**	134	**Vdd**	135	**dq39**	136	**dq38**
137	**Vss**	138	**dq37**	139	**dq36**	140	**Vdd**
141	**a6**	142	**a7**	143	**Vss**	144	**bs0**
145	NC	146	**Vdd**	147	**dqm**	148	**we#**
149	**Vss**	150	NC	151	**clk0**	152	**Vdd**
153	NC	154	**cs0#**	155	**Vss**	156	**ba1**
157	**a10/ap**	158	**Vdd**	159	**a2**	160	**a3**
161	**Vss**	162	**dq31**	163	**dq30**	164	**Vdd**
165	**dq29**	166	**dq28**	167	**Vss**	168	**dq23**
169	**dq22**	170	**Vdd**	171	**dq21**	172	**dq20**
173	**Vss**	174	NC	175	NC	176	**Vdd**
177	NC	178	**Vss**	179	**Vss**	180	NC
181	NC	182	**Vdd**	183	**dq11**	184	**dq10**
185	**Vss**	186	**dq9**	187	**dq8**	188	**Vdd**
189	**dq3**	190	**dq2**	191	**Vss**	192	**dq1**
193	**dq0**	194	**sda**	195	**sa0**	196	**sa1**
197	**sa2**	198	**Vdd**	199	NC	200	NC

2.4.7 Diskette (Floppy) Drive Bus Connector Pinouts

Table 2–9 shows the diskette (floppy) drive bus connector pinouts.

Table 2–9 Diskette (Floppy) Drive Bus Connector Pinouts (J43)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	**Gnd**	2	**DRVDEN0**	3	**Gnd**	4	NC
5	**Gnd**	6	**DRVDEN1**	7	**Gnd**	8	**INDEX**
9	**Gnd**	10	**MTR0**	11	**Gnd**	12	**DS1**
13	**Gnd**	14	**DS0**	15	**Gnd**	16	**MTR1**
17	**Gnd**	18	**DIR**	19	**Gnd**	20	**STEP**
21	**Gnd**	22	**WDATA**	23	**Gnd**	24	**WGATE**
25	**Gnd**	26	**TRK0**	27	**Gnd**	28	**WRTPRT**
29	**Gnd**	30	**RDATA**	31	**Gnd**	32	**HDSEL**
33	**Gnd**	34	**DSKCHG**	—	—	—	—

2.4.8 Parallel Bus Connector Pinouts

Table 2–10 shows the parallel bus connector pinouts.

Table 2–10 Parallel Bus Connector Pinouts (J17)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	**PSTB**	2	**PD0**	3	**PD1**	4	**PD2**
5	**PD3**	6	**PD4**	7	**PD5**	8	**PD6**
9	**PD7**	10	**PACK**	11	**PBUSY**	12	**PE**
13	**PSLCT**	14	**PAFD**	15	**PAR_ERROR**	16	**PINIT**
17	**PSLIN**	18	**Gnd**	19	**Gnd**	20	**Gnd**
21	**Gnd**	22	**Gnd**	23	**Gnd**	24	**Gnd**
25	**Gnd**	—	—	—	—	—	—

2.4.9 COM1/COM2 Serial Line Connector Pinouts

Table 2–11 shows the COM1/COM2 serial line connector pinouts.

Table 2–11 COM1/COM2 Serial Line Connector Pinouts (J19)

COM1 Pin (Top)	COM1 Signal	COM2 Pin (Bottom)	COM2 Signal
1	**DCD1**	10	**DCD2**
2	**SIN1**	11	**SIN2**
3	**SOUT1**	12	**SOUT2**
4	**DTR1**	13	**DTR2**
5	**Gnd**	14	**Gnd**
6	**DSR1**	15	**DSR2**
7	**RTS1**	16	**RTS2**
8	**CTS1**	17	**CTS2**
9	**RI1**	18	**RI2**

2.4.10 Keyboard/Mouse Connector Pinouts

Table 2–12 shows the keyboard/mouse connector pinouts.

Table 2–12 Keyboard/Mouse Connector Pinouts (J21)

Keyboard Pin (Top)	Keyboard Signal	Mouse Pin (Bottom)	Mouse Signal
1	**KBDATA**	7	**MSDATA**
2	NC	8	NC
3	**Gnd**	9	**Gnd**
4	**Vdd**	10	**Vdd**
5	**KBCLK**	11	**MSCLK**
6	NC	12	NC

2.4.11 +3-V Power Connector Pinouts

Table 2–13 shows the +3-V power connector pinouts.

Table 2–13 +3-V Power Connector Pinouts (J3)

Pin	Voltage	Pin	Voltage	Pin	Voltage	Pin	Voltage
1	**vdd_3v**	2	**Gnd**	3	**vdd_3v**	4	**Gnd**
5	**vdd_3v**	6	**Gnd**	7	**vdd_3v**	8	**Gnd**
9	**vdd_3v**	10	**Gnd**	11	**vdd_3v**	12	**Gnd**
13	**Gnd**	14	**vdd_3v**	15	**Gnd**	16	**vdd_3v**
17	**Gnd**	18	**vdd_3v**	19	**Gnd**	20	**vdd_3v**
21	+12 V dc	22	**ps_on**	23	**pok**	24	**5vsb**

2.4.12 +5-V Power Connector Pinouts

Table 2–14 shows the +5-V power connector pinouts.

Table 2–14 +5-V Power Connector Pinouts (J33)

Pin	Voltage	Pin	Voltage	Pin	Voltage	Pin	Voltage
1	**vdd_5v**	2	**Gnd**	3	**vdd_5v**	4	**Gnd**
5	**vdd_5v**	6	**Gnd**	7	**vdd_5v**	8	**Gnd**
9	**Gnd**	10	**vdd_5v**	11	**Gnd**	12	**vdd_5v**
13	**Gnd**	14	**vdd_5v**	15	-12 V dc	16	-5 V dc

2.4.13 Fan Box Power Connector Pinouts

Table 2–15 shows the fan box power connector pinouts.

Table 2–15 Fan Box Power Connector Pinouts (J2, J15, J22, J24)

Pin	Voltage	Pin	Voltage
1	**Gnd**	2	+12 V dc

2.4.14 Speaker Connector Pinouts

Table 2–16 shows the speaker connector pinouts.

Table 2–16 Speaker Connector Pinouts (J39)

Pin	Signal	Description
1	**spkr**	Speaker input
2	**vdd_5v**	—
3	**Gnd**	—
4	**vdd_5v**	—

2.4.15 Halt Button Connector Pinouts

Table 2–17 shows the halt button connector pinouts.

Table 2–17 Halt Button Connector Pinouts (J12)

Pin	Signal	Description
1	**halt_button**	Halt system (for Tru64 UNIX only)
2	**vdd_5v**	—

2.4.16 Reset Button Connector Pinouts

Table 2–18 shows the reset button connector pinouts.

Table 2–18 Reset Button Connector Pinouts (J8)

Pin	Signal	Description
1	**reset_button**	Reset system
2	**vdd_5v**	—

2.4.17 System Power Button Connector Pinouts

Table 2–19 shows the system power button connector pinouts.

Table 2–19 System Power Button Connector Pinouts (J7)

Pin	Signal	Description
1	**ps_on**	System power on/off
2	**Gnd**	—

2.4.18 Ultra SCSI Hard Drive LED Connector Pinouts

Table 2–20 shows the ultra SCSI hard drive LED connector pinouts.

Table 2–20 Ultra SCSI Hard Drive LED Connector Pinouts (J10)

Pin	Signal	Description
1	**scsi_hd_act**	Hard drive active
2	**vdd_5v**	—

2.4.19 Power LED Connector Pinouts

Table 2–21 shows the power LED connector pinouts.

Table 2–21 Power LED Connector Pinouts (J36)

Pin	Signal	Description
1	**power_led**	Power LED input
2	**Gnd**	—
3	NC	—
4	NC	—
5	NC	—

2.5 AlphaPC 264DP Daughtercard Connector Pinouts

This section lists the pinouts of the AlphaPC 264DP daughtercard connectors (see Table 2–22 through Table 2–25). See Figure 2–2 for connector locations.

2.5.1 Microprocessor Fan Power Connector Pinouts

Table 2–22 shows the microprocessor fan power connector pinouts.

Table 2–22 Microprocessor Fan Power Connector Pinouts (J1)

Pin	Signal	Description
1, 6	+12 V dc	—
2, 5	**Gnd**	—
3, 4	**fan_conn_l**	Fan connected

2.5.2 SROM Test Data Input Connector Pinouts

Table 2–23 shows the SROM test data input connector pinouts.

Table 2–23 SROM Test Data Input Connector Pinouts (J2)

Pin	Signal	Description
1	NC	—
2	**srom_clk_l**	Clock out
3	**Gnd**	—
4	NC	—
5	**test_srom_d_l**	SROM serial data in
6	NC	—

2.5.3 AlphaPC 264DP Daughtercard Connector Pinouts

Table 2–24 shows the AlphaPC 264DP daughtercard connector pinouts.

Table 2–24 Daughtercard Connector Pinouts (J3)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	**vdd_3v**	2	**vdd_3v**	3	**vdd_3v**	4	**vdd_3v**
5	**vdd_3v**	6	**vdd_3v**	7	**vdd_3v**	8	**vdd_3v**
9	**sysdata2_l**	10	**sysdata0_l**	11	**sysdata5_l**	12	**sysdata3_l**
13	**syscheck0_l**	14	**sysdata9_l**	15	**sysdata10_l**	16	**sysdata13_l**
17	**sysdata14_l**	18	**sysdataoutclk1_l**	19	**sysdata16_l**	20	**syscheck20_l**
21	**sysdata17_l**	22	**sysdata18_l**	23	**sysdataoutclk2_l**	24	**sysdata21_l**

Table 2–24 Daughtercard Connector Pinouts (J3) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
25	**sda**	26	**Gnd**	27	**Gnd**	28	**cpu_slot**
29	**sysdata26_l**	30	**sysdata25_l**	31	**sysdatainclk3_l**	32	**sysdata28_l**
33	**sysdata30_l**	34	**syscheck3_l**	35	**clkfwdreset_h**	36	**irq_0_h**
37	**irq_2_h**	38	**irq_4_h**	39	**2v_pwrgood_h**	40	**tsu_speed0**
41	**tsu_speed1**	42	**clk_rdy_h**	43	**tsu_speed2**	44	**sysfillvalid_l**
45	**sysaddin13_l**	46	**sysaddin8_l**	47	**sysaddin9_l**	48	**sysaddinclk_l**
49	**sysaddout13_l**	50	**sysaddin7_l**	51	**sysaddin1_l**	52	**sysaddin3_l**
53	**sysaddout14_l**	54	**sysaddout12_l**	55	**sysaddout10_l**	56	**sysaddoutclk_l**
57	**sysaddout6_l**	58	**sysaddout0_l**	59	**sysaddout2_l**	60	**syscheck7_l**
61	**sysaddout1_l**	62	**sysdata60_l**	63	**sysdatainclk7_l**	64	**sysdata52_l**
65	**sysdata54_l**	66	**sysdata57_l**	67	**sysdataoutclk6_l**	68	**sysdata51_l**
69	**sysdata49_l**	70	**syscheck5_l**	71	**sysdata46_l**	72	**sysdata47_l**
73	**sysdata45_l**	74	**sysdata42_l**	75	**sysdatainclk5_l**	76	**sysdata41_l**
77	**sysdataoutclk4_l**	78	**sysdata37_l**	79	**sysdata36_l**	80	**sysdata35_l**
81	**sysdata32_l**	82	**Gnd**	83	**bc_config1**	84	**bc_config3**
85	**cpu_speed1**	86	**+12v_mod**	87	**vdd_2v_term**	88	**vdd_2v_term**
89	**vdd_2v_term**	90	**vdd_2v_term**	91	**vdd_3v**	92	**vdd_3v**
93	**vdd_3v**	94	**vdd_3v**	95	**vdd_3v**	96	**vdd_3v**
97	**vdd_3v**	98	**vdd_3v**	99	**sysdatainclk0_l**	100	**sysdata6_l**
101	**sysdata1_l**	102	**sysdataoutclk0_l**	103	**sysdata4_l**	104	**sysdata7_l**
105	**sysdata8_l**	106	**sysdatainclk1_l**	107	**sysdata11_l**	108	**sysdata12_l**
109	**sysdata15_l**	110	**sysdata19_l**	111	**sysdatainclk2_l**	112	**sysdata20_l**
113	**sysdata22_l**	114	**sysdata23_l**	115	**pllbypass_h**	116	**srom_en_l**
117	**sclk**	118	**syscheck2_l**	119	**sysdata24_l**	120	**sysdata27_l**
121	**sysdataoutclk3_l**	122	**sysdata29_l**	123	**sysdata31_l**	124	**sysdataoutvalid_l**
125	**Gnd**	126	**Gnd**	127	**fan_ok_l**	128	**irq_1_h**
129	**irq_3_h**	130	**irq_5_h**	131	**mod_reset_l**	132	**sysaddin11_l**
133	**sysaddin14_l**	134	**sysdatainvalid_l**	135	**sysaddin10_l**	136	**sysaddin12_l**
137	**sysaddin4_l**	138	**sysaddin5_l**	139	**sysaddin2_l**	140	**sysaddin6_l**
141	**sysaddout11_l**	142	**sysaddin0_l**	143	**sysaddout7_l**	144	**sysaddout9_l**
145	**sysaddout8_l**	146	**sysaddout5_l**	147	**sysaddout4_l**	148	**sysaddout3_l**
149	**sysdata63_l**	150	**sysdata62_l**	151	**sysdata61_l**	152	**sysdata59_l**
153	**sysdataoutclk7_l**	154	**sysdata53_l**	155	**syscheck6_l**	156	**sysdata55_l**
157	**sysdata56_l**	158	**sysdata58_l**	159	**sysdatainclk6_l**	160	**sysdata50_l**

Table 2–24 Daughtercard Connector Pinouts (J3) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
161	**sysdata48_l**	162	**sysdata44_l**	163	**sysdataoutclk5_l**	164	**sysdata43_l**
165	**sysdata40_l**	166	**sysdata38_l**	167	**syscheck4_l**	168	**sysdata39_l**
169	**sysdata34_l**	170	**sysdatainclk4_l**	171	**sysdata33_l**	172	**bc_config0**
173	**bc_config2**	174	**cpu_speed0**	175	**cpu_speed2**	176	**–12v_mod**
177	**vdd_2v_term**	178	**vdd_2v_term**	179	**vdd_2v_term**	180	**vdd_2v_term**
181 to 211	**Gnd**	212	**pecl_clkin_h**	213	**pecl_clkin_l**	214	**Gnd**
215	**frameclk_h**	216	**frameclk_l**	217 to 270	**Gnd**		

2.5.4 AlphaPC 264DP Daughtercard Input Power Connector Pinouts

Table 2–25 shows the input power connector pinouts.

Table 2–25 Input Power Connector Pinouts (J4)

Pin	Voltage	Pin	Voltage	Pin	Voltage	Pin	Voltage
1	+5 V dc	2	**Gnd**	3	+5 V dc	4	**Gnd**
5	+5 V dc	6	**Gnd**	7	+5 V dc	8	**Gnd**
9	+5 V dc	10	**Gnd**	11	+5 V dc	12	**Gnd**
13	+5 V dc	14	**Gnd**	15	+5 V dc	16	**Gnd**
17	+5 V dc	18	**Gnd**				

3
Power and Environmental Requirements

This chapter describes the AlphaPC 264DP power and environmental requirements and physical board parameters, for both the mainboard and the daughtercard.

3.1 Power Requirements

The mainboard has a maximum total power dissipation of 215 W, excluding any disk drives. Each daughtercard has a maximum total power dissipation of 129 W. Table 3–1 lists the current requirement for each dc supply voltage.

Table 3–1 Power Supply DC Current Requirements

Voltage/Tolerance	Current
Mainboard	
+3.3 V dc, ±5%	30.0 A
+5 V dc, ±5%	20.0 A
5 VSB dc, ±5%	1.0 A
+12 V dc, ±5%	0.8 A
–12 V dc, ±5%	0.1 A
Daughtercard	
+3.3 V dc, ±5%	5.0 A
+5 V dc, ±5%	22.0 A
+12 V dc, ±5%	0.1 A
–12 V dc, ±5%	0.05 A

Caution: **Fan sensor required**. The 21264 microprocessor cooling fan *must* have a built-in sensor that will drive a signal if the airflow stops. The sensor is connected to power connector J1. When the signal is generated, it resets the system.

3.2 Environmental Requirements

The 21264 microprocessor is cooled by a small fan blowing directly into the chip's heat sink. The daughtercard is designed to run efficiently by using only this fan. Additional fans may be necessary depending upon cabinetry and the requirements of plug-in cards.

The AlphaPC 264DP mainboard and daughtercard are specified to run within the environment listed in Table 3–2.

Table 3–2 AlphaPC 264DP Environmental Requirements

Parameter	Specification
Operating temperature	10°C to 40°C (50°F to 104°F)
Storage temperature	–55°C to 125°C (–67°F to 257°F)
Relative humidity	10% to 90% with maximum wet bulb temperature 28°C (82°F) and minimum dew point 2°C (36°F)
Rate of (dry bulb) temperature change	11°C/hour ±2°C/hour (20°F/hour ±4°F/hour)

3.3 Physical Parameters

The mainboard is a printed-wiring board (PWB) with the following dimensions:

- Length: 42.11 cm (16.58 in ±0.0005 in)
- Width: 33.02 cm (13.0 in ±0.0005 in)
- Height: 3.81 cm (1.5 in)

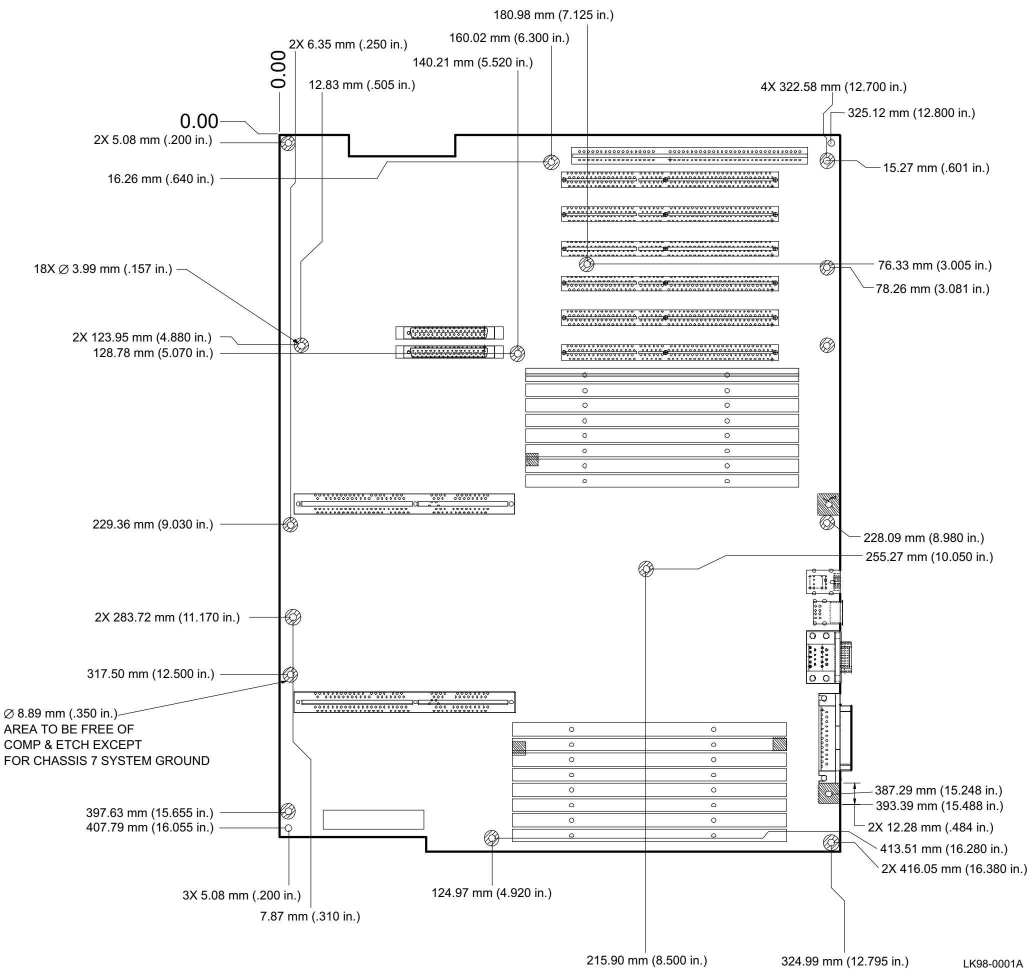
The daughtercard is a PWB with the following dimensions:

- Length: 30.48 cm (12.0 in ±0.0005 in)
- Width: 14.99 cm (5.905 in ±0.0005 in)
- Height: 6.40 cm (2.52 in ±0.0005 in)

3.4 AlphaPC 264DP Hole and Connector Specifications

Figure 3–1 shows the AlphaPC 264DP mainboard's hole specifications.

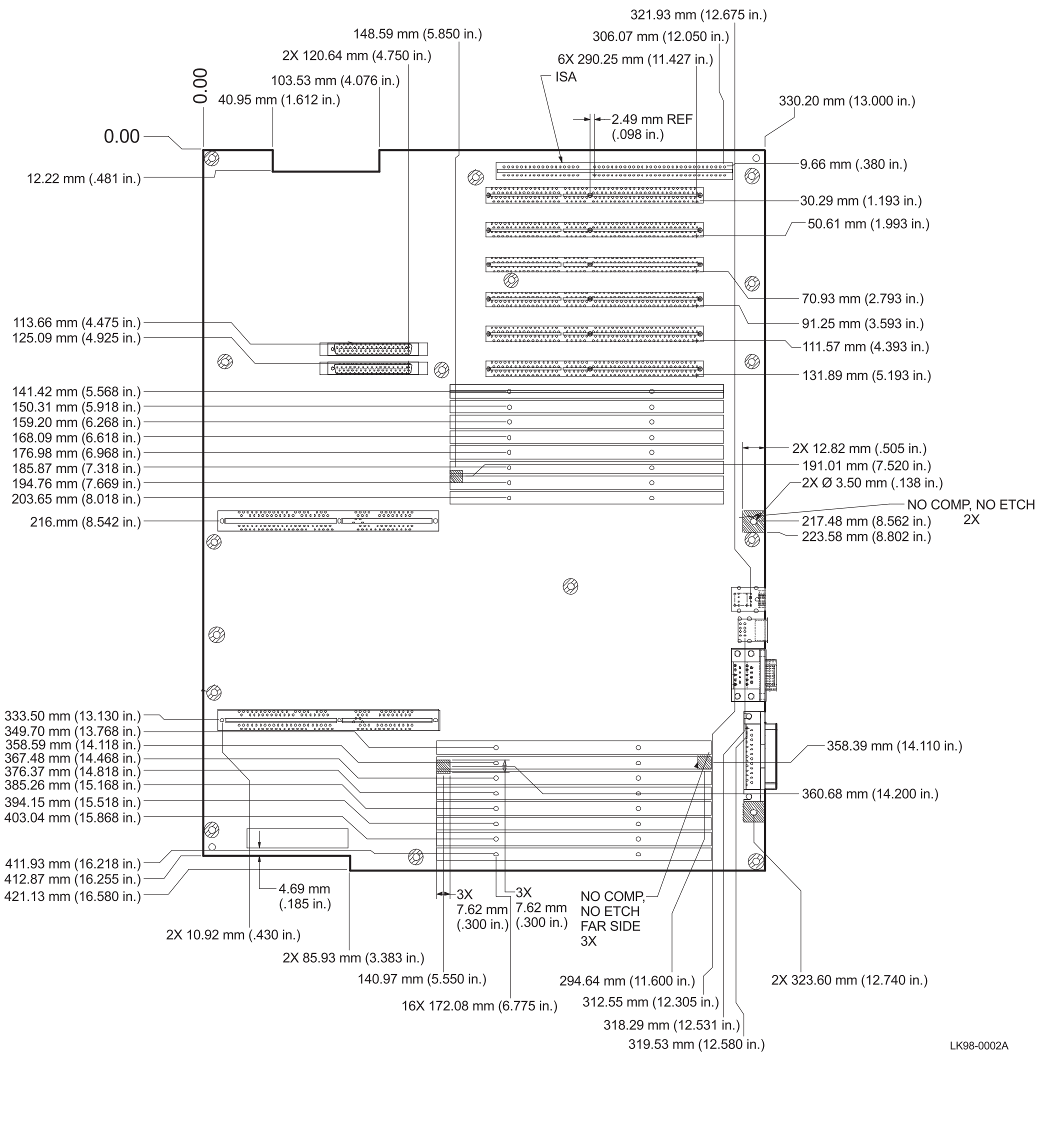
Figure 3–1 AlphaPC 264DP Mainboard Hole Specifications



AlphaPC 264DP Hole and Connector Specifications

Figure 3–2 shows the mainboard’s connector specifications.

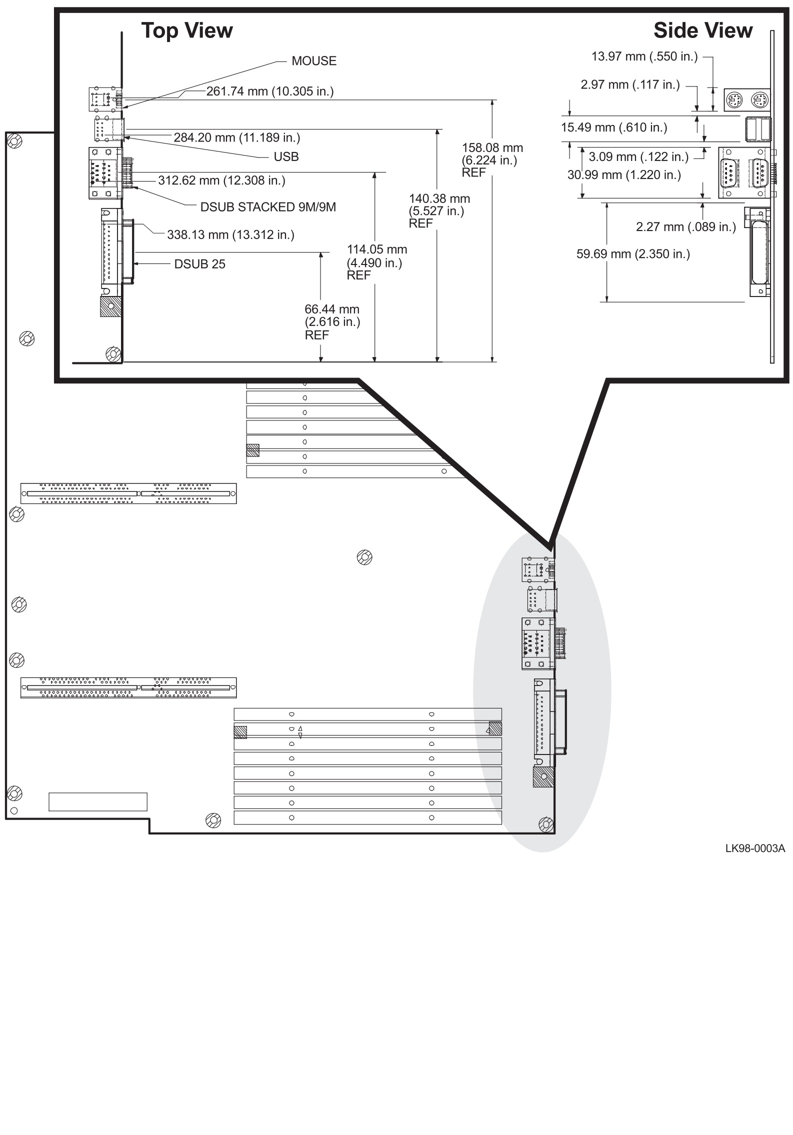
Figure 3–2 AlphaPC 264DP Mainboard Connector Specifications



AlphaPC 264DP Hole and Connector Specifications

Figure 3–3 shows the top and side views of the mainboard's I/O connectors.

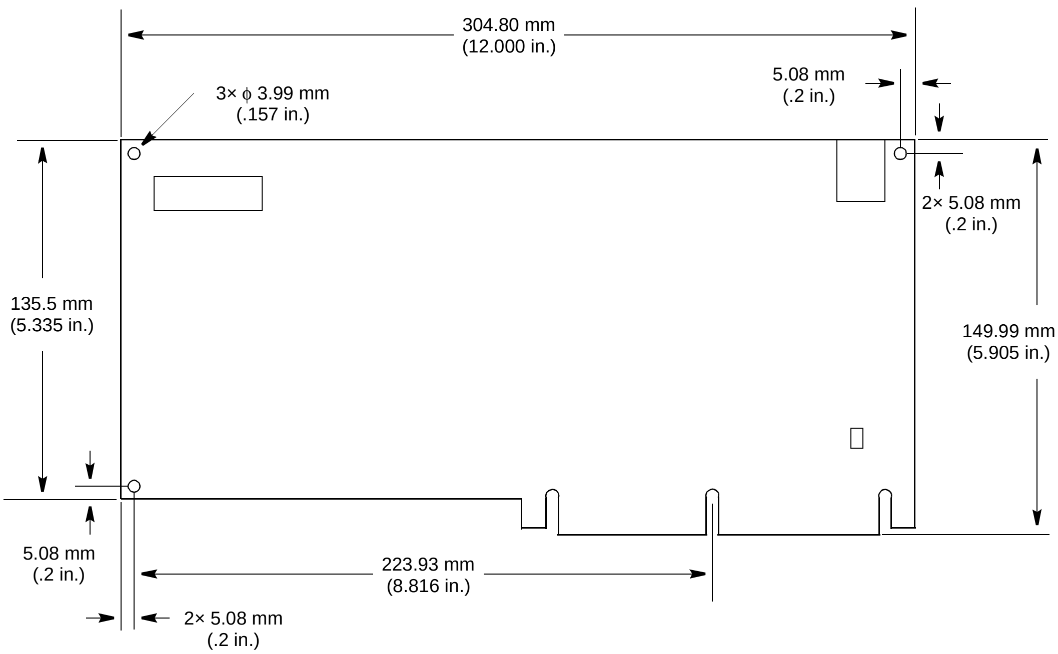
Figure 3–3 AlphaPC 264DP Mainboard I/O Connector Specifications



3.5 AlphaPC 264DP Daughtercard Hole Specification

Figure 3–4 shows the hole specifications for the daughtercard.

Figure 3–4 AlphaPC 264DP Daughtercard Hole Specification—Component Side



4
Functional Description

This chapter describes the functional operation of the AlphaPC 264DP. It introduces the 21272 core logic chipset (21272) and describes its implementation with the 21264 microprocessors and their supporting memory and I/O devices.

Information, such as bus timing and protocol, found in other specifications, data sheets, and reference documentation is not duplicated here.

Note : For detailed descriptions of chipset logic, operations, and transactions, refer to the 21272 chips' specification. For details of the PCI interface, refer to the *PCI System Design Guide* and the *PCI Local Bus Specification*.

4.1 21272 Core Logic Chipset Introduction

The 21272 provides a solution for designers developing uniprocessor or dual-processor systems using the 21264 microprocessor. The chipset provides a 256-bit memory interface and includes the following three gate arrays:

- Cchip: Address and commands, 432-pin ESBGA
- Dchip: Data path, 304-pin ESBGA
- Pchip: PCI interface, 304-pin ESBGA

4.2 Cchip Functional Overview

The Cchip provides the control interface between the 21264 and 21272 chipset. In addition, it provides control for the Dchips and Pchips. It also controls the memory subsystem and TIGbus. The Cchip performs the following functions:

- Maintains queues to store addresses and commands
- Controls and moves data to and from arrays of main memory
- Responds to commands from the CPU
- Supports interrupts and flash ROM via the TIGbus

On the AlphaPC 264DP, the Cchip controls four arrays of SDRAM DIMMs. The DIMMs can range in size from 32MB to 256MB. Note that there are two separate 256-bit paths and four arrays (two on each bus) on the AlphaPC 264DP.

The components of the memory subsystem are distributed between the Cchip and the Dchips. Together, the chips serve as an interface between the CPU and memory subsystem (see Figure 4–1).

The following list summarizes the major features of the Cchip:

- Accepts requests from the Pchip and CPU
- Orders the arriving requests
- Selects the request and issues controls to the DRAMs
- Issues probes to the CPU for the selected requests
- Translates CPU PIO address to PCI and CSR addresses
- Issues commands to the Pchip for the selected request
- Issues responses to the Dchip for the DRAM accesses, the probe, and Pchip responses
- Controls the TIGbus to manage interrupts and maintains CSRs, including those that represent interrupt status

4.2.1 CPU Interface

The CPU and Cchip communicate with each other through the system port. The system port is made up of unidirectional address and command buses. The Cchip system interface logic decodes the sysPort address for both CPU and DMA requests to determine the action to take. It supports cacheable memory accesses, programmed I/O, interrupts, Tig addresses, as well as accesses to 21272 CSR space.

4.2.2 Memory Controller

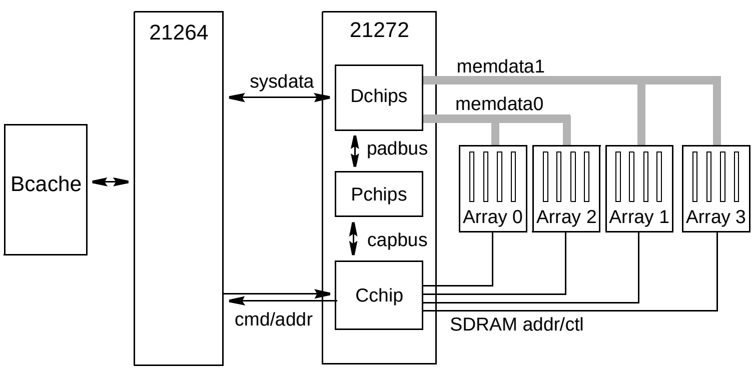
This section summarizes memory organization and memory controller features.

4.2.2.1 Memory Organization

The Cchip supports up to four arrays of SDRAM (Array 0–3), where each array consists of four DIMMs. The AlphaPC 264DP has four 256-bit arrays.

Memory is accessed at 256 bits; however, because the AlphaPC 264DP must use ECC, 288 bits are required. The maximum memory that is supported on the AlphaPC 264DP is 4GB using 256MB DIMMs (16 total).

Figure 4–1 Memory Datapath



4.2.2.2 Programmable Memory Timing

The memory control state machine performs its sequence of steps through all memory transactions. On memory read and write transactions, it communicates with the Dchips so that data may be latched from the memdata bus or driven onto the memdata bus respectively.

4.2.2.3 General-Purpose Logic

The Cchip provides an interface to logic such as presence detection, flash ROM, interrupts, and configuration through the TIGbus. The addresses of these devices and the data are transferred over the TigData lines. The TIGbus interface is implemented using a Quicklogic 2005-1PF FPGA.

4.3 Dchip Functional Overview

This section provides a functional overview of the Dchips and describes the following data bus configurations:

- sysdata bus, between the Dchips and the CPUs
- memdata bus, between the Dchips and the memory arrays
- padbus, between the Dchips and the Pchips

The Dchips provide the data path from the 21264 to main memory. Although a minimum of two chips are required for the memory interface using the 21272, eight chips are used for the interface on the AlphaPC 264DP.

The chips contain the CPU, Pchip, and memory interface data paths, which includes DMA and PIO queues.

The Dchips interface to the CPU using the sysdata bus. It interfaces with each Pchip through the 32-bit padbus (communications path between the Pchip and Dchips, padbus0 to Pchip0 and padbus1 to Pchip1). The Dchips function as the data path for the CPU, memory, and I/O subsystem, and contain the following data path functions:

- DMA write data/PIO read data queue
- DMA read data/PIO write data queue
- Queues to allow full bandwidth transfers from memory to the CPU
- Queue to hold old memory data to be merged with the Pchip data for DMA writes

4.3.1 Sysdata Bus

The sysdata bus, between the Dchips and each CPU, passes 128 bits of data (64 bits [8 bytes] from each CPU). It is connected as follows:

- Dchip 0 connects to each of the two byte 0s.
- Dchip 1 connects to each of the two byte 1s.

  ⋮

- Dchip 7 connects to each of the two byte 7s.

Note: The bytes correspond to the bytes from CPU0 and CPU1.

4.3.2 Memdata Bus

There are two memdata buses, each of which is a 256-bit, bidirectional bus between the Dchips and the memory arrays. Memdata0 connects to arrays 0 and 2; memdata1 connects to arrays 1 and 3 (see Figure 4–1).

Each Dchip sends/receives four bytes of data that it has accumulated to/from the memory arrays. The connections are as follows:

- Dchip0 connects to bytes 0,8,16,24
- Dchip1 connects to bytes 1,9,17,25
- Dchip2 connects to bytes 2,10,18,26
- Dchip3 connects to bytes 3,11,19,27
- Dchip4 connects to bytes 4,12,20,28
- Dchip5 connects to bytes 5,13,21,29
- Dchip6 connects to bytes 6,14,22,30
- Dchip7 connects to bytes 7,15,23,31

4.3.3 Padbus

The padbus is a 32-bit data bus that allows a Pchip and the Dchips to pass data back and forth. If there are two Pchips, then padbus0 (32 bits) connects to Pchip0 and padbus1 (32 bits) connects to Pchip1. The chips are connected in the following manner:

- Dchip0 connects to nibble 0, padbus0 and nibble 0, padbus1.
- Dchip1 connects to nibble 2, padbus0 and nibble 2, padbus1.
- Dchip2 connects to nibble 4, padbus0 and nibble 4, padbus1.
- Dchip3 connects to nibble 6, padbus0 and nibble 6, padbus1.
- Dchip4 connects to nibble 1, padbus0 and nibble 1, padbus1.
- Dchip5 connects to nibble 3, padbus0 and nibble 3, padbus1.
- Dchip6 connects to nibble 5, padbus0 and nibble 5, padbus1.
- Dchip7 connects to nibble 7, padbus0 and nibble 7, padbus1.

4.4 Pchip Functional Overview

The Pchip is the bridge between the PCI and the CPU and its cache and memory, and the chip interface protocol is compliant with the *PCI Local Bus Specification*, Revision 2.1. The Pchip contains all control functions of the bridge and some data path functions. Other data path functions reside in the Dchip.

Two Pchips are used on the AlphaPC 264DP to provide two separate 64-bit PCI buses.

The Pchip provides all controls and interfaces to the PCI and contains the following components and functions:

- Single 64-bit PCI bus implemented at 33 MHz
- PCI central arbiter (disabled on Pchip0)
- DMA write buffer
- Scatter-gather translation lookaside buffer (TLB)
- Downsteam and upstream queues for address and data

4.4.1 PCI Interface

The PCI interface of the Pchip is a fully compliant PCI host bridge. It acts as a master on the PCI on CPU-initiated transactions and is a target on memory space transactions initiated by PCI masters.

The Pchip is not a PCI peripheral; it is a bridge between the PCI peripherals and memory. The chip implements functions of a host bridge that are not sufficient to interface the chip as a PCI peripheral component.

4.5 Clock Subsystem

The system clocks can be divided into five areas:

- Input clocks required by the CPU/system
- Clock forwarding to/from the system logic
- Memory system
- PCI system
- Miscellaneous oscillators and clocks required for the peripheral interfaces and functions

4.5.1 CPU and System Clock Generation

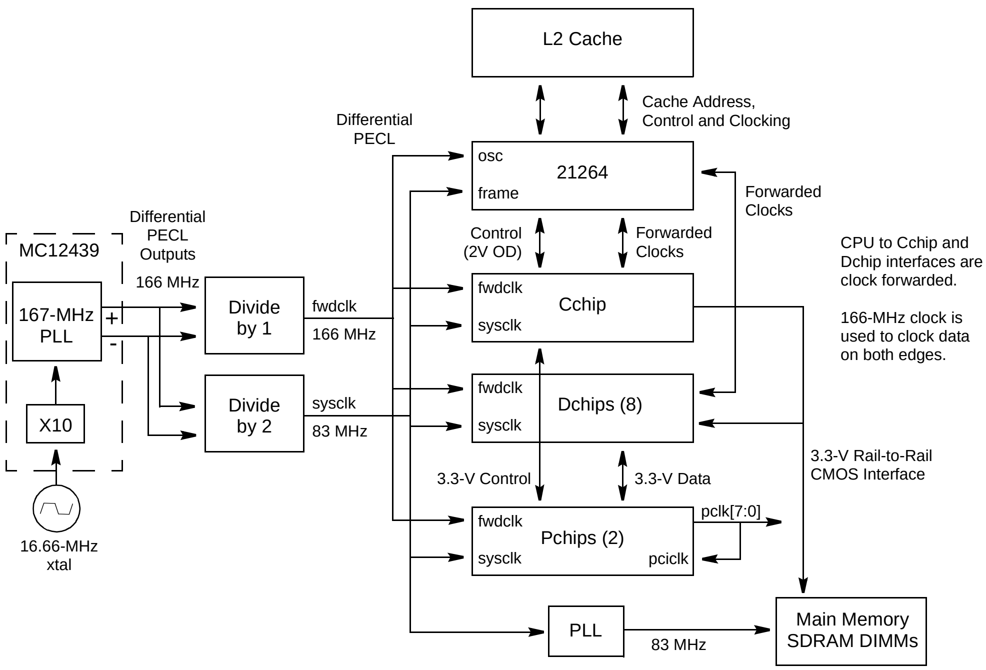
There is a crystal for 32.768 KHz, and other clocks are provided through a PC clock generator chip. A 14.1818-KHz crystal is used as the input clock for the PC clock generator.

A 32.768-KHz crystal provides input to the TOY function of the southbridge.

A 14.3-MHz oscillator (69.9-ns period) output is buffered from the PC clock generator to the host PCI-to-ISA bridge and the three ISA slots. This is the standard 14.31818-MHz ISA clock.

Figure 4–2 shows the clock distribution.

Figure 4–2 Clock Distribution



4.6 PCI Devices

The AlphaPC 264DP uses the PCI bus as the main I/O bus for the majority of peripheral functions. The board implements the ISA bus as an expansion bus for system support functions and peripheral devices.

Table 4–1 shows the IDSEL assignment for all the PCI devices.

Table 4–1 IDSEL Assignments for PCI Devices

Device/PCI Bus Number	IDSEL Assignment
Cypress PCI/ISA /Bus 0	PCI0_AD16
Slot 0/Bus 0	PCI0_AD18
Slot 1/Bus 0	PCI0_AD19
Slot 2/Bus 0	PCI0_AD20
Adaptec PCI/SCSI /Bus 0	PCI0_AD17

Table 4–1 IDSEL Assignments for PCI Devices (Continued)

Device/PCI Bus Number	IDSEL Assignment
Slot 0/Bus 1	PCI1_AD18
Slot 1/Bus 1	PCI1_AD19
Slot 2/Bus 1	PCI1_AD20

4.6.1 PCI0

The PCI0 supports the southbridge chip, three PCI slots, and the SCSI chip.

4.6.1.1 Southbridge Chip

The southbridge provides the bridge between the PCI bus and the Industry Standard Architecture (ISA) bus. The southbridge incorporates the logic for the following:

- A PCI interface (master and slave)
- An ISA interface (master and slave) (see Section 4.8)
- Enhanced 7-channel DMA controller that supports DMA transfers and scatter-gather, and data buffers to isolate the PCI bus from the ISA bus
- An IDE interface, with a maximum cable length of 12 inches
- A 14-level interrupt controller
- A 16-bit BIOS timer
- Three programmable timer counters
- Non-maskable interrupt (NMI) control logic
- Decoding and control for utility bus peripheral devices
- Speaker driver
- PCI arbitration control (disabled on AlphaPC 264DP). Refer to the Cypress hyperCache chipset databook for additional information.

4.6.1.2 PCI0 Expansion Slots

Three PCI bus expansion slots are available on PCI0, with support for 64-bit devices. Note that 3.3 V and +5 V are provided to the appropriate PCI connector pins.

4.6.1.3 PCI SCSI Interface

The Adaptec AIC7895 is used as a bridge from PCI to SCSI. The AIC7895 has two ultra SCSI ports and is packaged in a 208-pin plastic quad flat pack (PQFP). Both ports support ultrawide SCSI devices. Note that parity must be disabled for the SRAM that attaches to the AIC7895.

4.6.2 PCI1

Three PCI bus expansion slots are available on PCI1, with one slot shared with the ISA. All three slots support 64-bit devices. Note that 3.3 V and +5 V are provided to the appropriate PCI connector pins.

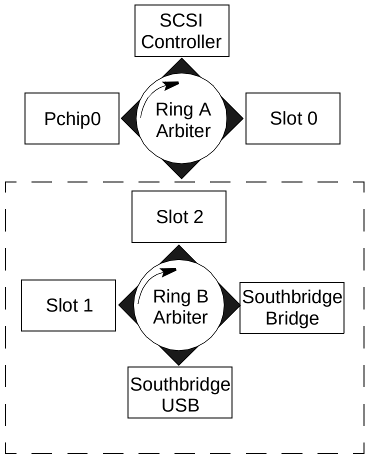
4.6.3 PCI Arbitration

Arbitration logic is implemented in the Pchips, and the scheme is flexible and software programmable. Note, however, that Pchip1 handles the arbitration for PCI1, but the TIGbus FPGA is the arbiter for PCI0. The arbitration logic in the southbridge and in Pchip0 is disabled.

PCI0 Arbitration Scheme

The arbitration is controlled by the TIGbus FPGA, using a dual round-robin priority scheme. There are two rings, A and B, with the scheme shown in Figure 4–3. Ring A has a round-robin priority between Pchip0, SCSI controller, slot 0, and the designated device from ring B. Ring B has a round-robin priority between slot 2, slot 1, the southbridge bridge request, and the southbridge USB request.

Figure 4–3 PCI0 Arbitration Scheme



PCI1 Arbitration Scheme

The arbitration for PCI1 is handled by Pchip1. It is a simple round-robin scheme between slots 0, 1, and 2.

4.7 PCI and System Interrupts

Interrupt logic is implemented in the Cchip and the FPGA. The interrupt lines from the PCI slots, southbridge chip, and SCSI chip are connected directly to the IRQ buffers that reside on the TigData bus. They are driven onto the TigData bus by the encoded TIGADR signals. The AlphaPC 264DP has 34 interrupts that are shown in Figure 4–4.

All PCI interrupts are combined in the Cchip and driven out onto the TIGbus. There is also a Cchip error interrupt and an I/O controller error interrupt within the Cchip.

The CPU interrupt assignment, during normal operation, is listed in Table 4–2.

The Cchip Tig controller polls interrupts continuously except when any other TIG-bus access is requested. The 48 interrupt inputs (34 enabled, 14 reserved) implemented on the AlphaPC 264DP are polled eight at a time by selecting a byte using **tigadr[2:0]** and asserting TigIntOE to allow the selected byte to be driven on the TIGbus. Once all the interrupts are polled, the Cchip drives the **irq[3:0]** data to the two CPUs on to **tigdata[7:0]** and asserts TigIS to strobe it to the flip flop that drives it into the CPU.

PCI and System Interrupts

Figure 4–4 Interrupt Request Register

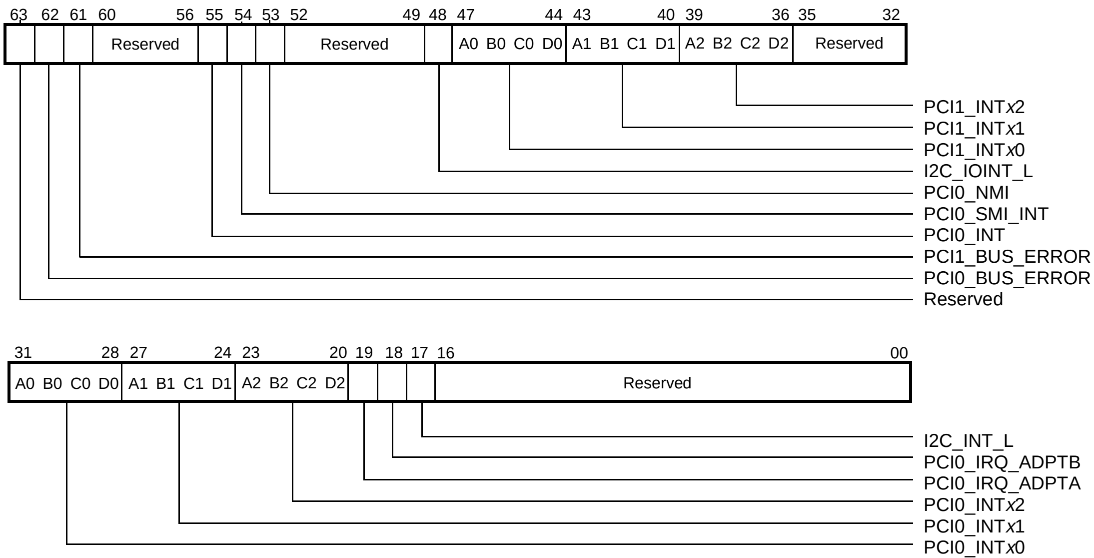


Table 4–2 CPU Interrupt Assignment

CPU Interrupt	Interrupt Souce	Description
cpu_irq0	Pchips	Error interrupts
cpu_irq1	PCI/ISA devices	PCI and ISA interrupts
cpu_irq2	rtc_irq	Real-time clock interrupt
cpu_irq3	c_chip_csr	Interprocessor
cpu_irq4	Halt jumper or software	Halt for each processor
cpu_irq5	Reserved	—

The ISA bus interrupts (IRQ0 through IRQ8 and IRQ12 through IRQ14) are all nested through the southbridge (on INT output) to the Cchip (via the TIGbus) and then into the CPU. The interrupt assignment is configurable but is normally used as shown in Table 4–3.

Table 4–3 ISA Interrupts

Interrupt Level	Interrupt Source	Interrupt Level	Interrupt Source
IRQ0	Interval timer	IRQ8	Reserved
IRQ1	Keyboard	IRQ9	16-bit ISA
IRQ2	Chains interrupt from slave peripheral interrupt controller	IRQ10	16-bit ISA
IRQ3	8-bit ISA (COM2)	IRQ11	16-bit ISA
IRQ4	8-bit ISA (COM1)	IRQ12	Mouse
IRQ5	8-bit ISA (parallel port)	IRQ13	16-bit ISA
IRQ6	8-bit ISA (floppy disk)	IRQ14	16-bit ISA
IRQ7	8-bit ISA (parallel port)	IRQ15	IDE

The AlphaPC 264DP timer interrupt is generated by the real-time clock by means of the square-wave output of the southbridge chip, which routes the interrupt directly to the Cchip.

4.8 ISA Devices

The following section describes the AlphaPC 264DP ISA bus implementation with peripheral devices and connectors.

4.8.1 Super I/O Controller

The AlphaPC 264DP uses the SMC FDC37C669 as the combination controller chip (see Table 2–1 and Figure 2–1). It is packaged in a 100-pin PQFP configuration. The chip provides the following ISA peripheral functions:

- Diskette controller – Software compatible with the Intel PC8477 (contains a superset of the Intel DP8473 and NEC PD765 and the Intel N82077 FDC functions). The onchip analog data separator requires no external filter components and supports the 4Mb drive format and 5.25-inch and 3.5-inch diskette drives. FDC data and control lines are brought out to a standard 34-pin connector. A ribbon cable interfaces the connector to one or two diskette drives.
- Serial ports – Two UARTs with modem control, compatible with NS16450 or PC16550, are brought out to separate onboard, 10-pin connectors. The lines can be brought out through 9-pin female D-sub connectors on the bulkhead of a standard PC enclosure.
- Parallel port – The bidirectional parallel port is brought out to an onboard 25-pin connector. It can be brought out through a 25-pin female D-sub connector on the bulkhead of a standard PC enclosure.

Refer to the SMC FDC37C669 specification for further information (including timing, electrical characteristics, and mechanical data).

4.8.2 ISA Expansion Slot

One ISA expansion slot is provided for plug-in ISA peripherals. This slot is shared with the PCI and can be used for a PCI or ISA device.

4.9 DC Power Distribution

The AlphaPC 264DP derives its system power from a user-supplied power supply. The power supply must provide +12 V dc, –12 V dc, –5 V dc, +5 V dc, 5VSB dc and 3.3 V dc. The dc power is supplied through two power connectors on the mainboard (J3 and J33) and one on the daughtercard (J4). Power is distributed to the board logic through dedicated power planes within the 12-layer board structure. Power is distributed to the daughtercard through the connector and dedicated 18-pin power connector from the power supply.

DC Power Distribution

Figure 4–5 shows that the +12 V dc, –12 V dc, +5 V dc, and –5 V dc are supplied to ISA connector J47. The +12 V dc and –12 V dc are supplied to the PCI connectors J35, J40–42, J44, and J46, and to the two daughtercard connectors J18 and J23. The +12 V dc is also supplied to the fan box connectors J2, J15, J22, and J24.

In addition to the ISA connector, +5.0 V dc is supplied to the PCI connectors and to most of the board's integrated circuits.

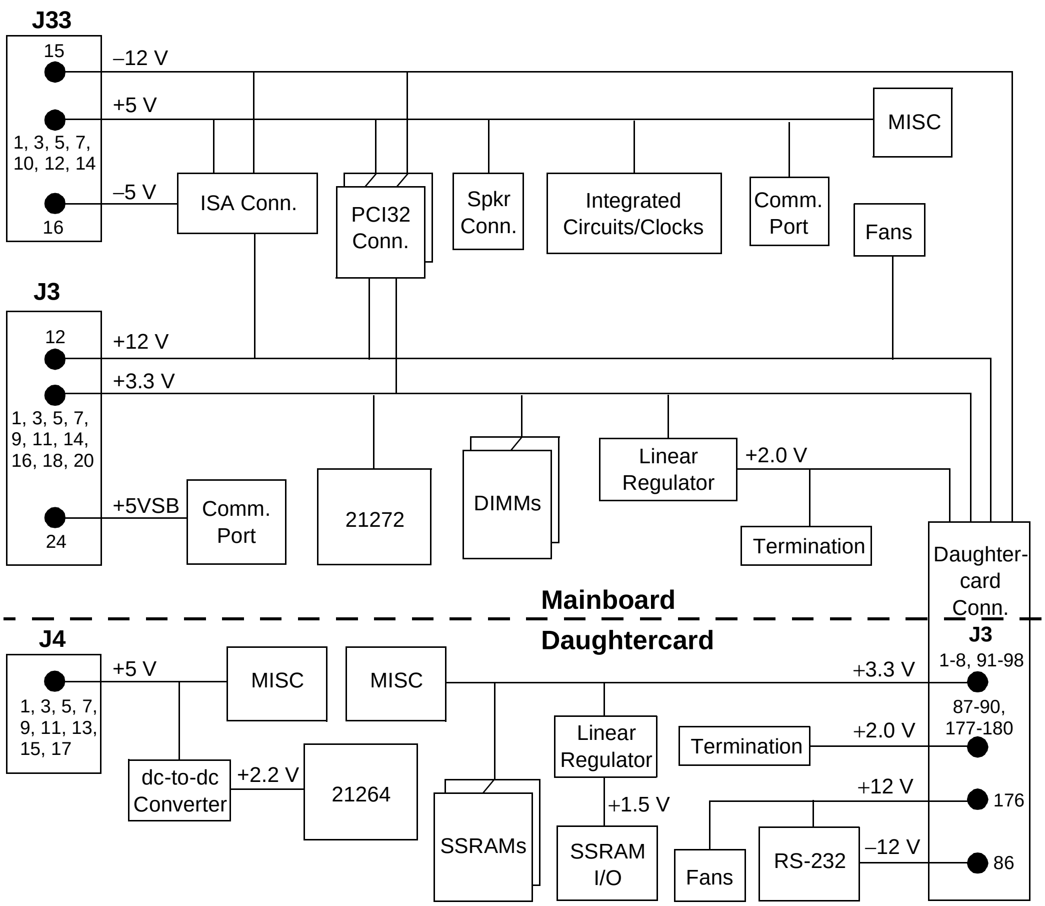
The +3.3 V dc is provided to the PCI slots, the 21272 core logic chipset, the DIMMs, the daughtercard connectors, and the linear regulator that provides the 2.0-V termination voltage to the mainboard and the daughtercard connectors.

The power supply also provides 5 VSB to the comm port (J19) and soft power.

Figure 4–5 also shows that the daughtercard receives +5 V dc from the power supply and distributes it to the dc-to-dc converter and miscellaneous logic on the card. The daughtercard edge connector (J3) provides the following voltages from the mainboard:

- +3.3 V for the SSRAMs, miscellaneous logic on the card, and for the linear regulator for conversion to 1.5 V for SSRAM I/O
- +12 V for fan power and RS-232 logic
- –12 V for RS-232 logic
- +2.0 V for termination logic

Figure 4–5 AlphaPC 264DP Power Distribution



4.10 Reset and Initialization

This logic is contained on the daughtercard in a Quicklogic QL12X16BL FPGA. This controls reset, power OK, SROM test port, and interrupts to the CPU.

The TIGbus FPGA will implement system irq, general configuration registers, and Motorola synthesizer setup based on CPU speed and 21272 speed. It will also provide the interface to the flash ROM.

4.11 System Software

The AlphaPC 264DP software is divided into the following categories:

- Serial ROM code
- Flash ROM code
- Operating systems

4.11.1 Serial ROM Code

The serial ROM code is contained in a 512KB flash ROM. The serial ROM code initializes the system, which includes loading Debug Monitor or other code from the flash ROM. The serial ROM code then transfers control to the code loaded from the flash ROM.

The Mini-Debugger is also resident in the SROM. Switch 4 can be set on SW2 (see Section 2.2) for CPU0 and CPU1 to trap to the Mini-Debugger. Connector J2 on the daughtercard provides a terminal port for the Mini-Debugger.

4.11.2 Flash ROM Code

The AlphaPC 264DP includes an industry-standard, 2MB flash ROM – AMD AM29F016.

4.11.3 Operating Systems

The AlphaPC 264DP is designed to run Windows NT and Tru64 UNIX.

5
System Memory and Address Mapping

5.1 Memory Subsystem

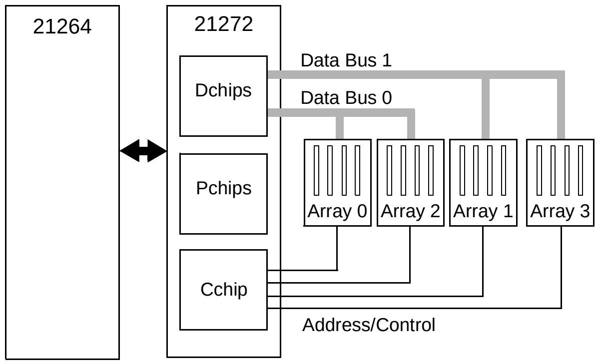
The DRAM memory subsystem on the AlphaPC 264DP consists of sixteen 200-pin buffered DIMM slots, which are organized as four arrays of memory. The 21272 chipset supports two 256-bit memory buses (288-bit including ECC) with two arrays on each bus (see Figure 5–1).

The 72-bit, 100-MHz DIMMs consist of 64 bits of data and 8 bits of ECC, and can be 32MB, 64MB, 128MB, or 256MB. The minimum configuration (one array populated with four 32MB DIMMs) is 128MB. The maximum configuation (four arrays each populated with four 256MB DIMMs) is 4GB.

The memory cycle time is 83 MHz, identical to the 21272 chipset cycle time.

Note: Although the memory cycle time is 83 MHz, qualified 100-MHz DIMMs are required.

Figure 5–1 AlphaPC 264DP Memory Subsystem



5.2 Configuring SDRAM Memory

For the memory system in the AlphaPC 264DP, one to four arrays may be used, following the configuration rules.

Configuration Rules

- Each array must be fully populated with DIMMs of the same size and type.
- Array 0 must be populated.
- Additional arrays can be populated in any order.

  For a memory subsystem with two arrays, placing the second array on bus 1 (array 1 or array 3) is recommended.

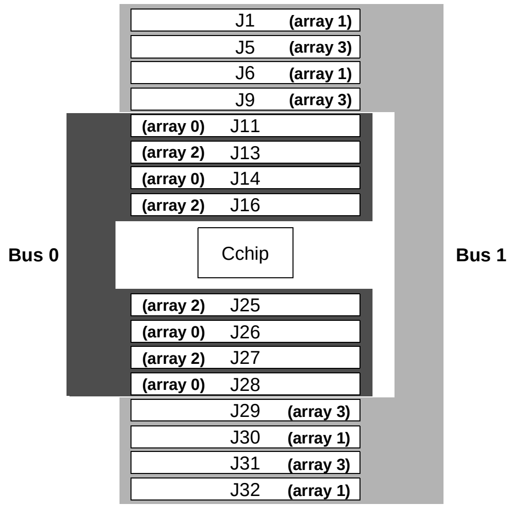
Arrays

The arrays are made up of the following connectors:

- **Array 0**: J11, J14, J26, J28
- **Array 1**: J1, J6, J30, J32
- **Array 2**: J13, J16, J25, J27
- **Array 3**: J5, J9, J29, J31

Figure 5–2 shows the relationship of the connectors/arrays. Refer to Figure 1–1 for DIMM connector locations on the mainboard.

Figure 5–2 AlphaPC 264DP DIMM Connectors



Configuring SDRAM Memory

Possible Configurations

Memory sizes from 128MB to 4GB are supported.

Although not an exhaustive list, Table 5–1 lists some of the SDRAM memory configurations available. Any combinations of DIMMs that meet the configuration rules are supported by the 21272 chipset.

For a list of vendors who supply components and accessories for the AlphaPC 264DP, see Appendix A.

Table 5–1 AlphaPC 264DP SDRAM Memory Configurations

Total Memory	Array 0[1]	Array 1[1]	Array 2[1]	Array 3[1]
128MB	32MB	—	—	—
256MB	32MB	32MB	—	—
	64MB	—	—	—
512MB	128MB	—	—	—
	64MB	64MB	—	—
768MB	128MB	64MB	—	—
	64MB	64MB	64MB	—
1GB	256MB	—	—	—
	128MB	128MB	—	—
	64MB	64MB	64MB	64MB
1.5GB	256MB	128MB	—	—
	128MB	128MB	64MB	64MB
2GB	256MB	256MB	—	—
2.5GB	256MB	256MB	128MB	—
3GB	256MB	256MB	128MB	128MB
3.5GB	256MB	256MB	256MB	128MB
4GB	256MB	256MB	256MB	256MB

[1] Each array has 4 DIMMs.

5.3 System Address Mapping

This section describes the mapping of the processor physical address space into memory and I/O space addresses. It also includes the translations of the processor-initiated address into a PCI address, and PCI-initiated addresses into physical memory addresses.

5.3.1 CPU Address Mapping to PCI Space

The physical sysbus address space is composed of the following:

- Memory address space
- Local I/O space, for registers residing on the sysbus (that is, registers in the Cchip, Dchips, and Pchips)
- PCI space

The PCI defines four physical address spaces, as follows:

- PCI memory space (for memory residing on the PCI)
- PCI I/O space
- PCI configuration space
- PCI interrupt acknowledge cycles /PCI special cycles

Refer to the 21272 functional specification for details in this area.

5.3.2 TIGbus Address Mapping

Table 5–2 shows the address map for the TIGbus.

Table 5–2 TIGbus Address Mapping

capbus [23:21]	Physical Address	Access	Function	Comment
000	801 00xx xxx0 (2MB)	RW	Flash ROM address space	—
001	801 08xx xxx0	RO	Gpen_0 Array0_PD[7:0]	Reserved
010	801 10xx xxx0	RO	Gpen_1 Array1_PD[7:0]	Reserved
011	801 18xx xxx0	RO	Gpen_2 Array2_PD[7:0]	Reserved
100	801 20xx xxx0	RO	Gpen_3 Array3_PD[7:0]	Reserved

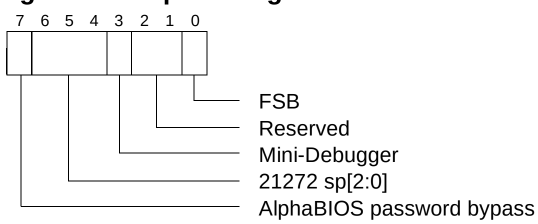
Table 5–2 TIGbus Address Mapping (Continued)

capbus [23:21]	Physical Address	Access	Function	Comment
101	801 28xx xxx0	RO	Gpen_4 Con_bit[7:0]	General configuration register. See Figure 5–3.
110	801 30xx x000	RO	Gpen_5 CPU0_config[7:0]	CPU0 configuration register. See Figure 5–4.
	801 30xx x040	RW	Flash write enable[0]	Writing a 1 to this location enables flash writes.
	801 30xx xA00	RW	Reserved	—
	801 30xx xA40	RW	Reserved	—
	801 30xx x3C0	RW	CPU[1:0] HaltA [1]	Writing a 1 to either bit will halt the specified CPU.
	801 30xx x5C0	RW	CPU[1:0] HaltB [1]	Writing a 1 to either bit will halt the specified CPU.
111	801 38xx x000	RO	Gpen_6 CPU1_config[7:0]	CPU1 configuration register. See Figure 5–5.
	801 38xx x040	RAZ	Reserved	—
	801 38xx x080	WO	PCI_0_ok[0]	PCI0 self-test register.
	801 38xx x0C0	WO	PCI_1_ok[0]	PCI1 self-test register.
	801 38xx x100	RW	Soft_reset[0]	To set a hardware reset for a short period of time, first write a 0, then write a 1 to this location.
	801 38xx x140	RO	Tig_PAL_rev[7:0]	Bits [7:5] specify the major revision (corresponding to the board revision), [4:0] specify the minor revision.
	801 38xx x180	RO	Arbiter_rev[7:0]	Bits [7:5] specify the major revision, [4:0] specify the minor revision.
	801 38xx x1C0	RW	Feature_mask[7:0]	See Figure 5–6.

[1] These are two separate halt registers.

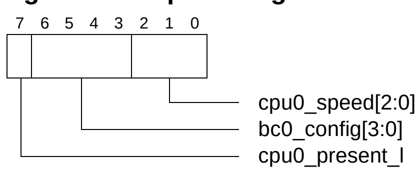
The Gpen4 register, shown in Figure 5–3, reflects the settings of the mainboard's switchpack 2 (see Figure 2–3).

Figure 5–3 Gpen4 Register



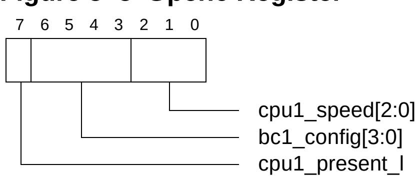
The Gpen5 register, shown in Figure 5–4, shows the CPU speed and Bcache configuration (set by onboard resistors) on the daughtercard containing CPU0.

Figure 5–4 Gpen5 Register



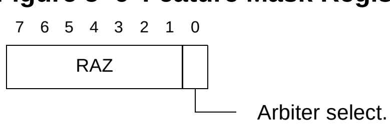
The Gpen6 register, shown in Figure 5–5, shows the CPU speed and Bcache configuration (set by onboard resistors) on the daughtercard containing CPU1.

Figure 5–5 Gpen6 Register



The feature mask register, shown in Figure 5–6, allows you to set the Cypress chip's arbiter activity.

Figure 5–6 Feature Mask Register



0	Selects the arbiter that deasserts the Cypress chip's grant after it claims the transaction.
1	Selects the arbiter that holds the assertion of the Cypress chip's grant until it has deasserted its request.

A

Support, Products, and Documentation

A.1 Customer Support

Alpha OEM provides the following web page resources for customer support.

URL	Description
http://www.digital.com/alphaoem	Contains the following links: • **Developers' Area:** Development tools, code examples, driver developers' information, and technical white papers • **Motherboard Products:** Motherboard details and performance information • **Microprocessor Products:** Microprocessor details and performance information • **News:** Press releases • **Technical Information:** Motherboard firmware and drivers, hardware compatibility lists, and product documentation library • **Customer Support:** Feedback form

A.2 Supporting Products

This section lists sources for components and accessories that are not included with the AlphaPC 264DP.

A.2.1 Memory

Dual inline memory modules (DIMMs) are available from a variety of vendors. For a list of the qualified vendors, visit the Alpha OEM World Wide Web Internet site at URL:

http://www.digital.com/alphaoem

Click on **Technical Information**.
Then click on **Alpha OEM Hardware Compatibility List**.

A.2.2 Power Supply

A power supply, suitable for use with the AlphaPC 264DP (+3.3 V, +5 V, –5 V, +12 V, –12 V), is available from:

Antec, Inc.

2859 Bayview Drive
Fremont, CA 94538
Phone: 510–770–1200, ext. 312
PN PRS-618 (630 W)

A.2.3 Enclosure

An enclosure, suitable for housing the AlphaPC 264DP and its power supply, is available from:

Delta Axxion Technology

1550 Northwestern
El Paso, TX 79912
Phone: 915–877–5288
PN TL-22

A.3 Alpha Products

To order the AlphaPC 264DP mainboard, contact your local sales office. The following tables list some of the Alpha products available.

Note: The following products and order numbers might have been revised. For the latest versions, contact your local sales office.

Chips	Order Number
Alpha 21264 microprocessor (500 MHz)	21264–A1

Motherboard kits include the mainboard and user's manual.

Motherboard Kits	Order Number
AlphaPC 264DP Dual Processor Planar Board	21A06–B0
AlphaPC 264DP 500-MHz CPU Board with 2MB Cache	21A06–M0
AlphaPC 264DP 500-MHz CPU Board with 4MB Cache	21A06–M1

Design kits include documentation and schematics. They do not include related hardware.

Design Kits	Order Number
Alpha Motherboards Software Developer's Kit	QR–21B02–04

A.4 Alpha Documentation

The following table lists some of the available Alpha documentation. You can download Alpha documentation from the Alpha OEM World Wide Web Internet site:

http://www.digital.com/alphaoem

Click on **Technical Information**, then click on **Documentation Library**.

Title	Order Number
Alpha Architecture Reference Manual[1]	EY–W938E–DP
Alpha Architecture Handbook	EC–QD2KB–TE
Alpha 21264 Microprocessor Hardware Specification	DS–0013C–TE

[1]To purchase the *Alpha Architecture Reference Manual*, contact your local sales office or call Butterworth-Heinemann (DIGITAL Press) at 1–800–366–2665.

A.5 Third–Party Documentation

You can order the following third-party documentation directly from the vendor.

Title	Vendor
PCI Local Bus Specification, Revision 2.1 PCI Multimedia Design Guide, Revision 1.0 PCI System Design Guide PCI-to-PCI Bridge Architecture Specification, Revision 1.0 PCI BIOS Specification, Revision 2.1	PCI Special Interest Group U.S. 1–800–433–5177 International 1–503–797–4207 Fax 1–503–234–6762
CY82C693UB hyperCache/Stand-Alone PCI Peripheral Controller with USB Data Sheet	Cypress Semiconductor Corporation 3901 North First Street San Jose, CA 95134 Phone: 1–800–858–1810
Super I/O Floppy Disk Controller with Infrared Support (FDC37C669) Data Sheet	Standard Microsystems Corporation 80 Arkay Drive Hauppauge, NY 11788 Phone: 1–800–443–7364 Fax: 1–516–231–6004

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