Release Notes

MT25208 InfiniHost III Ex Firmware

(MemFree)

FW-25218 Rev 5.0.1

MT25208 InfiniHost III Ex Firmware FW-25218 Release Notes

Document Number:

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1 Overview

This document summarizes the contents of Rev 5.0.1 release of MT25208 InfiniHost III Ex Firmware FW-25218 (MemFree).

The document consists of the following sections:

2 InfiniHost III Ex HCA Boards Supported

This FW-25218 firmware can be burnt onto the following HCA boards:

- MHEL-CFXXX-T[1] - Lion Cub (Previous PN: MTLP25208)
- MHEA28-XT - Lion Mini (MemFree)

Notes:

1. Each board has its own *Board Definition file* (.brd file) which must be used for the burning process.
2. After burning the Lion Cub board, a complete shutdown of the machine is required before the new firmware can take effect.

1. XXX stand for the size of attached DDR DRAM in MB: 128, 256, or 512

3 Known Issues

The following table describes known issues in this firmware release and possible workarounds.

Table 1 - Known Issues

Index	Issue	Description	Current Implemented Workaround in FW	Possible Workaround	Patch Release (fix)	Scheduled Release (fix)
1.	MSIx vectors	Writing to MSIx vectors (Address/Data/Mask) does not take immediate effect. There may be MSIx messages that leave the device according to the old vector.	NA	NA	NA	NA
2.	QPC.Flight_LIM	QPC field – no HW limit, infinite WQEs on send.	NA	NA	NA	NA
3.	QUERY_DDR	Query does not return JEDEC vendor ID yet. Scope of status is limited to active / not active.	NA	NA	NA	NA
4.	RTR2RTS_QPEE; SQD2RTS_QPEE: changing optional fields rra_max and ra_buf_index is not supported.	The optional fields rra_max and ra_buf_index are not supported in the RTR2RTS_QPEE and SQD2TRS_QPEE commands.	Change requests for these fields will not take effect, and no error indication is provided.	Mask these optional fields.	NA	NA
5.	PCI 2.3 control and status - for interrupts	InfiniHost III Ex does not support PCI2.3 control and status bits for interrupts.	NA	NA	NA	NA
6.	Change of memory bars on a disabled system	Changing memory bars size / addresses between SYS_DIS and SYS_EN may cause the InfiniHost III Ex to hang (ID: 24206)	NA	NA	NA	NA
7.	BAR resizing on an enabled system	Changing bar sizes when a system is enabled may cause the InfiniHost III Ex to hang (ID: 24208).	NA	NA	NA	NA
8.	SW reset via configuration cycles	SW reset via config cycles may create double PCI- Express completions for the configuration transaction.	NA	If InfiniHost III Ex boots in memory controller mode, perform power cycle / hot reset after restoring the flash.	NA	NA
9.	SW reset is performed during a configuration transaction	If SW reset is performed while a configuration transaction is outstanding, it may create double PCI- Express completions for the configuration transaction.	NA	Do not perform SW reset during configuration cycles.	NA	NA
10.	Flash CRC error	InfiniHost III Ex fails to report a Flash CRC error as required by the Flash Burning Application Notes	NA	NA	NA	NA

Table 1 - Known Issues (Continued)

Index	Issue	Description	Current Implemented Workaround in FW	Possible Workaround	Patch Release (fix)	Scheduled Release (fix)
11.	MADs:PortInfo Get()	When querying for information about an InfiniHost III Ex IB port via its other IB port, the wrong Local port number is returned. Instead of the number of the second port, the one which received the MAD packets, the number of the first port is being returned. (ID: 24177)	NA	NA	NA	NA
12.	Change of Link Width via infiniburn (IB_TAB)	Change of Link Width via infiniburn (IB_TAB) does not take effect. (ID: 24211)	NA	NA	NA	NA
13.	A Concurrent Bind and Deallocate for the same Memory Window will prevent closing the Memory Region of this Window	Bind and Deallocate modify the same 'unprotected' variable of the Memory Region. If both operations are attempted simultaneously for the same Memory Window, the variable does not get updated correctly. This prevents closing the Memory Region as the corrupted variable value may indicate that a Memory Window is still bound to it.	NA	Avoid simultaneous Bind and Deallocate operations for the same Memory Window.	NA	Next Release

3.1 Unsupported *InfiniHost III Programmer's Reference Manual* (Device-ID 25218) Changes

The following features of the *InfiniHost III Programmer's Reference Manual, Document no. 2248PM*, are not scheduled to be supported:

1. Flight lim value in QPC may show a value other than 0'1111 even when set for unlimited usage.

Appendix: InfiniHost III Ex FW parameters with "refnames"

This appendix lists all InfiniHost III Ex FW parameters settable in the Board Definition file used by the MST tool **infiniburn**. For details, please refer to *MST User's Manual, Document #2125SM*.

```
-------
PARAM:   "Adapter Vendor ID":
REFNAME: "adapter_vendor_id":
Adapter Vendor ID reported to QUERY_ADAPTER query by Driver

refname: adapter_vendor_id

-------
PARAM:   "Adapter Device ID":
REFNAME: "adapter_dev_id":
Adapter Device ID reported to QUERY_ADAPTER query by Driver

refname: adapter_dev_id

-------
PARAM:   "Adapter Revision ID":
REFNAME: "adapter_rev_id":
Adapter Revision ID reported to QUERY_ADAPTER query by Driver

refname: adapter_rev_id

-------
PARAM:   "Adapter VSD":
REFNAME: "adapter_vsd":
Vendor Specific Data on flash

refname: adapter_vsd

-------
PARAM:   "PSID":
REFNAME: "PSID":
Parameter Set IDentification

refname: PSID

-------
PARAM:   "INTA# Pin ID":
REFNAME: "INTA":
Device GPIO pin number which is connected
to INTA# on the adapter. If INTO# pin is
```

```
connected to INTA#, set value to 63.

refname: INTA

-------
PARAM:   "SERR":
REFNAME: "report_catastrophic_error_serr":
Enables/Disables the pulling of SERR
interrupt pin upon catastrophic error.

refname: report_catastrophic_error_serr

-------
PARAM:   "INTO":
REFNAME: "report_catastrophic_error_into":
Enables/Disables the pulling of INTO
interrupt pin upon catastrophic error.

refname: report_catastrophic_error_into

-------
PARAM:   "INTB":
REFNAME: "report_catastrophic_error_intb":
Enables/Disables the pulling of INTB
interrupt pin upon catastrophic error.

refname: report_catastrophic_error_intb

-------
PARAM:   "SERR":
REFNAME: "unreport_catastrophic_error_serr":
Enables/Disables the pulling of SERR
interrupt pin upon catastrophic error.

refname: unreport_catastrophic_error_serr

-------
PARAM:   "INTO":
REFNAME: "unreport_catastrophic_error_into":
Enables/Disables the pulling of INTO
interrupt pin upon catastrophic error.

refname: unreport_catastrophic_error_into

-------
PARAM:   "INTB":
REFNAME: "unreport_catastrophic_error_intb":
Enables/Disables the pulling of INTB
```

```
interrupt pin upon catastrophic error.

refname: unreport_catastrophic_error_intb

-------
PARAM:   "Interrupt Coalescing Delay":
REFNAME: "int_coalsing_delay":
Min delay between two consecutive interrupts generated by HCA (in clock units)

refname: int_coalsing_delay

-------
PARAM:   "Expansion ROM Enable":
REFNAME: "exp_rom_en":
Enable Expansion ROM BAR.

refname: exp_rom_en

-------
PARAM:   "VPD Enable":
REFNAME: "vpd_enable":
Disable/enable the VPD support

refname: vpd_enable

-------
PARAM:   "VPD size":
REFNAME: "vpd_size":
VPD size in bytes.

refname: vpd_size

-------
PARAM:   "Log2 VPD EEPROM size":
REFNAME: "log2_vpd_eeprom_size":
size of each one of EEPROM slaves of the VPD

refname: log2_vpd_eeprom_size

-------
PARAM:   "Num of VPD EEPROMs":
REFNAME: "vpd_num_of_eeproms":
number of EEPROM slaves that contain the VPD

refname: vpd_num_of_eeproms

-------
PARAM:   "VPD EEPROM addr":
REFNAME: "vpd_address":
i2c slave address of EEPROM. (first EEPROM if there are multiple addresses.
Other EEPROM's i2c addresses are successive.
```

```
refname: vpd_address

-------
PARAM:   "VPD EEPROM offset":
REFNAME: "vpd_offset":
 offset in EEPROM.

refname: vpd_offset

-------
PARAM:   "VPD i2c width 16 bits":
REFNAME: "vpd_i2c_16bit":
i2c bit width is 16 bits (rather than 8 bits)

refname: vpd_i2c_16bit

-------
PARAM:   "Slot Clock Configuration":
REFNAME: "slot_clock_cfg":
PCI Express Link Status Register. Slot Clock Configuration.
This bit indicates that the component uses the same physical reference clock
that the platform provides on the connector.
If the device uses an independent clock irrespective of the presence
of a reference on the connector, this bit must be clear.

refname: slot_clock_cfg

-------
PARAM:   "HCA Vendor ID":
REFNAME: "hca_header_vendor_id":
Mellanox HCA Vendor ID reported
to system sweep process.

refname: hca_header_vendor_id

-------
PARAM:   "HCA Device ID":
REFNAME: "hca_header_device_id":
Mellanox InfiniHost Device ID
reported to system sweep process.

refname: hca_header_device_id

-------
PARAM:   "HCA Revision ID":
REFNAME: "hca_rev_id":
Mellanox InfiniHost Revision ID
reported to system sweep process.

refname: hca_rev_id
```

```
-------
PARAM:   "SubSystem Vendor ID":
REFNAME: "hca_header_subsystem_vendor_id":
Mellanox subsystem HCA Vendor ID
reported to system sweep process.

refname: hca_header_subsystem_vendor_id

-------
PARAM:   "SubSystem Device ID":
REFNAME: "hca_header_subsystem_id":
Mellanox subsystem HCA ID
reported to system sweep process.

refname: hca_header_subsystem_id

-------
PARAM:   "Power Management Capability Enable":
REFNAME: "pci_power_management_en":
Enable PCI Power Management Capability.
Required for PCI Express compliance.

refname: pci_power_management_en

-------
PARAM:   "Vendor Key [31:0]":
REFNAME: "v_key_31_0":
Vendor Key [31:0]

refname: v_key_31_0

-------
PARAM:   "Vendor Key [31:0]":
REFNAME: "v_key_63_32":
Vendor Key [63:32]

refname: v_key_63_32

-------
PARAM:   "MSI Capability Enable":
REFNAME: "msi_en":
Enable MSI Capability.
Support for this capability, or MSI-X capability is required for PCI Express
compliance.

refname: msi_en
```

```
-------
PARAM:   "MSI-X Capability Enable":
REFNAME: "msi_x_en":
Enable MSI-X Capability.
Support for this capability, or MSI capability is required for PCI Express com-
pliance.

refname: msi_x_en

-------
PARAM:   "Advanced Error Reporting Capability Enable":
REFNAME: "advanced_error_reporting_en":
Enable PCI Express Advanced Error Reporting Capability.
This capability resides in PCI Express Extended Configuration Space.

refname: advanced_error_reporting_en

-------
PARAM:   "PCI Express Capability Enable":
REFNAME: "pci_express_en":
Enable PCI Express Capability.
Required for PCI Express compatibility.

refname: pci_express_en

-------
PARAM:   "Default Max Read Request Size":
REFNAME: "default_max_read_request_size":
Default value for Max_Read_Request_Size field
in the PCI Express Capability Device Control Register.
Set to 0x2 for strict PCI Express compatibility.

 14:12 Max_Read_Request_Size .
 This field sets the maximum Read Request size for the Device as a Requester.
 The Device must not generate read requests with size exceeding the set value.
 Defined encodings for this field are:
 000b 128 bytes max read request size
 001b 256 bytes max read request size
 010b 512 bytes max read request size
 011b 1024 bytes max read request size
 100b 2048 bytes max read request size
 101b 4096 bytes max read request size
 110b Reserved
 111b Reserved
 Devices that do not generate Read Request larger than 128
 bytes are permitted to implement this field as Read Only (ro="1")
 with a value of 000b.
 Default value of this field is 010b
```

```
refname: default_max_read_request_size

-------
PARAM:   "Log2 Max Read Request Size (in byte)":
REFNAME: "emt_max_outstanding_read_request_size":
Log2 of Max Read Request Size.
10 - 1Kb
11 - 2Kb
12 - 4Kb

Using larger value here will limit the number of HW engines
in use.

refname: emt_max_outstanding_read_request_size

-------
PARAM:   "Max Outstanding Read Requests":
REFNAME: "emt_max_outstanding_read_requests":
Limits the max number of outstanding read requests.

refname: emt_max_outstanding_read_requests

-------
PARAM:   "Log2 UAR Size (in pages)":
REFNAME: "db_area_size":
Log2 of Maximum Number of UARs
to be used to access the device.

refname: db_area_size

-------
PARAM:   "Log2 of System Page Size (in bytes)":
REFNAME: "page_size":
Log2 of System Page Size.

refname: page_size

-------
PARAM:   "TPT Map":
REFNAME: "tpt_cfg_xlcache_conf":
Determines the indexing method of the TPT
translation cache entries.

refname: tpt_cfg_xlcache_conf

-------
PARAM:   "SRQ enable ":
```

```
REFNAME: "srq_enable":
Disable/enable the SRQ support.

refname: srq_enable

-------
PARAM:   "Log max SRQ":
REFNAME: "log_max_srqs":
Log 2 max SRQ supported

refname: log_max_srqs

-------
PARAM:   "IEEE Vendor ID":
REFNAME: "nodeinfo_vendor_id":
Mellanox IB Vendor ID.
A part of the Node Information that may be queried
by the Subnet Manager (SM)

refname: nodeinfo_vendor_id

-------
PARAM:   "Device ID":
REFNAME: "nodeinfo_ib_dev":
Mellanox IB Device ID.
A part of the Node Information that may be
queried by the Subnet Manager (SM)

refname: nodeinfo_ib_dev

-------
PARAM:   "Revision ID":
REFNAME: "nodeinfo_ibrev_id":
HW Revision ID.
A part of the Node Information that may be queried
by the Subnet Manager (SM)

refname: nodeinfo_ibrev_id

-------
PARAM:   "Base Version":
REFNAME: "nodeinfo_base_ver":
Supported MAD Base Version.
A part of the Node Information that may be
queried by the Subnet Manager (SM).

refname: nodeinfo_base_ver
```

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-------
PARAM:   "Class Version":
REFNAME: "nodeinfo_class_ver":
Supported Subnet Management Class Version.
A part of the Node Information that may be
queried by the Subnet Manager (SM).

refname: nodeinfo_class_ver

-------
PARAM:   "Node Type":
REFNAME: "nodeinfo_node_type":

IB Node type.
A part of the Node Information that may be queried
by the Subnet Manager (SM).

refname: nodeinfo_node_type

-------
PARAM:   "Num of Ports":
REFNAME: "nodeinfo_num_ports":
Number of operating ports.

refname: nodeinfo_num_ports

-------
PARAM:   "Log2 Partition Capability":
REFNAME: "nodeinfo_log_partition_cap":
Log 2 of Partition Table size supported by each port.
Maximum number of entries per port in InfiniHost is 64.

refname: nodeinfo_log_partition_cap

-------
PARAM:   "DD":
REFNAME: "DD":


refname: DD

-------
PARAM:   "MM":
REFNAME: "MM":


refname: MM
```

```
-------
PARAM:   "YY":
REFNAME: "YY":


refname: YY

-------
PARAM:   "-":
REFNAME: "NUM":


refname: NUM

-------
PARAM:   "Node GUID [39:32]":
REFNAME: "nodeguid_39_32":
Bits [39:32] of Mellanox HCA Node GUID
Part of the Node information that may be queried
by the Subnet Manager (SM).

refname: nodeguid_39_32

-------
PARAM:   "SystemImageGUID [39:32]":
REFNAME: "systemimageguid_39_32":
Bits [39:32] of SystemImageGUID of NodeInfo.
Enables system software to indicate the availability of
multiple paths to the same destination via multiple nodes.
Set to zero if indication of node association is not desired.

refname: systemimageguid_39_32

-------
PARAM:   "SystemImageGUID [31:0]":
REFNAME: "systemimageguid_31_0":
Lower 32 bits of SystemImageGUID of NodeInfo.
Enables system software to indicate the availability of
multiple paths to the same destination via multiple nodes.
Set to zero if indication of node association is not desired.

refname: systemimageguid_31_0

-------
PARAM:   "Node Description":
REFNAME: "node_desc":
Mellanox InfiniHost node description.
A part of the NodeDescription that may be queried
```

```
by the Subnet Manager (SM).

refname: node_desc

-------
PARAM:   "Number of Enabled Ports":
REFNAME: "num_of_ports":
Enable or Disable the InfiniHost Ports.
The Node information given by the Device
reflects port availability.

refname: num_of_ports

-------
PARAM:   "Ports Width Capability":
REFNAME: "ports_link_width_max":

PortWidth supported as defined by IB spec.
Ports may be opened as supporting either 1x, 4x or both.

refname: ports_link_width_max

-------
PARAM:   "Port1 GUID [39:32]":
REFNAME: "port1guid_39_32":
Bits [39:32] of Port Guid parameter.
The PortGUID is the first entry in the GUID table,
which may be queried by the Subnet Manager (SM).

refname: port1guid_39_32

-------
PARAM:   "Port2 GUID [39:32]":
REFNAME: "port2guid_39_32":
Bits [39:32] of Port Guid parameter.
The PortGUID is the first entry in the GUID table,
which may be queried by the Subnet Manager (SM).

refname: port2guid_39_32

-------
PARAM:   "Port1 GUID [31:0]":
REFNAME: "port1guid_31_0":
LSbits of Port Guid parameter.
Port GUID value for each port. The PortGUID is the first
entry in the GUID table, that may be queried by the Subnet Manager (SM).

refname: port1guid_31_0
```

```
-------
PARAM:   "Port2 GUID [31:0]":
REFNAME: "port2guid_31_0":
LSbits of Port Guid parameter.
Port GUID value for each port. The PortGUID is the first
entry in the GUID table, that may be queried by the Subnet Manager (SM).

refname: port2guid_31_0

-------
PARAM:   "Tx Lane Polarity":
REFNAME: "tx_lane_polarity_port1":
When set, the serial input data on lane X on this port
will be inverted. This is equivalent to flipping the
differential input of the SERDES.
Each bit relates to Lane X where X=0,1,2,3.

refname: tx_lane_polarity_port1

-------
PARAM:   "Tx Lane Polarity":
REFNAME: "tx_lane_polarity_port2":
When set, the serial input data on lane X on this port
will be inverted. This is equivalent to flipping the
differential input of the SERDES.
Each bit relates to Lane X where X=0,1,2,3.

refname: tx_lane_polarity_port2

-------
PARAM:   "Phy LED GPIO":
REFNAME: "port1_phy_led_gpio":
0-0xff : GPIO number connected to the LED
indicating physical/logical state of the port.
NOTE: if Self-Refresh is enabled, GPIO13 and
GPIO8 cannot be used.

refname: port1_phy_led_gpio

-------
PARAM:   "Phy LED GPIO":
REFNAME: "port2_phy_led_gpio":
0-0xff : GPIO number connected to the LED
indicating physical/logical state of the port
NOTE: if Self-Refresh is enabled, GPIO13 and
GPIO8 cannot be used.
```

```
refname: port2_phy_led_gpio

-------
PARAM:   "Log LED GPIO":
REFNAME: "port1_log_led_gpio":
0-0xff : GPIO number connected to the LED
indicating physical/logical state of the port
NOTE: if Self-Refresh is enabled, GPIO13 and
GPIO8 cannot be used.

refname: port1_log_led_gpio

-------
PARAM:   "Log LED GPIO":
REFNAME: "port2_log_led_gpio":
0-0xff : GPIO number connected to the LED
indicating physical/logical state of the port
NOTE: if Self-Refresh is enabled, GPIO13 and
GPIO8 cannot be used.

refname: port2_log_led_gpio

-------
PARAM:   "Disable LEDS blinking":
REFNAME: "disable_leds_blink":


refname: disable_leds_blink

-------
PARAM:   "E1 Clock Divider":
REFNAME: "flash_i2c_clk":
e1clk divider to read pll boot record

refname: flash_i2c_clk

-------
PARAM:   "Core N":
REFNAME: "core_n":
pll divider. i1clk will be e1clk * (m/2n)
1N8
0000 = 8

refname: core_n

-------
PARAM:   "Core M":
REFNAME: "core_m":
```

```
1M16
0000 = 16

refname: core_m

-------
PARAM:   "VCO Range":
REFNAME: "core_vco_range":
if i1clk>=133mhz, vco_range should be '1' (pll input)

refname: core_vco_range

-------
PARAM:   "Bypass":
REFNAME: "core_bypass":
pll bypass. not usable here. we use the input pad

refname: core_bypass

-------
PARAM:   "Lock enable":
REFNAME: "core_lock":


refname: core_lock

-------
PARAM:   "Output enable":
REFNAME: "core_eout":


refname: core_eout

-------
PARAM:   "DMU N":
REFNAME: "dmu_n":
1N8
0000 = 8
pll divider. d1clk will be (1+dmu_deskew) * mclkin * (m/(2-dddso)n) ..... dddso
= disable_dmu_divider strapping option

refname: dmu_n

-------
PARAM:   "DMU M":
REFNAME: "dmu_m":
1M16
0000 = 16
```

```
refname: dmu_m

-------
PARAM:   "VCO Range":
REFNAME: "dmu_vco_range":
if d1clk*2>=133mhz, vco_range should be '1' (pll input)

refname: dmu_vco_range

-------
PARAM:   "Deskew":
REFNAME: "dmu_deskew":
deskew option to the pll

refname: dmu_deskew

-------
PARAM:   "Bypass":
REFNAME: "dmu_bypass":
pll bypass. not usable here. we use the input pad

refname: dmu_bypass

-------
PARAM:   "Lock enable":
REFNAME: "dmu_lock":


refname: dmu_lock

-------
PARAM:   "Output enable":
REFNAME: "dmu_eout":


refname: dmu_eout

-------
PARAM:   "RSU Common":
REFNAME: "r0_rsu_common":
put 0x0. mode of pll for ib clk.

refname: r0_rsu_common

-------
PARAM:   "Nref":
REFNAME: "r0_nref":
```

```
put 0x0. ask smeloy if u want...

refname: r0_nref

-------
PARAM:   "PFD":
REFNAME: "r0_pfd":
put 0x0. ask smeloy if u want...

refname: r0_pfd

-------
PARAM:   "LDIV":
REFNAME: "r0_ldiv":
IB clock divider, for VRCLKP/N pin.
for serdes at 2.5Ghz ,the following frequences are allowed for VRCLKP/N input:
if input 125MHz put 0x0,
         250Mhz put 0x1,
         62.5MHz put 0x2,
     for 31.25MHz put 0x3,
       for 100MHz put 0x4-0x7 (e.g. TGU is 100MHz, put 0x7)

refname: r0_ldiv

-------
PARAM:   "Bypass":
REFNAME: "r0_bypass":
pll bypass. not usable here. we use the input pad

refname: r0_bypass

-------
PARAM:   "Lock":
REFNAME: "r0_lock":
enable pll lock indication (enable to push it on the pad)

refname: r0_lock

-------
PARAM:   "Out":
REFNAME: "r0_eout":
enable the clock_out on the pad (refclk/2)

refname: r0_eout

-------
PARAM:   "RSU Common":
REFNAME: "t0_rsu_common":
```

```
put 0x0. mode of pll for ib clk.

refname: t0_rsu_common

-------
PARAM:   "Nref":
REFNAME: "t0_nref":
put 0x0. ask smeloy if u want...

refname: t0_nref

-------
PARAM:   "PFD":
REFNAME: "t0_pfd":
put 0x0. ask smeloy if u want...

refname: t0_pfd

-------
PARAM:   "LDIV":
REFNAME: "t0_ldiv":
PCI Express clock divider, for XRCLKP/N.
for serdes at 2.5Ghz ,the following frequences are allowed for XRCLKP/N input:
if input 125MHz put 0x0,
         250Mhz put 0x1,
         62.5MHz put 0x2,
     for 31.25MHz put 0x3,
       for 100MHz put 0x4-0x7 (e.g. TGU is 100MHz, put 0x7)

refname: t0_ldiv

-------
PARAM:   "Bypass":
REFNAME: "t0_bypass":
pll bypass. not usable here. we use the input pad

refname: t0_bypass

-------
PARAM:   "Lock":
REFNAME: "t0_lock":
enable pll lock indication (enable to push it on the pad)

refname: t0_lock

-------
PARAM:   "Out":
REFNAME: "t0_eout":
```

```
enable the clock_out on the pad (refclk/2)

refname: t0_eout

-------
PARAM:   "PLL Stabilization Time":
REFNAME: "pll_stabilize":
(1024 * pll_stabilize) is num of e1clk cycles to wait for stabilization put 1.0
milisec = 1024 * 60 * e1clk(66MHz) . lets put 0x80

refname: pll_stabilize

-------
PARAM:   "CCLK: Adapter Core Reference Clock (KHz)":
REFNAME: "adapter_core_ref_clock_khz":
Input core clock to PLL (KHz)

refname: adapter_core_ref_clock_khz

-------
PARAM:   "MCLK: Adapter DMU Reference Clock (KHz)":
REFNAME: "adapter_dmu_ref_clock_khz":
Input DDR Memory clock to PLL (KHz)

refname: adapter_dmu_ref_clock_khz

-------
PARAM:   "DMU Divider Disable":
REFNAME: "disable_dmu_divider":
Select if disable_dmu_divider strapping option [sdostrb] is set.

refname: disable_dmu_divider

-------
PARAM:   "Core Frequency Output":
REFNAME: "core_frequency_khz":
Core Clock Frequency Output from PLL (KHz). 125000-200000 KHz

refname: core_frequency_khz

-------
PARAM:   "DDR DRAM Frequency Output (x1)":
REFNAME: "dram_frequency_1x_khz":
On board DIMMs frequency (x1) (KHz) 80000-166000KHz

refname: dram_frequency_1x_khz

-------
```

```
PARAM:   "DDR DRAM Frequency Output (x2)":
REFNAME: "dram_frequency_2x_khz":
On board DIMMs frequency (x2) (KHz) 160000-333000KHz

refname: dram_frequency_2x_khz

-------
PARAM:   "Allowed VRCLKP/N Frequency Input":
REFNAME: "allowed_vrclkp_khz":
Allowed VRCLKP/N Frequency (KHz)

refname: allowed_vrclkp_khz

-------
PARAM:   "Allowed XRCLKP/N Frequency Input":
REFNAME: "allowed_vrclkp_tg_khz":
Allowed XRCLKP/N Frequency (KHz)

refname: allowed_vrclkp_tg_khz

-------
PARAM:   "Internal core clock must be greater than 125MHz":
REFNAME: "coreclk_gt_125mhz":
coreclk > 125 MHz

refname: coreclk_gt_125mhz

-------
PARAM:   "Coreclk must be greater than half the ddrclk":
REFNAME: "coreclk_gt_fraq_ddrclk_2":
coreclk > ddrclk/2

refname: coreclk_gt_fraq_ddrclk_2

-------
PARAM:   "Log DDR Max Size":
REFNAME: "log2_ddr_size":
Log 2 of DDR Maximum size.
DDR Maximum Size parameter enables the user to
limit the use of the attached memory (DRAM) to
less than actuall size.

refname: log2_ddr_size

-------
PARAM:   "ECC Mode":
REFNAME: "ecc_mode":
```

Determines type of attached DIMMs EEC mode

refname: ecc_mode

PARAM: "Auto Precharge Mode":
REFNAME: "auto_precharge_mode":

Determines Auto Precharge mode

refname: auto_precharge_mode

PARAM: "Cmd Gap Rate0":
REFNAME: "cmd_gap_rate0":
Minimum gap (in clocks) between execution of 2 requests (RD or WR) from the PCI port.
For power reduction. This value affects performance.

refname: cmd_gap_rate0

PARAM: "Cmd Gap Rate1":
REFNAME: "cmd_gap_rate1":
Minimum gap (in clocks) between execution of 2 requests (RD or WR) from the HCA port.
For power reduction. This value affects performance.

refname: cmd_gap_rate1

PARAM: "Hide DDR":
REFNAME: "hide_ddr_en":
Enables/disables the DDR BAR.

refname: hide_ddr_en

PARAM: "DDR Address Lsb":
REFNAME: "ddr_addr_lsb":
[31:0] bits address of ddr space given by user.

refname: ddr_addr_lsb

PARAM: "DDR Address Msb":
REFNAME: "ddr_addr_msb":
[63:32] bits address of ddr space given by user.

```
refname: ddr_addr_msb

-------
PARAM:   "Exit SR WAITING PERIOD[DCLK]":
REFNAME: "xsr_dclk_wait":
Numer of dram clocks InfiniHost waits before exiting
after Self-Refresh has been activated.

refname: xsr_dclk_wait

-------
PARAM:   "SPD Address":
REFNAME: "SPD0_addr":
First DIMM slot address on board.
Please specify the following values:
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.
NOT PRESSENT: 0x100 - DIMMs not present in any form.
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD0_addr

-------
PARAM:   "SPD Address":
REFNAME: "SPD1_addr":
Second Dimm slot address on board.
Please specify the following values:
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.
NOT PRESSENT: 0x100 - DIMMs not present in any form.
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD1_addr

-------
PARAM:   "SPD offset":
REFNAME: "SPD0_offset":
first Dimm slot offset on EEPROM (valid only if address is from EEPROM).

refname: SPD0_offset

-------
PARAM:   "SPD Offset":
REFNAME: "SPD1_offset":
Second Dimm slot address EEPROM (valid only if address is from EEPROM).

refname: SPD1_offset

-------
```

```
PARAM:   "SPD 16 bit addr ":
REFNAME: "SPD0_width":
First Dimm slot EEPROM address width (valid only if address is from EEPROM).

refname: SPD0_width

-------
PARAM:   "SPD 16 bit addr ":
REFNAME: "SPD1_width":
Second Dimm slot EEPROM address width (valid only if address is from EEPROM).

refname: SPD1_width

-------
PARAM:   "WriteOnly DIMM":
REFNAME: "dimm0_writeonly":


refname: dimm0_writeonly

-------
PARAM:   "WriteOnly DIMM":
REFNAME: "dimm1_writeonly":


refname: dimm1_writeonly

-------
PARAM:   "Supported Dimm Types":
REFNAME: "dimm0_types":


refname: dimm0_types

-------
PARAM:   "Supported Dimm Types":
REFNAME: "dimm1_types":


refname: dimm1_types

-------
PARAM:   "SPD Address":
REFNAME: "SPD2_addr":
Third Dimm slot address on board.
Please specify the following values:
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.
NOT PRESSENT: 0x100 - DIMMs not present in any form.
```

```
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD2_addr

-------
PARAM:   "SPD Address":
REFNAME: "SPD3_addr":
Fourth Dimm slot address on board.
Please specify the following values:
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.
NOT PRESSENT: 0x100 - DIMMs not present in any form.
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD3_addr

-------
PARAM:   "SPD offset":
REFNAME: "SPD2_offset":
first Dimm slot offset on EEPROM (valid only if address is from EEPROM).

refname: SPD2_offset

-------
PARAM:   "SPD Offset":
REFNAME: "SPD3_offset":
Second Dimm slot address EEPROM (valid only if address is from EEPROM).

refname: SPD3_offset

-------
PARAM:   "SPD 16 bit addr ":
REFNAME: "SPD2_width":
Third Dimm slot EEPROM address width (valid only if address is from EEPROM).

refname: SPD2_width

-------
PARAM:   "SPD 16 bit addr ":
REFNAME: "SPD3_width":
Forth Dimm slot EEPROM address width (valid only if address is from EEPROM).

refname: SPD3_width

-------
PARAM:   "WriteOnly DIMM":
REFNAME: "dimm2_writeonly":
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```
refname: dimm2_writeonly

-------
PARAM:   "WriteOnly DIMM":
REFNAME: "dimm3_writeonly":


refname: dimm3_writeonly

-------
PARAM:   "Supported Dimm Types":
REFNAME: "dimm2_types":


refname: dimm2_types

-------
PARAM:   "Supported Dimm Types":
REFNAME: "dimm3_types":


refname: dimm3_types

-------
PARAM:   "dimm0_byte0":
REFNAME: "dimm0_byte0":


refname: dimm0_byte0

-------
PARAM:   "dimm0_byte1":
REFNAME: "dimm0_byte1":


refname: dimm0_byte1

-------
PARAM:   "dimm0_byte2":
REFNAME: "dimm0_byte2":


refname: dimm0_byte2

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PARAM:   "dimm0_byte3":
REFNAME: "dimm0_byte3":
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refname: dimm0_byte3

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PARAM:   "dimm0_byte4":
REFNAME: "dimm0_byte4":


refname: dimm0_byte4

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PARAM:   "dimm0_byte5":
REFNAME: "dimm0_byte5":


refname: dimm0_byte5

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PARAM:   "dimm0_byte6":
REFNAME: "dimm0_byte6":


refname: dimm0_byte6

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PARAM:   "dimm0_byte7":
REFNAME: "dimm0_byte7":


refname: dimm0_byte7

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PARAM:   "dimm0_byte8":
REFNAME: "dimm0_byte8":


refname: dimm0_byte8

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PARAM:   "dimm0_byte9":
REFNAME: "dimm0_byte9":


refname: dimm0_byte9

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PARAM:   "dimm0_byte10":
REFNAME: "dimm0_byte10":
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refname: dimm0_byte10

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PARAM:   "dimm0_byte11":
REFNAME: "dimm0_byte11":


refname: dimm0_byte11

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PARAM:   "dimm0_byte12":
REFNAME: "dimm0_byte12":


refname: dimm0_byte12

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PARAM:   "dimm0_byte13":
REFNAME: "dimm0_byte13":


refname: dimm0_byte13

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PARAM:   "dimm0_byte14":
REFNAME: "dimm0_byte14":


refname: dimm0_byte14

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PARAM:   "dimm0_byte15":
REFNAME: "dimm0_byte15":


refname: dimm0_byte15

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PARAM:   "dimm0_byte16":
REFNAME: "dimm0_byte16":


refname: dimm0_byte16

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PARAM:   "dimm0_byte17":
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REFNAME: "dimm0_byte17":


refname: dimm0_byte17

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PARAM:   "dimm0_byte18":
REFNAME: "dimm0_byte18":


refname: dimm0_byte18

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PARAM:   "dimm0_byte19":
REFNAME: "dimm0_byte19":


refname: dimm0_byte19

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PARAM:   "dimm0_byte20":
REFNAME: "dimm0_byte20":


refname: dimm0_byte20

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PARAM:   "dimm0_byte21":
REFNAME: "dimm0_byte21":


refname: dimm0_byte21

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PARAM:   "dimm0_byte22":
REFNAME: "dimm0_byte22":


refname: dimm0_byte22

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PARAM:   "dimm0_byte23":
REFNAME: "dimm0_byte23":


refname: dimm0_byte23

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PARAM:   "dimm0_byte24":
REFNAME: "dimm0_byte24":


refname: dimm0_byte24

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PARAM:   "dimm0_byte25":
REFNAME: "dimm0_byte25":


refname: dimm0_byte25

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PARAM:   "dimm0_byte26":
REFNAME: "dimm0_byte26":


refname: dimm0_byte26

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PARAM:   "dimm0_byte27":
REFNAME: "dimm0_byte27":


refname: dimm0_byte27

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PARAM:   "dimm0_byte28":
REFNAME: "dimm0_byte28":


refname: dimm0_byte28

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PARAM:   "dimm0_byte29":
REFNAME: "dimm0_byte29":


refname: dimm0_byte29

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PARAM:   "dimm0_byte30":
REFNAME: "dimm0_byte30":


refname: dimm0_byte30
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PARAM:   "dimm0_byte31":
REFNAME: "dimm0_byte31":


refname: dimm0_byte31

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PARAM:   "dimm0_byte32":
REFNAME: "dimm0_byte32":


refname: dimm0_byte32

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PARAM:   "dimm0_byte33":
REFNAME: "dimm0_byte33":


refname: dimm0_byte33

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REFNAME: "dimm0_byte34":


refname: dimm0_byte34

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PARAM:   "dimm0_byte35":
REFNAME: "dimm0_byte35":


refname: dimm0_byte35

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REFNAME: "dimm0_byte36":


refname: dimm0_byte36

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PARAM:   "dimm0_byte37":
REFNAME: "dimm0_byte37":


refname: dimm0_byte37
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PARAM:   "dimm0_byte38":
REFNAME: "dimm0_byte38":


refname: dimm0_byte38

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REFNAME: "dimm0_byte39":


refname: dimm0_byte39

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PARAM:   "dimm0_byte40":
REFNAME: "dimm0_byte40":


refname: dimm0_byte40

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PARAM:   "dimm0_byte41":
REFNAME: "dimm0_byte41":


refname: dimm0_byte41

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PARAM:   "dimm0_byte42":
REFNAME: "dimm0_byte42":


refname: dimm0_byte42

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REFNAME: "dimm0_byte43":


refname: dimm0_byte43

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PARAM:   "dimm0_byte44":
REFNAME: "dimm0_byte44":
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refname: dimm0_byte44

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REFNAME: "dimm0_byte45":


refname: dimm0_byte45

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REFNAME: "dimm0_byte46":


refname: dimm0_byte46

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refname: dimm0_byte50

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PARAM:   "dimm0_byte51":
REFNAME: "dimm0_byte51":
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refname: dimm0_byte51

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refname: dimm0_byte52

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PARAM:   "dimm0_byte58":
REFNAME: "dimm0_byte58":
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refname: dimm0_byte58

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refname: dimm0_byte59

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PARAM:   "dimm1_byte1":
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REFNAME: "dimm1_byte1":


refname: dimm1_byte1

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PARAM:   "dimm1_byte2":
REFNAME: "dimm1_byte2":


refname: dimm1_byte2

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PARAM:   "dimm1_byte3":
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refname: dimm1_byte6

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PARAM:   "dimm1_byte7":
REFNAME: "dimm1_byte7":


refname: dimm1_byte7

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PARAM:   "dimm1_byte8":
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refname: dimm1_byte8

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refname: dimm1_byte9

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refname: dimm1_byte20

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PARAM:   "dimm1_byte21":
REFNAME: "dimm1_byte21":


refname: dimm1_byte21
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PARAM:   "dimm1_byte22":
REFNAME: "dimm1_byte22":


refname: dimm1_byte22

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REFNAME: "dimm1_byte23":


refname: dimm1_byte23

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refname: dimm1_byte27

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PARAM:   "dimm1_byte28":
REFNAME: "dimm1_byte28":
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refname: dimm1_byte28

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REFNAME: "dimm1_byte29":


refname: dimm1_byte29

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REFNAME: "dimm1_byte30":


refname: dimm1_byte30

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refname: dimm1_byte31

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REFNAME: "dimm1_byte32":


refname: dimm1_byte32

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PARAM:   "dimm1_byte33":
REFNAME: "dimm1_byte33":


refname: dimm1_byte33

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PARAM:   "dimm1_byte34":
REFNAME: "dimm1_byte34":


refname: dimm1_byte34

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PARAM:   "dimm1_byte35":
REFNAME: "dimm1_byte35":
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refname: dimm1_byte35

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PARAM:   "dimm1_byte36":
REFNAME: "dimm1_byte36":


refname: dimm1_byte36

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PARAM:   "dimm1_byte37":
REFNAME: "dimm1_byte37":


refname: dimm1_byte37

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refname: dimm1_byte38

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refname: dimm1_byte39

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refname: dimm1_byte40

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PARAM:   "dimm1_byte41":
REFNAME: "dimm1_byte41":


refname: dimm1_byte41

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PARAM:   "dimm1_byte42":
REFNAME: "dimm1_byte42":
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refname: dimm1_byte42

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PARAM:   "dimm1_byte43":
REFNAME: "dimm1_byte43":


refname: dimm1_byte43

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PARAM:   "dimm1_byte44":
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refname: dimm1_byte44

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PARAM:   "dimm1_byte45":
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PARAM:   "dimm1_byte46":
REFNAME: "dimm1_byte46":


refname: dimm1_byte46

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PARAM:   "dimm1_byte47":
REFNAME: "dimm1_byte47":


refname: dimm1_byte47

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PARAM:   "dimm1_byte48":
REFNAME: "dimm1_byte48":


refname: dimm1_byte48

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PARAM:   "dimm1_byte49":
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REFNAME: "dimm1_byte49":


refname: dimm1_byte49

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PARAM:   "dimm1_byte50":
REFNAME: "dimm1_byte50":


refname: dimm1_byte50

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PARAM:   "dimm1_byte51":
REFNAME: "dimm1_byte51":


refname: dimm1_byte51

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PARAM:   "dimm1_byte52":
REFNAME: "dimm1_byte52":


refname: dimm1_byte52

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PARAM:   "dimm1_byte53":
REFNAME: "dimm1_byte53":


refname: dimm1_byte53

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PARAM:   "dimm1_byte54":
REFNAME: "dimm1_byte54":


refname: dimm1_byte54

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PARAM:   "dimm1_byte55":
REFNAME: "dimm1_byte55":


refname: dimm1_byte55

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PARAM:   "dimm1_byte56":
REFNAME: "dimm1_byte56":


refname: dimm1_byte56

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PARAM:   "dimm1_byte57":
REFNAME: "dimm1_byte57":


refname: dimm1_byte57

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PARAM:   "dimm1_byte58":
REFNAME: "dimm1_byte58":


refname: dimm1_byte58

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PARAM:   "dimm1_byte59":
REFNAME: "dimm1_byte59":


refname: dimm1_byte59

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PARAM:   "dimm1_byte60":
REFNAME: "dimm1_byte60":


refname: dimm1_byte60

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PARAM:   "dimm1_byte61":
REFNAME: "dimm1_byte61":


refname: dimm1_byte61

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PARAM:   "dimm1_byte62":
REFNAME: "dimm1_byte62":


refname: dimm1_byte62
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PARAM:   "dimm1_byte63":
REFNAME: "dimm1_byte63":


refname: dimm1_byte63

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PARAM:   "dimm2_byte0":
REFNAME: "dimm2_byte0":


refname: dimm2_byte0

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PARAM:   "dimm2_byte1":
REFNAME: "dimm2_byte1":


refname: dimm2_byte1

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PARAM:   "dimm2_byte2":
REFNAME: "dimm2_byte2":


refname: dimm2_byte2

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PARAM:   "dimm2_byte3":
REFNAME: "dimm2_byte3":


refname: dimm2_byte3

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PARAM:   "dimm2_byte4":
REFNAME: "dimm2_byte4":


refname: dimm2_byte4

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PARAM:   "dimm2_byte5":
REFNAME: "dimm2_byte5":


refname: dimm2_byte5
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PARAM:   "dimm2_byte6":
REFNAME: "dimm2_byte6":


refname: dimm2_byte6

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PARAM:   "dimm2_byte7":
REFNAME: "dimm2_byte7":


refname: dimm2_byte7

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PARAM:   "dimm2_byte8":
REFNAME: "dimm2_byte8":


refname: dimm2_byte8

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PARAM:   "dimm2_byte9":
REFNAME: "dimm2_byte9":


refname: dimm2_byte9

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PARAM:   "dimm2_byte10":
REFNAME: "dimm2_byte10":


refname: dimm2_byte10

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PARAM:   "dimm2_byte11":
REFNAME: "dimm2_byte11":


refname: dimm2_byte11

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PARAM:   "dimm2_byte12":
REFNAME: "dimm2_byte12":
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refname: dimm2_byte12

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PARAM:   "dimm2_byte13":
REFNAME: "dimm2_byte13":


refname: dimm2_byte13

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PARAM:   "dimm2_byte14":
REFNAME: "dimm2_byte14":


refname: dimm2_byte14

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PARAM:   "dimm2_byte15":
REFNAME: "dimm2_byte15":


refname: dimm2_byte15

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PARAM:   "dimm2_byte16":
REFNAME: "dimm2_byte16":


refname: dimm2_byte16

-------
PARAM:   "dimm2_byte17":
REFNAME: "dimm2_byte17":


refname: dimm2_byte17

-------
PARAM:   "dimm2_byte18":
REFNAME: "dimm2_byte18":


refname: dimm2_byte18

-------
PARAM:   "dimm2_byte19":
REFNAME: "dimm2_byte19":
```

```
refname: dimm2_byte19

-------
PARAM:   "dimm2_byte20":
REFNAME: "dimm2_byte20":


refname: dimm2_byte20

-------
PARAM:   "dimm2_byte21":
REFNAME: "dimm2_byte21":


refname: dimm2_byte21

-------
PARAM:   "dimm2_byte22":
REFNAME: "dimm2_byte22":


refname: dimm2_byte22

-------
PARAM:   "dimm2_byte23":
REFNAME: "dimm2_byte23":


refname: dimm2_byte23

-------
PARAM:   "dimm2_byte24":
REFNAME: "dimm2_byte24":


refname: dimm2_byte24

-------
PARAM:   "dimm2_byte25":
REFNAME: "dimm2_byte25":


refname: dimm2_byte25

-------
PARAM:   "dimm2_byte26":
REFNAME: "dimm2_byte26":
```

```
refname: dimm2_byte26

-------
PARAM:   "dimm2_byte27":
REFNAME: "dimm2_byte27":


refname: dimm2_byte27

-------
PARAM:   "dimm2_byte28":
REFNAME: "dimm2_byte28":


refname: dimm2_byte28

-------
PARAM:   "dimm2_byte29":
REFNAME: "dimm2_byte29":


refname: dimm2_byte29

-------
PARAM:   "dimm2_byte30":
REFNAME: "dimm2_byte30":


refname: dimm2_byte30

-------
PARAM:   "dimm2_byte31":
REFNAME: "dimm2_byte31":


refname: dimm2_byte31

-------
PARAM:   "dimm2_byte32":
REFNAME: "dimm2_byte32":


refname: dimm2_byte32

-------
PARAM:   "dimm2_byte33":
```

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REFNAME: "dimm2_byte33":


refname: dimm2_byte33

-------
PARAM:   "dimm2_byte34":
REFNAME: "dimm2_byte34":


refname: dimm2_byte34

-------
PARAM:   "dimm2_byte35":
REFNAME: "dimm2_byte35":


refname: dimm2_byte35

-------
PARAM:   "dimm2_byte36":
REFNAME: "dimm2_byte36":


refname: dimm2_byte36

-------
PARAM:   "dimm2_byte37":
REFNAME: "dimm2_byte37":


refname: dimm2_byte37

-------
PARAM:   "dimm2_byte38":
REFNAME: "dimm2_byte38":


refname: dimm2_byte38

-------
PARAM:   "dimm2_byte39":
REFNAME: "dimm2_byte39":


refname: dimm2_byte39

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```

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PARAM:   "dimm2_byte40":
REFNAME: "dimm2_byte40":


refname: dimm2_byte40

-------
PARAM:   "dimm2_byte41":
REFNAME: "dimm2_byte41":


refname: dimm2_byte41

-------
PARAM:   "dimm2_byte42":
REFNAME: "dimm2_byte42":


refname: dimm2_byte42

-------
PARAM:   "dimm2_byte43":
REFNAME: "dimm2_byte43":


refname: dimm2_byte43

-------
PARAM:   "dimm2_byte44":
REFNAME: "dimm2_byte44":


refname: dimm2_byte44

-------
PARAM:   "dimm2_byte45":
REFNAME: "dimm2_byte45":


refname: dimm2_byte45

-------
PARAM:   "dimm2_byte46":
REFNAME: "dimm2_byte46":


refname: dimm2_byte46
```

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-------
PARAM:   "dimm2_byte47":
REFNAME: "dimm2_byte47":


refname: dimm2_byte47

-------
PARAM:   "dimm2_byte48":
REFNAME: "dimm2_byte48":


refname: dimm2_byte48

-------
PARAM:   "dimm2_byte49":
REFNAME: "dimm2_byte49":


refname: dimm2_byte49

-------
PARAM:   "dimm2_byte50":
REFNAME: "dimm2_byte50":


refname: dimm2_byte50

-------
PARAM:   "dimm2_byte51":
REFNAME: "dimm2_byte51":


refname: dimm2_byte51

-------
PARAM:   "dimm2_byte52":
REFNAME: "dimm2_byte52":


refname: dimm2_byte52

-------
PARAM:   "dimm2_byte53":
REFNAME: "dimm2_byte53":


refname: dimm2_byte53
```

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-------
PARAM:   "dimm2_byte54":
REFNAME: "dimm2_byte54":


refname: dimm2_byte54

-------
PARAM:   "dimm2_byte55":
REFNAME: "dimm2_byte55":


refname: dimm2_byte55

-------
PARAM:   "dimm2_byte56":
REFNAME: "dimm2_byte56":


refname: dimm2_byte56

-------
PARAM:   "dimm2_byte57":
REFNAME: "dimm2_byte57":


refname: dimm2_byte57

-------
PARAM:   "dimm2_byte58":
REFNAME: "dimm2_byte58":


refname: dimm2_byte58

-------
PARAM:   "dimm2_byte59":
REFNAME: "dimm2_byte59":


refname: dimm2_byte59

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PARAM:   "dimm2_byte60":
REFNAME: "dimm2_byte60":
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refname: dimm2_byte60

-------
PARAM:   "dimm2_byte61":
REFNAME: "dimm2_byte61":


refname: dimm2_byte61

-------
PARAM:   "dimm2_byte62":
REFNAME: "dimm2_byte62":


refname: dimm2_byte62

-------
PARAM:   "dimm2_byte63":
REFNAME: "dimm2_byte63":


refname: dimm2_byte63

-------
PARAM:   "dimm3_byte0":
REFNAME: "dimm3_byte0":


refname: dimm3_byte0

-------
PARAM:   "dimm3_byte1":
REFNAME: "dimm3_byte1":


refname: dimm3_byte1

-------
PARAM:   "dimm3_byte2":
REFNAME: "dimm3_byte2":


refname: dimm3_byte2

-------
PARAM:   "dimm3_byte3":
REFNAME: "dimm3_byte3":
```

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refname: dimm3_byte3

-------
PARAM:   "dimm3_byte4":
REFNAME: "dimm3_byte4":


refname: dimm3_byte4

-------
PARAM:   "dimm3_byte5":
REFNAME: "dimm3_byte5":


refname: dimm3_byte5

-------
PARAM:   "dimm3_byte6":
REFNAME: "dimm3_byte6":


refname: dimm3_byte6

-------
PARAM:   "dimm3_byte7":
REFNAME: "dimm3_byte7":


refname: dimm3_byte7

-------
PARAM:   "dimm3_byte8":
REFNAME: "dimm3_byte8":


refname: dimm3_byte8

-------
PARAM:   "dimm3_byte9":
REFNAME: "dimm3_byte9":


refname: dimm3_byte9

-------
PARAM:   "dimm3_byte10":
REFNAME: "dimm3_byte10":
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refname: dimm3_byte10

-------
PARAM:   "dimm3_byte11":
REFNAME: "dimm3_byte11":


refname: dimm3_byte11

-------
PARAM:   "dimm3_byte12":
REFNAME: "dimm3_byte12":


refname: dimm3_byte12

-------
PARAM:   "dimm3_byte13":
REFNAME: "dimm3_byte13":


refname: dimm3_byte13

-------
PARAM:   "dimm3_byte14":
REFNAME: "dimm3_byte14":


refname: dimm3_byte14

-------
PARAM:   "dimm3_byte15":
REFNAME: "dimm3_byte15":


refname: dimm3_byte15

-------
PARAM:   "dimm3_byte16":
REFNAME: "dimm3_byte16":


refname: dimm3_byte16

-------
PARAM:   "dimm3_byte17":
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REFNAME: "dimm3_byte17":


refname: dimm3_byte17

-------
PARAM:   "dimm3_byte18":
REFNAME: "dimm3_byte18":


refname: dimm3_byte18

-------
PARAM:   "dimm3_byte19":
REFNAME: "dimm3_byte19":


refname: dimm3_byte19

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PARAM:   "dimm3_byte20":
REFNAME: "dimm3_byte20":


refname: dimm3_byte20

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PARAM:   "dimm3_byte21":
REFNAME: "dimm3_byte21":


refname: dimm3_byte21

-------
PARAM:   "dimm3_byte22":
REFNAME: "dimm3_byte22":


refname: dimm3_byte22

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PARAM:   "dimm3_byte23":
REFNAME: "dimm3_byte23":


refname: dimm3_byte23

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```

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PARAM:   "dimm3_byte24":
REFNAME: "dimm3_byte24":


refname: dimm3_byte24

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PARAM:   "dimm3_byte25":
REFNAME: "dimm3_byte25":


refname: dimm3_byte25

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PARAM:   "dimm3_byte26":
REFNAME: "dimm3_byte26":


refname: dimm3_byte26

-------
PARAM:   "dimm3_byte27":
REFNAME: "dimm3_byte27":


refname: dimm3_byte27

-------
PARAM:   "dimm3_byte28":
REFNAME: "dimm3_byte28":


refname: dimm3_byte28

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PARAM:   "dimm3_byte29":
REFNAME: "dimm3_byte29":


refname: dimm3_byte29

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PARAM:   "dimm3_byte30":
REFNAME: "dimm3_byte30":


refname: dimm3_byte30
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-------
PARAM:   "dimm3_byte31":
REFNAME: "dimm3_byte31":


refname: dimm3_byte31

-------
PARAM:   "dimm3_byte32":
REFNAME: "dimm3_byte32":


refname: dimm3_byte32

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PARAM:   "dimm3_byte33":
REFNAME: "dimm3_byte33":


refname: dimm3_byte33

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PARAM:   "dimm3_byte34":
REFNAME: "dimm3_byte34":


refname: dimm3_byte34

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PARAM:   "dimm3_byte35":
REFNAME: "dimm3_byte35":


refname: dimm3_byte35

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PARAM:   "dimm3_byte36":
REFNAME: "dimm3_byte36":


refname: dimm3_byte36

-------
PARAM:   "dimm3_byte37":
REFNAME: "dimm3_byte37":


refname: dimm3_byte37
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-------
PARAM:   "dimm3_byte38":
REFNAME: "dimm3_byte38":


refname: dimm3_byte38

-------
PARAM:   "dimm3_byte39":
REFNAME: "dimm3_byte39":


refname: dimm3_byte39

-------
PARAM:   "dimm3_byte40":
REFNAME: "dimm3_byte40":


refname: dimm3_byte40

-------
PARAM:   "dimm3_byte41":
REFNAME: "dimm3_byte41":


refname: dimm3_byte41

-------
PARAM:   "dimm3_byte42":
REFNAME: "dimm3_byte42":


refname: dimm3_byte42

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PARAM:   "dimm3_byte43":
REFNAME: "dimm3_byte43":


refname: dimm3_byte43

-------
PARAM:   "dimm3_byte44":
REFNAME: "dimm3_byte44":
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refname: dimm3_byte44

-------
PARAM:   "dimm3_byte45":
REFNAME: "dimm3_byte45":


refname: dimm3_byte45

-------
PARAM:   "dimm3_byte46":
REFNAME: "dimm3_byte46":


refname: dimm3_byte46

-------
PARAM:   "dimm3_byte47":
REFNAME: "dimm3_byte47":


refname: dimm3_byte47

-------
PARAM:   "dimm3_byte48":
REFNAME: "dimm3_byte48":


refname: dimm3_byte48

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PARAM:   "dimm3_byte49":
REFNAME: "dimm3_byte49":


refname: dimm3_byte49

-------
PARAM:   "dimm3_byte50":
REFNAME: "dimm3_byte50":


refname: dimm3_byte50

-------
PARAM:   "dimm3_byte51":
REFNAME: "dimm3_byte51":
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refname: dimm3_byte51

-------
PARAM:   "dimm3_byte52":
REFNAME: "dimm3_byte52":


refname: dimm3_byte52

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PARAM:   "dimm3_byte53":
REFNAME: "dimm3_byte53":


refname: dimm3_byte53

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PARAM:   "dimm3_byte54":
REFNAME: "dimm3_byte54":


refname: dimm3_byte54

-------
PARAM:   "dimm3_byte55":
REFNAME: "dimm3_byte55":


refname: dimm3_byte55

-------
PARAM:   "dimm3_byte56":
REFNAME: "dimm3_byte56":


refname: dimm3_byte56

-------
PARAM:   "dimm3_byte57":
REFNAME: "dimm3_byte57":


refname: dimm3_byte57

-------
PARAM:   "dimm3_byte58":
REFNAME: "dimm3_byte58":
```

```
refname: dimm3_byte58

-------
PARAM:   "dimm3_byte59":
REFNAME: "dimm3_byte59":


refname: dimm3_byte59

-------
PARAM:   "dimm3_byte60":
REFNAME: "dimm3_byte60":


refname: dimm3_byte60

-------
PARAM:   "dimm3_byte61":
REFNAME: "dimm3_byte61":


refname: dimm3_byte61

-------
PARAM:   "dimm3_byte62":
REFNAME: "dimm3_byte62":


refname: dimm3_byte62

-------
PARAM:   "dimm3_byte63":
REFNAME: "dimm3_byte63":


refname: dimm3_byte63

-------
PARAM:   "FW Size in DDR":
REFNAME: "fw_length":
Log2 of DDR memory allocated for InifniHost FW (Bytes).
This memory area should not be accessed by any
external device (see PRM restrictions).

refname: fw_length
```

```
-------
PARAM:   "FW Trace Buffer Size (MB)":
REFNAME: "total_trace_buf_sz_mb":
Trace Buffer size for all iRISCs. The Trace buffer
is divided to six parts - one for each iRISC.
The trace buffer resides in DDR memory. Its allocation is
in addition to FW required length.

refname: total_trace_buf_sz_mb

-------
PARAM:   "Disable Vendor Specific MADs":
REFNAME: "vendor_specific_sup":
Enables/disable Vendor specific MAD support

refname: vendor_specific_s
-------
PARAM:      "Port1 SerDes0 OBPreAmp"
REFNAME:    "port1_sd0_OBPreAmp"

-------
PARAM="Port1 SerDes1 OBPreAmp"
refname="port1_sd1_OBPreAmp"

-------
PARAM="Port1 SerDes2 OBPreAmp"
refname="port1_sd2_OBPreAmp"

-------
PARAM="Port1 SerDes3 OBPreAmp"
refname="port1_sd3_OBPreAmp"

-------
PARAM="Port2 SerDes0 OBPreAmp"
refname="port2_sd0_OBPreAmp"

-------
PARAM="Port2 SerDes1 OBPreAmp"
refname="port2_sd1_OBPreAmp"

-------
PARAM="Port2 SerDes2 OBPreAmp"
refname="port2_sd2_OBPreAmp"

-------
PARAM="Port2 SerDes3 OBPreAmp"
refname="port2_sd3_OBPreAmp"

-------
PARAM="Port1 SerDes0 OBVoltage"
refname="port1_sd0_OBVoltage"
```

```
-------
PARAM="Port1 SerDes1 OBVoltage"
refname="port1_sd1_OBVoltage"

-------
PARAM="Port1 SerDes2 OBVoltage"
refname="port1_sd2_OBVoltage"

-------
PARAM="Port1 SerDes3 OBVoltage"
refname="port1_sd3_OBVoltage"

-------
PARAM="Port2 SerDes0 OBVoltage"
refname="port2_sd0_OBVoltage"

-------
PARAM="Port2 SerDes1 OBVoltage"
refname="port2_sd1_OBVoltage"

-------
PARAM="Port2 SerDes2 OBVoltage"
refname="port2_sd2_OBVoltage"

-------
PARAM="Port2 SerDes3 OBVoltage"
refname="port2_sd3_OBVoltage"

-------
PARAM="Port1 SerDes0 OBPreEmpPreAmp"
refname="port1_sd0_OBPreEmpPreAmp"

-------
PARAM="Port1 SerDes1 OBPreEmpPreAmp"
refname="port1_sd1_OBPreEmpPreAmp"

-------
PARAM="Port1 SerDes2 OBPreEmpPreAmp"
refname="port1_sd2_OBPreEmpPreAmp"

-------
PARAM="Port1 SerDes3 OBPreEmpPreAmp"
refname="port1_sd3_OBPreEmpPreAmp"

-------
PARAM="Port2 SerDes0 OBPreEmpPreAmp"
refname="port2_sd0_OBPreEmpPreAmp"

-------
PARAM="Port2 SerDes1 OBPreEmpPreAmp"
refname="port2_sd1_OBPreEmpPreAmp"

-------
```

```
PARAM="Port2 SerDes2 OBPreEmpPreAmp"
refname="port2_sd2_OBPreEmpPreAmp"

-------
PARAM="Port2 SerDes3 OBPreEmpPreAmp"
refname="port2_sd3_OBPreEmpPreAmp"

-------
PARAM="Port1 SerDes0 OBPreEmpOut"
refname="port1_sd0_OBPreEmpOut"

-------
PARAM="Port1 SerDes1 OBPreEmpOut"
refname="port1_sd1_OBPreEmpOut"

-------
PARAM="Port1 SerDes2 OBPreEmpOut"
refname="port1_sd2_OBPreEmpOut"

-------
PARAM="Port1 SerDes3 OBPreEmpOut"
refname="port1_sd3_OBPreEmpOut"

-------
PARAM="Port2 SerDes0 OBPreEmpOut"
refname="port2_sd0_OBPreEmpOut"

-------
PARAM="Port2 SerDes1 OBPreEmpOut"
refname="port2_sd1_OBPreEmpOut"

-------
PARAM="Port2 SerDes2 OBPreEmpOut"
refname="port2_sd2_OBPreEmpOut"

-------
PARAM="Port2 SerDes3 OBPreEmpOut"
refname="port2_sd3_OBPreEmpOut"

-------
PARAM="Port1 SerDes0 RX Equalization"
refname="port1_sd0_Equal"

-------
PARAM="Port1 SerDes1 RX Equalization"
refname="port1_sd1_Equal"

-------
PARAM="Port1 SerDes2 RX Equalization"
refname="port1_sd2_Equal"

-------
PARAM="Port1 SerDes3 RX Equalization"
refname="port1_sd3_Equal"
```

```
-------
PARAM="Port2 SerDes0 RX Equalization"
refname="port2_sd0_Equal"

-------
PARAM="Port2 SerDes1 RX Equalization"
refname="port2_sd1_Equal"

-------
PARAM="Port2 SerDes2 RX Equalization"
refname="port2_sd2_Equal"

-------
PARAM="Port2 SerDes3 RX Equalization"
refname="port2_sd3_Equal"
```