



Release Notes

MT25208 InfiniHost III Ex Firmware

(MT23108 InfiniHost-Compatible Mode)

FW-25208 Rev 4.6.2

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1 Overview

This document summarizes the contents of Rev 4.6.2 release of MT25208 InfiniHost III Ex Firmware FW-25208. This is the Beta firmware release of the MT25208 device functioning as an MT23108 InfiniHost-Compatible device.

The document consists of the following sections:

- This “Overview” (page 3)
- “Major New Features” (page 3)
- “Fixes for Known Issues” (page 4)
- “Known Issues” (page 5)
- “Invariant Sector Changes / Fixes” (page 7)
- “History” (page 8)
- “InfiniHost FW parameters with “refnames”” (page 10) - This is a list of FW parameters settable in the *Board Definition file*

2 Major New Features

None

3 Fixes for Known Issues

The following table describes known issues from previous releases of InfiniHost III Ex firmware which were fixed in this firmware release.

Table 1 - Fixed Known Issues

Issue	Description	Discovered in	Fixed in
Consumer Index corruption in a Completion Queue	When using Increment_CI doorbells, to increment the CI in more than 1, CI may advance wrongly, causing a false CQ overrun, or not detecting a real overrun (ID: 27893)	4.6.1	4.6.2
Memory Region WindowCount corruption	When deallocating a window and trying to bind it simultaneously, the Region entry WindowsCount may be corrupted. (ID: 26829)	4.6.1	4.6.2

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4 Known Issues

The following table describes known issues in this firmware release and possible workarounds.

Table 2 - Known Issues

Issue	Description	Current Implemented Workaround in FW	Possible Workaround in Driver	Patch Release (fix)	Scheduled Release (fix)
MSIx vectors	Writing to MSIX vectors (Address/Data/Mask) does not take immediate effect. There may be MSIX messages that leave the device according to the old vector.	NA	NA	NA	NA
QPC.Flight_LIM	QPC field – no HW limit, infinite WQEs on send.	NA	NA	NA	NA
QUERY_DDR	Query does not return JEDEC vendor ID yet. Scope of status is limited to active / not active.	NA	NA	NA	NA
RTR2RTS_QPEE; SQD2RTS_QPEE: changing optional fields rra_max and ra_buf_index is not supported.	The optional fields rra_max and ra_buf_index are not supported in the RTR2RTS_QPEE and SQD2TRS_QPEE commands.	Change requests for these fields will not take effect, and no error indication is provided.	Mask these optional fields	NA	NA
PCI 2.3 control and status - for interrupts	InfiniHost III Ex does not support PCI2.3 control and status bits for interrupts.	NA	NA	NA	NA
Change of memory bars on a disabled system	Changing memory bars size / addresses between SYS_DIS and SYS_EN may cause the InfiniHost III Ex to hang (ID: 24206)	NA	NA	NA	NA
BAR resizing on an enabled system	Changing bar sizes when a system is enabled may cause the InfiniHost III Ex to hang (ID: 24208).	NA	NA	NA	NA
SW reset via configuration cycles	SW reset via config cycles may create double PCI- Express completions for the configuration transaction.	NA	If InfiniHost III Ex boots in memory controller mode, perform power cycle / hot reset after restoring the flash.	NA	NA
SW reset is performed during a configuration transaction	If SW reset is performed while a configuration transaction is outstanding, it may create double PCI- Express completions for the configuration transaction.	NA	Do not perform SW reset during configuration cycles.	NA	NA
Flash CRC error	InfiniHost III Ex fails to report a flash CRC error as required by the Flash Burning Application Notes	NA	NA	NA	NA

Table 2 - Known Issues (Continued)

Issue	Description	Current Implemented Workaround in FW	Possible Workaround in Driver	Patch Release (fix)	Scheduled Release (fix)
MADs:PortInfo Get()	When querying for information about an InfiniHost III Ex IB port via its other IB port, the wrong Local port number is returned. Instead of the number of the second port, the one which received the MAD packets, the number of the first port is being returned. (ID: 24177)	NA	NA	NA	NA
Change of Link Width via infiniburn (IB_TAB)	Change of Link Width via infiniburn (IB_TAB) does not take effect. (ID: 24211)	NA	NA	NA	NA

4.1 Unsupported *InfiniHost III Ex Programmer's Reference Manual* Changes

The following features of *MT25208 InfiniHost III Ex Programmer's Reference Manual (Rev 0.45)* are not scheduled to be supported:

1. Flight lim value in QPC may show a value other than 0'1111 even when set for unlimited usage.

5 Invariant Sector Changes / Fixes

Issue	Description	Discovered in	Fixed in
PCI memory space must be disabled by default	PCI memory space must be disabled by default (ID: 27341)	4.5.3	4.6.1
SW reset may block PCIe message generation	In some cases, SW reset may block the generation of future PCIe messages by the device (ID: 21721,27015)	4.5.3	4.6.1
PCI express DeviceControl.unsupported_error_report_enable is R/W	When flash is corrupted, bit 3 in device control (unsupported error reporting enable) is Read Only. It must be read/write (ID: 25570)	4.5.0	4.5.3
PCI compliancy and init changes	Revision number changed to 21	4.0.1	4.5.0

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6 History

Table 3 - Fixed Issues History

Issue	Description	Discovered in	Fixed in
access to VPD with partial ByteEnables	configuraion access to VPD with partial ByteEnables may cause VPD corruption (ID: 27690)	4.5.3	4.6.1
MAD with bad methods	MAD with an unsupported method should be dropped (ID: 27472)	4.5.3	4.6.1
QP in retry may halt sending	A QP that is committing a message retry may hang and stop sending it (ID: 27252)	4.5.3	4.6.1
Q_Key source changes from QPC /WQE	If the Q_Key source changes from QPC /WQE, Infini-Host generates a packet with a wrong Q_key (ID: 21987)	4.5.3	4.6.1
Successful TimeOut-Driven-APM may cause QP context corruption	When an APM occurs as a result of TimeOut, QP context may be corrupted (ID: 26632)	4.5.3	4.6.1
Closing-QP commands get stuck	The commands 2RST_QPEE and RST2ERR_QPEE get stuck if a bad NACK is sent simultaneously (ID: 26243)	4.5.3	4.6.1
Validation of duplicate RDMA_READ/Atomic	Duplicate RDMA_READs/Atomics are not validated against the original requests (ID: 26247)	4.5.3	4.6.1
APM EQE due to TimeOut	An APM that resulted from a TimeOut does not generate an "APM succeeded" EQE (ID: 25948)	4.5.3	4.6.1
Binding Memory Windows across a 4GB boundary	There is an error in binding a Memory Window across a 4GB boundary (ID: 25958)	4.5.3	4.6.1
MAD with wrong BaseVersion or ClassVersion	MAD with wrong BaseVersion or ClassVersion should return status 0x1 (ID: 25888)	4.5.0	4.5.3
PortInfo.ResponseTime	The returned PortInfo.ResponseTime is too short (ID: 10597)	4.5.0	4.5.3
MAD with wrong Attribute-Modifier	MAD with wrong AttributeModifier should cause the response-MAD to have status INVALID_ATTR (ID: 25875)	4.5.0	4.5.3
MTTs in addresses > 4GB	If MTTs are in address > 4GB (e.g. in HIDE DDR), the device may get stuck (ID: 25877)	4.5.0	4.5.3
FW Debug version Data Section corruption	In Debug version of FW, FW Linker can cause a corruption in the Data Section of iRISC (ID: 25774)	4.5.0	4.5.3
PCI express DeviceControl.unsupported_error_report_enable is R/W	When flash is corrupted, bit 3 in device control (unsupported error reporting enable) was Read Only. It must be read/write (ID: 25570)	4.5.0	4.5.3
Link phy error threshold	link phy error threshold was set to a value larger by 1 than the one accepted in portInfo SET() (ID: 25854)	4.5.0	4.5.3
QP state mis-calculation	QPSTATE is shifted in a bit when QPC is non-cacheable. This may cause an unsolicited ACK to be dropped (ID: 25814)	4.5.0	4.5.3
local_ca_ack_delay	QUERY_DEV_LIM.local_ca_ack_delay was 16, which implies 266ms. Changed to 15. Driver can choose to return a lower number for in a non-stress case (ID: 25584)	4.5.0	4.5.3
CQE with error counters	The error counters sq_num_wrfe and rq_num_wrfe miss some increments (ID: 24463)	4.5.0	4.5.3

Issue	Description	Discovered in	Fixed in
2err_qp/2rst_qpee starvation	If a CQE with Error is scheduled, and a heavy back-pressure is applied by UpLink, QP may be put to end of queue, and wait a long time till next chance to generate the CQE w/ Error (ID: 25044)	4.5.0	4.5.3
EQE loss	In stress, an ARM doorbell that should discover a non-empty CQ may be bypassed by a SET_CI doorbell. Thus CQ will seem empty, and an EQE will not be generated (ID: 24911)	4.5.0	4.5.3
MSIX memory mapped tables endianness	MSIX vectors and pending bits have wrong endianness (ID: 22794)	4.5.0	4.5.3

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Appendix: InfiniHost FW parameters with “refnames”

This appendix lists all InfiniHost FW parameters settable in the Board Definition file used by the MST tool Infiniburn. For details, please refer to *MST User's Manual, Document #2125SM*.

```
-----
PARAM:   "Adapter Vendor ID":
REFNAME: "adapter_vendor_id":
Adapter Vendor ID reported to QUERY_ADAPTER query by Driver

refname: adapter_vendor_id

-----
PARAM:   "Adapter Device ID":
REFNAME: "adapter_dev_id":
Adapter Device ID reported to QUERY_ADAPTER query by Driver

refname: adapter_dev_id

-----
PARAM:   "Adapter Revision ID":
REFNAME: "adapter_rev_id":
Adapter Revision ID reported to QUERY_ADAPTER query by Driver

refname: adapter_rev_id

-----
PARAM:   "Adapter VSD":
REFNAME: "adapter_vsd":
Vendor Specific Data on flash

refname: adapter_vsd

-----
PARAM:   "PSID":
REFNAME: "PSID":
Parameter Set IDentification

refname: PSID

-----
PARAM:   "INTA# Pin ID":
REFNAME: "INTA":
Device GPIO pin number which is connected
to INTA# on the adapter. If INTO# pin is
connected to INTA#, set value to 63.
```

refname: INTA

PARAM: "SERR":
REFNAME: "report_catastrophic_error_serr":
Enables/Disables the pulling of SERR
interrupt pin upon catastrophic error.

refname: report_catastrophic_error_serr

PARAM: "INTO":
REFNAME: "report_catastrophic_error_into":
Enables/Disables the pulling of INTO
interrupt pin upon catastrophic error.

refname: report_catastrophic_error_into

PARAM: "INTB":
REFNAME: "report_catastrophic_error_intb":
Enables/Disables the pulling of INTB
interrupt pin upon catastrophic error.

refname: report_catastrophic_error_intb

PARAM: "SERR":
REFNAME: "unreport_catastrophic_error_serr":
Enables/Disables the pulling of SERR
interrupt pin upon catastrophic error.

refname: unreport_catastrophic_error_serr

PARAM: "INTO":
REFNAME: "unreport_catastrophic_error_into":
Enables/Disables the pulling of INTO
interrupt pin upon catastrophic error.

refname: unreport_catastrophic_error_into

PARAM: "INTB":
REFNAME: "unreport_catastrophic_error_intb":
Enables/Disables the pulling of INTB
interrupt pin upon catastrophic error.

refname: unreport_catastrophic_error_intb

PARAM: "Interrupt Coalescing Delay":

REFNAME: "int_coalsing_delay":

Min delay between two consecutive interrupts generated by HCA (in clock units)

refname: int_coalsing_delay

PARAM: "Expansion ROM Enable":

REFNAME: "exp_rom_en":

Enable Expansion ROM BAR.

refname: exp_rom_en

PARAM: "VPD Enable":

REFNAME: "vpd_enable":

Disable/enable the VPD support

refname: vpd_enable

PARAM: "VPD size":

REFNAME: "vpd_size":

VPD size in bytes.

refname: vpd_size

PARAM: "Log2 VPD EEPROM size":

REFNAME: "log2_vpd_eeprom_size":

size of each one of EEPROM slaves of the VPD

refname: log2_vpd_eeprom_size

PARAM: "Num of VPD EEPROMs":

REFNAME: "vpd_num_of_eeproms":

number of EEPROM slaves that contain the VPD

refname: vpd_num_of_eeproms

PARAM: "VPD EEPROM addr":

REFNAME: "vpd_address":

i2c slave address of EEPROM. (first EEPROM if there are multiple addresses.
Other EEPROM's i2c addresses are successive.

refname: vpd_address

```
-----
PARAM:   "VPD EEPROM offset":
REFNAME: "vpd_offset":
  offset in EEPROM.

refname: vpd_offset

-----
PARAM:   "VPD i2c width 16 bits":
REFNAME: "vpd_i2c_16bit":
  i2c bit width is 16 bits (rather than 8 bits)

refname: vpd_i2c_16bit

-----
PARAM:   "Slot Clock Configuration":
REFNAME: "slot_clock_cfg":
  PCI Express Link Status Register. Slot Clock Configuration.
  This bit indicates that the component uses the same physical reference clock
  that the platform provides on the connector.
  If the device uses an independent clock irrespective of the presence
  of a reference on the connector, this bit must be clear.

refname: slot_clock_cfg

-----
PARAM:   "HCA Vendor ID":
REFNAME: "hca_header_vendor_id":
  Mellanox HCA Vendor ID reported
  to system sweep process.

refname: hca_header_vendor_id

-----
PARAM:   "HCA Device ID":
REFNAME: "hca_header_device_id":
  Mellanox InfiniHost Device ID
  reported to system sweep process.

refname: hca_header_device_id

-----
PARAM:   "HCA Revision ID":
REFNAME: "hca_rev_id":
  Mellanox InfiniHost Revision ID
  reported to system sweep process.

refname: hca_rev_id
```

PARAM: "SubSystem Vendor ID":
REFNAME: "hca_header_subsystem_vendor_id":
Mellanox subsystem HCA Vendor ID
reported to system sweep process.

refname: hca_header_subsystem_vendor_id

PARAM: "SubSystem Device ID":
REFNAME: "hca_header_subsystem_id":
Mellanox subsystem HCA ID
reported to system sweep process.

refname: hca_header_subsystem_id

PARAM: "Power Management Capability Enable":
REFNAME: "pci_power_management_en":
Enable PCI Power Management Capability.
Required for PCI Express compliance.

refname: pci_power_management_en

PARAM: "Vendor Key [31:0]":
REFNAME: "v_key_31_0":
Vendor Key [31:0]

refname: v_key_31_0

PARAM: "Vendor Key [63:32]":
REFNAME: "v_key_63_32":
Vendor Key [63:32]

refname: v_key_63_32

PARAM: "MSI Capability Enable":
REFNAME: "msi_en":
Enable MSI Capability.
Support for this capability, or MSI-X capability is required for PCI Express
compliance.

refname: msi_en

PARAM: "MSI-X Capability Enable":
REFNAME: "msi_x_en":
Enable MSI-X Capability.
Support for this capability, or MSI capability is required for PCI Express compliance.

refname: msi_x_en

PARAM: "Advanced Error Reporting Capability Enable":
REFNAME: "advanced_error_reporting_en":
Enable PCI Express Advanced Error Reporting Capability.
This capability resides in PCI Express Extended Configuration Space.

refname: advanced_error_reporting_en

PARAM: "PCI Express Capability Enable":
REFNAME: "pci_express_en":
Enable PCI Express Capability.
Required for PCI Express compatibility.

refname: pci_express_en

PARAM: "Default Max Read Request Size":
REFNAME: "default_max_read_request_size":
Default value for Max_Read_Request_Size field
in the PCI Express Capability Device Control Register.
Set to 0x2 for strict PCI Express compatibility.

14:12 Max_Read_Request_Size .

This field sets the maximum Read Request size for the Device as a Requester.
The Device must not generate read requests with size exceeding the set value.
Defined encodings for this field are:

000b 128 bytes max read request size
001b 256 bytes max read request size
010b 512 bytes max read request size
011b 1024 bytes max read request size
100b 2048 bytes max read request size
101b 4096 bytes max read request size
110b Reserved
111b Reserved

Devices that do not generate Read Request larger than 128
bytes are permitted to implement this field as Read Only (ro="1")
with a value of 000b.

Default value of this field is 010b

refname: default_max_read_request_size

PARAM: "Log2 Max Read Request Size (in byte)":
REFNAME: "emt_max_outstanding_read_request_size":
Log2 of Max Read Request Size.
10 - 1Kb
11 - 2Kb
12 - 4Kb

Using larger value here will limit the number of HW engines
in use.

refname: emt_max_outstanding_read_request_size

PARAM: "Max Outstanding Read Requests":
REFNAME: "emt_max_outstanding_read_requests":
Limits the max number of outstanding read requests.

refname: emt_max_outstanding_read_requests

PARAM: "Log2 UAR Size (in pages)":
REFNAME: "db_area_size":
Log2 of Maximum Number of UARs
to be used to access the device.

refname: db_area_size

PARAM: "Log2 of System Page Size (in bytes)":
REFNAME: "page_size":
Log2 of System Page Size.

refname: page_size

PARAM: "TPT Map":
REFNAME: "tpt_cfg_xlcache_conf":
Determines the indexing method of the TPT
translation cache entries.

refname: tpt_cfg_xlcache_conf

PARAM: "SRQ enable ":
REFNAME: "srq_enable":

Disable/enable the SRQ support.

refname: srq_enable

PARAM: "Log max SRQ":
REFNAME: "log_max_srqs":
Log 2 max SRQ supported

refname: log_max_srqs

PARAM: "IEEE Vendor ID":
REFNAME: "nodeinfo_vendor_id":
Mellanox IB Vendor ID.
A part of the Node Information that may be queried
by the Subnet Manager (SM)

refname: nodeinfo_vendor_id

PARAM: "Device ID":
REFNAME: "nodeinfo_ib_dev":
Mellanox IB Device ID.
A part of the Node Information that may be
queried by the Subnet Manager (SM)

refname: nodeinfo_ib_dev

PARAM: "Revision ID":
REFNAME: "nodeinfo_ibrev_id":
HW Revision ID.
A part of the Node Information that may be queried
by the Subnet Manager (SM)

refname: nodeinfo_ibrev_id

PARAM: "Base Version":
REFNAME: "nodeinfo_base_ver":
Supported MAD Base Version.
A part of the Node Information that may be
queried by the Subnet Manager (SM).

refname: nodeinfo_base_ver

PARAM: "Class Version":
REFNAME: "nodeinfo_class_ver":
Supported Subnet Management Class Version.
A part of the Node Information that may be
queried by the Subnet Manager (SM).

refname: nodeinfo_class_ver

PARAM: "Node Type":
REFNAME: "nodeinfo_node_type":

IB Node type.
A part of the Node Information that may be queried
by the Subnet Manager (SM).

refname: nodeinfo_node_type

PARAM: "Num of Ports":
REFNAME: "nodeinfo_num_ports":
Number of operating ports.

refname: nodeinfo_num_ports

PARAM: "Log2 Partition Capability":
REFNAME: "nodeinfo_log_partition_cap":
Log 2 of Partition Table size supported by each port.
Maximum number of entries per port in InfiniHost is 64.

refname: nodeinfo_log_partition_cap

PARAM: "DD":
REFNAME: "DD":

refname: DD

PARAM: "MM":
REFNAME: "MM":

refname: MM

PARAM: "YY":
REFNAME: "YY":

refname: YY

PARAM: "-":
REFNAME: "NUM":

refname: NUM

PARAM: "Node GUID [39:32]":
REFNAME: "nodeguid_39_32":
Bits [39:32] of Mellanox HCA Node GUID
Part of the Node information that may be queried
by the Subnet Manager (SM).

refname: nodeguid_39_32

PARAM: "SystemImageGUID [39:32]":
REFNAME: "systemimageguid_39_32":
Bits [39:32] of SystemImageGUID of NodeInfo.
Enables system software to indicate the availability of
multiple paths to the same destination via multiple nodes.
Set to zero if indication of node association is not desired.

refname: systemimageguid_39_32

PARAM: "SystemImageGUID [31:0]":
REFNAME: "systemimageguid_31_0":
Lower 32 bits of SystemImageGUID of NodeInfo.
Enables system software to indicate the availability of
multiple paths to the same destination via multiple nodes.
Set to zero if indication of node association is not desired.

refname: systemimageguid_31_0

PARAM: "Node Description":
REFNAME: "node_desc":
Mellanox InfiniHost node description.
A part of the NodeDescription that may be queried
by the Subnet Manager (SM).

refname: node_desc

PARAM: "Number of Enabled Ports":
REFNAME: "num_of_ports":
Enable or Disable the InfiniHost Ports.
The Node information given by the Device
reflects port availability.

refname: num_of_ports

PARAM: "Ports Width Capability":
REFNAME: "ports_link_width_max":

PortWidth supported as defined by IB spec.
Ports may be opened as supporting either 1x, 4x or both.

refname: ports_link_width_max

PARAM: "Port1 GUID [39:32]":
REFNAME: "port1guid_39_32":
Bits [39:32] of Port Guid parameter.
The PortGUID is the first entry in the GUID table,
which may be queried by the Subnet Manager (SM).

refname: port1guid_39_32

PARAM: "Port2 GUID [39:32]":
REFNAME: "port2guid_39_32":
Bits [39:32] of Port Guid parameter.
The PortGUID is the first entry in the GUID table,
which may be queried by the Subnet Manager (SM).

refname: port2guid_39_32

PARAM: "Port1 GUID [31:0]":
REFNAME: "port1guid_31_0":
LSbits of Port Guid parameter.
Port GUID value for each port. The PortGUID is the first
entry in the GUID table, that may be queried by the Subnet Manager (SM).

refname: port1guid_31_0

PARAM: "Port2 GUID [31:0]":
REFNAME: "port2guid_31_0":
LSbits of Port Guid parameter.
Port GUID value for each port. The PortGUID is the first
entry in the GUID table, that may be queried by the Subnet Manager (SM).

refname: port2guid_31_0

PARAM: "Tx Lane Polarity":
REFNAME: "tx_lane_polarity_port1":
When set, the serial input data on lane X on this port
will be inverted. This is equivalent to flipping the
differential input of the SERDES.
Each bit relates to Lane X where X=0,1,2,3.

refname: tx_lane_polarity_port1

PARAM: "Tx Lane Polarity":
REFNAME: "tx_lane_polarity_port2":
When set, the serial input data on lane X on this port
will be inverted. This is equivalent to flipping the
differential input of the SERDES.
Each bit relates to Lane X where X=0,1,2,3.

refname: tx_lane_polarity_port2

PARAM: "Phy LED GPIO":
REFNAME: "port1_phy_led_gpio":
0-0xff : GPIO number connected to the LED
indicating physical/logical state of the port.
NOTE: if Self-Refresh is enabled, GPIO13 and
GPIO8 cannot be used.

refname: port1_phy_led_gpio

PARAM: "Phy LED GPIO":
REFNAME: "port2_phy_led_gpio":
0-0xff : GPIO number connected to the LED
indicating physical/logical state of the port
NOTE: if Self-Refresh is enabled, GPIO13 and
GPIO8 cannot be used.

refname: port2_phy_led_gpio

PARAM: "Log LED GPIO":
REFNAME: "port1_log_led_gpio":
0-0xff : GPIO number connected to the LED
indicating physical/logical state of the port
NOTE: if Self-Refresh is enabled, GPIO13 and
GPIO8 cannot be used.

refname: port1_log_led_gpio

PARAM: "Log LED GPIO":
REFNAME: "port2_log_led_gpio":
0-0xff : GPIO number connected to the LED
indicating physical/logical state of the port
NOTE: if Self-Refresh is enabled, GPIO13 and
GPIO8 cannot be used.

refname: port2_log_led_gpio

PARAM: "Disable Leds blinking":
REFNAME: "disable_leds_blink":

refname: disable_leds_blink

PARAM: "E1 Clock Divider":
REFNAME: "flash_i2c_clk":
elclk divider to read pll boot record

refname: flash_i2c_clk

PARAM: "Core N":
REFNAME: "core_n":
pll divider. ilclk will be elclk * (m/2n)
1N8
0000 = 8

refname: core_n

PARAM: "Core M":
REFNAME: "core_m":
1M16

```
0000 = 16

refname: core_m

-----
PARAM: "VCO Range":
REFNAME: "core_vco_range":
if ilclk>=133mhz, vco_range should be '1' (pll input)

refname: core_vco_range

-----
PARAM: "Bypass":
REFNAME: "core_bypass":
pll bypass. not usable here. we use the input pad

refname: core_bypass

-----
PARAM: "Lock enable":
REFNAME: "core_lock":

refname: core_lock

-----
PARAM: "Output enable":
REFNAME: "core_eout":

refname: core_eout

-----
PARAM: "DMU N":
REFNAME: "dmu_n":
1N8
0000 = 8
pll divider. dlclk will be (1+dmu_deskew) * mclkin * (m/(2-dddso)n) ..... dddso
= disable_dmu_divider strapping option

refname: dmu_n

-----
PARAM: "DMU M":
REFNAME: "dmu_m":
1M16
0000 = 16
```

```
refname: dmu_m

-----
PARAM:    "VCO Range":
REFNAME:  "dmu_vco_range":
if dlclk*2>=133mhz, vco_range should be '1' (pll input)

refname: dmu_vco_range

-----
PARAM:    "Deskew":
REFNAME:  "dmu_deskew":
deskew option to the pll

refname: dmu_deskew

-----
PARAM:    "Bypass":
REFNAME:  "dmu_bypass":
pll bypass. not usable here. we use the input pad

refname: dmu_bypass

-----
PARAM:    "Lock enable":
REFNAME:  "dmu_lock":

refname: dmu_lock

-----
PARAM:    "Output enable":
REFNAME:  "dmu_eout":

refname: dmu_eout

-----
PARAM:    "RSU Common":
REFNAME:  "r0_rsu_common":
put 0x0. mode of pll for ib clk.

refname: r0_rsu_common

-----
PARAM:    "Nref":
REFNAME:  "r0_nref":
put 0x0. ask smeloy if u want...
```

refname: r0_nref

PARAM: "PFD":
REFNAME: "r0_pfd":
put 0x0. ask smeloy if u want...

refname: r0_pfd

PARAM: "LDIV":
REFNAME: "r0_ldiv":
IB clock divider, for VRCLKP/N pin.
for serdes at 2.5Ghz ,the following frequencies are allowed for VRCLKP/N input:
if input 125MHz put 0x0,
250Mhz put 0x1,
62.5MHz put 0x2,
for 31.25MHz put 0x3,
for 100MHz put 0x4-0x7 (e.g. TGU is 100MHz, put 0x7)

refname: r0_ldiv

PARAM: "Bypass":
REFNAME: "r0_bypass":
pll bypass. not usable here. we use the input pad

refname: r0_bypass

PARAM: "Lock":
REFNAME: "r0_lock":
enable pll lock indication (enable to push it on the pad)

refname: r0_lock

PARAM: "Out":
REFNAME: "r0_eout":
enable the clock_out on the pad (refclk/2)

refname: r0_eout

PARAM: "RSU Common":
REFNAME: "t0_rsu_common":
put 0x0. mode of pll for ib clk.

```
refname: t0_rsu_common
```

```
-----
```

```
PARAM: "Nref":  
REFNAME: "t0_nref":  
put 0x0. ask smeloy if u want...
```

```
refname: t0_nref
```

```
-----
```

```
PARAM: "PFD":  
REFNAME: "t0_pfd":  
put 0x0. ask smeloy if u want...
```

```
refname: t0_pfd
```

```
-----
```

```
PARAM: "LDIV":  
REFNAME: "t0_ldiv":  
PCI Express clock divider, for XRCLKP/N.  
for serdes at 2.5Ghz ,the following frequencies are allowed for XRCLKP/N input:  
if input 125MHz put 0x0,  
    250MHz put 0x1,  
    62.5MHz put 0x2,  
    for 31.25MHz put 0x3,  
    for 100MHz put 0x4-0x7 (e.g. TGU is 100MHz, put 0x7)
```

```
refname: t0_ldiv
```

```
-----
```

```
PARAM: "Bypass":  
REFNAME: "t0_bypass":  
pll bypass. not usable here. we use the input pad
```

```
refname: t0_bypass
```

```
-----
```

```
PARAM: "Lock":  
REFNAME: "t0_lock":  
enable pll lock indication (enable to push it on the pad)
```

```
refname: t0_lock
```

```
-----
```

```
PARAM: "Out":  
REFNAME: "t0_eout":  
enable the clock_out on the pad (refclk/2)
```

refname: t0_eout

PARAM: "PLL Stabilization Time":

REFNAME: "pll_stabilize":

(1024 * pll_stabilize) is num of elclk cycles to wait for stabilization put 1.0
milisec = 1024 * 60 * elclk(66MHz) . lets put 0x80

refname: pll_stabilize

PARAM: "CCLK: Adapter Core Reference Clock (KHz)":

REFNAME: "adapter_core_ref_clock_khz":

Input core clock to PLL (KHz)

refname: adapter_core_ref_clock_khz

PARAM: "MCLK: Adapter DMU Reference Clock (KHz)":

REFNAME: "adapter_dmu_ref_clock_khz":

Input DDR Memory clock to PLL (KHz)

refname: adapter_dmu_ref_clock_khz

PARAM: "DMU Divider Disable":

REFNAME: "disable_dmu_divider":

Select if disable_dmu_divider strapping option [sdostrb] is set.

refname: disable_dmu_divider

PARAM: "Core Frequency Output":

REFNAME: "core_frequency_khz":

Core Clock Frequency Output from PLL (KHz). 125000-200000 KHz

refname: core_frequency_khz

PARAM: "DDR DRAM Frequency Output (x1)":

REFNAME: "dram_frequency_1x_khz":

On board DIMMs frequency (x1) (KHz) 80000-166000KHz

refname: dram_frequency_1x_khz

PARAM: "DDR DRAM Frequency Output (x2)":

REFNAME: "dram_frequency_2x_khz":
On board DIMMs frequency (x2) (KHz) 160000-333000KHz

refname: dram_frequency_2x_khz

PARAM: "Allowed VRCLKP/N Frequency Input":
REFNAME: "allowed_vrclkp_khz":
Allowed VRCLKP/N Frequency (KHz)

refname: allowed_vrclkp_khz

PARAM: "Allowed XRCLKP/N Frequency Input":
REFNAME: "allowed_vrclkp_tg_khz":
Allowed XRCLKP/N Frequency (KHz)

refname: allowed_vrclkp_tg_khz

PARAM: "Internal core clock must be greater than 125MHz":
REFNAME: "coreclk_gt_125mhz":
coreclk > 125 MHz

refname: coreclk_gt_125mhz

PARAM: "Coreclk must be greater than half the ddrclk":
REFNAME: "coreclk_gt_fraq_ddrclk_2":
coreclk > ddrclk/2

refname: coreclk_gt_fraq_ddrclk_2

PARAM: "Log DDR Max Size":
REFNAME: "log2_ddr_size":
Log 2 of DDR Maximum size.
DDR Maximum Size parameter enables the user to
limit the use of the attached memory (DRAM) to
less than actual size.

refname: log2_ddr_size

PARAM: "ECC Mode":
REFNAME: "ecc_mode":

Determines type of attached DIMMs EEC mode

refname: ecc_mode

PARAM: "Auto Precharge Mode":

REFNAME: "auto_precharge_mode":

Determines Auto Precharge mode

refname: auto_precharge_mode

PARAM: "Cmd Gap Rate0":

REFNAME: "cmd_gap_rate0":

Minimum gap (in clocks) between execution of 2 requests (RD or WR) from the PCI port.

For power reduction. This value affects performance.

refname: cmd_gap_rate0

PARAM: "Cmd Gap Rate1":

REFNAME: "cmd_gap_rate1":

Minimum gap (in clocks) between execution of 2 requests (RD or WR) from the HCA port.

For power reduction. This value affects performance.

refname: cmd_gap_rate1

PARAM: "Hide DDR":

REFNAME: "hide_dds_en":

Enables/disables the DDR BAR.

refname: hide_dds_en

PARAM: "DDR Address Lsb":

REFNAME: "ddr_addr_lsb":

[31:0] bits address of ddr space given by user.

refname: ddr_addr_lsb

PARAM: "DDR Address Msb":

REFNAME: "ddr_addr_msb":

[63:32] bits address of ddr space given by user.

refname: ddr_addr_msb

PARAM: "Exit SR WAITING PERIOD[DCLK]":
REFNAME: "xsr_dclk_wait":
Numer of dram clocks InfiniHost waits before exiting
after Self-Refresh has been activated.

refname: xsr_dclk_wait

PARAM: "SPD Address":
REFNAME: "SPD0_addr":
First DIMM slot address on board.
Please specify the following values:
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.
NOT PRESENT: 0x100 - DIMMs not present in any form.
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD0_addr

PARAM: "SPD Address":
REFNAME: "SPD1_addr":
Second Dimm slot address on board.
Please specify the following values:
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.
NOT PRESENT: 0x100 - DIMMs not present in any form.
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD1_addr

PARAM: "SPD offset":
REFNAME: "SPD0_offset":
first Dimm slot offset on EEPROM (valid only if address is from EEPROM).

refname: SPD0_offset

PARAM: "SPD Offset":
REFNAME: "SPD1_offset":
Second Dimm slot address EEPROM (valid only if address is from EEPROM).

refname: SPD1_offset

PARAM: "SPD 16 bit addr ":

```
REFNAME: "SPD0_width":  
First Dimm slot EEPROM address width (valid only if address is from EEPROM).  
  
refname: SPD0_width  
  
-----  
PARAM: "SPD 16 bit addr ":  
REFNAME: "SPD1_width":  
Second Dimm slot EEPROM address width (valid only if address is from EEPROM).  
  
refname: SPD1_width  
  
-----  
PARAM: "WriteOnly DIMM":  
REFNAME: "dimm0_writeonly":  
  
refname: dimm0_writeonly  
  
-----  
PARAM: "WriteOnly DIMM":  
REFNAME: "dimm1_writeonly":  
  
refname: dimm1_writeonly  
  
-----  
PARAM: "Supported Dimm Types":  
REFNAME: "dimm0_types":  
  
refname: dimm0_types  
  
-----  
PARAM: "Supported Dimm Types":  
REFNAME: "dimm1_types":  
  
refname: dimm1_types  
  
-----  
PARAM: "SPD Address":  
REFNAME: "SPD2_addr":  
Third Dimm slot address on board.  
Please specify the following values:  
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.  
NOT PRESENT: 0x100 - DIMMs not present in any form.  
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values
```

refname: SPD2_addr

PARAM: "SPD Address":

REFNAME: "SPD3_addr":

Fourth Dimm slot address on board.

Please specify the following values:

DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.

NOT PRESENT: 0x100 - DIMMs not present in any form.

SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD3_addr

PARAM: "SPD offset":

REFNAME: "SPD2_offset":

first Dimm slot offset on EEPROM (valid only if address is from EEPROM).

refname: SPD2_offset

PARAM: "SPD Offset":

REFNAME: "SPD3_offset":

Second Dimm slot address EEPROM (valid only if address is from EEPROM).

refname: SPD3_offset

PARAM: "SPD 16 bit addr ":

REFNAME: "SPD2_width":

Third Dimm slot EEPROM address width (valid only if address is from EEPROM).

refname: SPD2_width

PARAM: "SPD 16 bit addr ":

REFNAME: "SPD3_width":

Forth Dimm slot EEPROM address width (valid only if address is from EEPROM).

refname: SPD3_width

PARAM: "WriteOnly DIMM":

REFNAME: "dimm2_writeonly":

refname: dimm2_writeonly

PARAM: "WriteOnly DIMM":
REFNAME: "dimm3_writeonly":

refname: dimm3_writeonly

PARAM: "Supported Dimm Types":
REFNAME: "dimm2_types":

refname: dimm2_types

PARAM: "Supported Dimm Types":
REFNAME: "dimm3_types":

refname: dimm3_types

PARAM: "dimm0_byte0":
REFNAME: "dimm0_byte0":

refname: dimm0_byte0

PARAM: "dimm0_byte1":
REFNAME: "dimm0_byte1":

refname: dimm0_byte1

PARAM: "dimm0_byte2":
REFNAME: "dimm0_byte2":

refname: dimm0_byte2

PARAM: "dimm0_byte3":
REFNAME: "dimm0_byte3":

refname: dimm0_byte3

PARAM: "dimm0_byte4":

REFNAME: "dimm0_byte4":

refname: dimm0_byte4

PARAM: "dimm0_byte5":

REFNAME: "dimm0_byte5":

refname: dimm0_byte5

PARAM: "dimm0_byte6":

REFNAME: "dimm0_byte6":

refname: dimm0_byte6

PARAM: "dimm0_byte7":

REFNAME: "dimm0_byte7":

refname: dimm0_byte7

PARAM: "dimm0_byte8":

REFNAME: "dimm0_byte8":

refname: dimm0_byte8

PARAM: "dimm0_byte9":

REFNAME: "dimm0_byte9":

refname: dimm0_byte9

PARAM: "dimm0_byte10":

REFNAME: "dimm0_byte10":

refname: dimm0_byte10

PARAM: "dimm0_byte11":

REFNAME: "dimm0_byte11":

refname: dimm0_byte11

PARAM: "dimm0_byte12":

REFNAME: "dimm0_byte12":

refname: dimm0_byte12

PARAM: "dimm0_byte13":

REFNAME: "dimm0_byte13":

refname: dimm0_byte13

PARAM: "dimm0_byte14":

REFNAME: "dimm0_byte14":

refname: dimm0_byte14

PARAM: "dimm0_byte15":

REFNAME: "dimm0_byte15":

refname: dimm0_byte15

PARAM: "dimm0_byte16":

REFNAME: "dimm0_byte16":

refname: dimm0_byte16

PARAM: "dimm0_byte17":

REFNAME: "dimm0_byte17":

refname: dimm0_byte17

PARAM: "dimm0_byte18":

REFNAME: "dimm0_byte18":

refname: dimm0_byte18

PARAM: "dimm0_byte19":

REFNAME: "dimm0_byte19":

refname: dimm0_byte19

PARAM: "dimm0_byte20":

REFNAME: "dimm0_byte20":

refname: dimm0_byte20

PARAM: "dimm0_byte21":

REFNAME: "dimm0_byte21":

refname: dimm0_byte21

PARAM: "dimm0_byte22":

REFNAME: "dimm0_byte22":

refname: dimm0_byte22

PARAM: "dimm0_byte23":

REFNAME: "dimm0_byte23":

refname: dimm0_byte23

PARAM: "dimm0_byte24":

REFNAME: "dimm0_byte24":

refname: dimm0_byte24

PARAM: "dimm0_byte25":

REFNAME: "dimm0_byte25":

refname: dimm0_byte25

PARAM: "dimm0_byte26":

REFNAME: "dimm0_byte26":

refname: dimm0_byte26

PARAM: "dimm0_byte27":

REFNAME: "dimm0_byte27":

refname: dimm0_byte27

PARAM: "dimm0_byte28":

REFNAME: "dimm0_byte28":

refname: dimm0_byte28

PARAM: "dimm0_byte29":

REFNAME: "dimm0_byte29":

refname: dimm0_byte29

PARAM: "dimm0_byte30":

REFNAME: "dimm0_byte30":

refname: dimm0_byte30

PARAM: "dimm0_byte31":
REFNAME: "dimm0_byte31":

refname: dimm0_byte31

PARAM: "dimm0_byte32":
REFNAME: "dimm0_byte32":

refname: dimm0_byte32

PARAM: "dimm0_byte33":
REFNAME: "dimm0_byte33":

refname: dimm0_byte33

PARAM: "dimm0_byte34":
REFNAME: "dimm0_byte34":

refname: dimm0_byte34

PARAM: "dimm0_byte35":
REFNAME: "dimm0_byte35":

refname: dimm0_byte35

PARAM: "dimm0_byte36":
REFNAME: "dimm0_byte36":

refname: dimm0_byte36

PARAM: "dimm0_byte37":
REFNAME: "dimm0_byte37":

refname: dimm0_byte37

PARAM: "dimm0_byte38":
REFNAME: "dimm0_byte38":

refname: dimm0_byte38

PARAM: "dimm0_byte39":
REFNAME: "dimm0_byte39":

refname: dimm0_byte39

PARAM: "dimm0_byte40":
REFNAME: "dimm0_byte40":

refname: dimm0_byte40

PARAM: "dimm0_byte41":
REFNAME: "dimm0_byte41":

refname: dimm0_byte41

PARAM: "dimm0_byte42":
REFNAME: "dimm0_byte42":

refname: dimm0_byte42

PARAM: "dimm0_byte43":
REFNAME: "dimm0_byte43":

refname: dimm0_byte43

PARAM: "dimm0_byte44":
REFNAME: "dimm0_byte44":

refname: dimm0_byte44

PARAM: "dimm0_byte45":
REFNAME: "dimm0_byte45":

refname: dimm0_byte45

PARAM: "dimm0_byte46":
REFNAME: "dimm0_byte46":

refname: dimm0_byte46

PARAM: "dimm0_byte47":
REFNAME: "dimm0_byte47":

refname: dimm0_byte47

PARAM: "dimm0_byte48":
REFNAME: "dimm0_byte48":

refname: dimm0_byte48

PARAM: "dimm0_byte49":
REFNAME: "dimm0_byte49":

refname: dimm0_byte49

PARAM: "dimm0_byte50":
REFNAME: "dimm0_byte50":

refname: dimm0_byte50

PARAM: "dimm0_byte51":
REFNAME: "dimm0_byte51":

refname: dimm0_byte51

PARAM: "dimm0_byte52":

REFNAME: "dimm0_byte52":

refname: dimm0_byte52

PARAM: "dimm0_byte53":

REFNAME: "dimm0_byte53":

refname: dimm0_byte53

PARAM: "dimm0_byte54":

REFNAME: "dimm0_byte54":

refname: dimm0_byte54

PARAM: "dimm0_byte55":

REFNAME: "dimm0_byte55":

refname: dimm0_byte55

PARAM: "dimm0_byte56":

REFNAME: "dimm0_byte56":

refname: dimm0_byte56

PARAM: "dimm0_byte57":

REFNAME: "dimm0_byte57":

refname: dimm0_byte57

PARAM: "dimm0_byte58":

REFNAME: "dimm0_byte58":

refname: dimm0_byte58

PARAM: "dimm0_byte59":

REFNAME: "dimm0_byte59":

refname: dimm0_byte59

PARAM: "dimm0_byte60":

REFNAME: "dimm0_byte60":

refname: dimm0_byte60

PARAM: "dimm0_byte61":

REFNAME: "dimm0_byte61":

refname: dimm0_byte61

PARAM: "dimm0_byte62":

REFNAME: "dimm0_byte62":

refname: dimm0_byte62

PARAM: "dimm0_byte63":

REFNAME: "dimm0_byte63":

refname: dimm0_byte63

PARAM: "dimml_byte0":

REFNAME: "dimml_byte0":

refname: dimml_byte0

PARAM: "dimml_byte1":

REFNAME: "dimml_byte1":

refname: dimm1_byte1

PARAM: "dimm1_byte2":

REFNAME: "dimm1_byte2":

refname: dimm1_byte2

PARAM: "dimm1_byte3":

REFNAME: "dimm1_byte3":

refname: dimm1_byte3

PARAM: "dimm1_byte4":

REFNAME: "dimm1_byte4":

refname: dimm1_byte4

PARAM: "dimm1_byte5":

REFNAME: "dimm1_byte5":

refname: dimm1_byte5

PARAM: "dimm1_byte6":

REFNAME: "dimm1_byte6":

refname: dimm1_byte6

PARAM: "dimm1_byte7":

REFNAME: "dimm1_byte7":

refname: dimm1_byte7

PARAM: "dimm1_byte8":

REFNAME: "dimml_byte8":

refname: dimml_byte8

PARAM: "dimml_byte9":

REFNAME: "dimml_byte9":

refname: dimml_byte9

PARAM: "dimml_byte10":

REFNAME: "dimml_byte10":

refname: dimml_byte10

PARAM: "dimml_byte11":

REFNAME: "dimml_byte11":

refname: dimml_byte11

PARAM: "dimml_byte12":

REFNAME: "dimml_byte12":

refname: dimml_byte12

PARAM: "dimml_byte13":

REFNAME: "dimml_byte13":

refname: dimml_byte13

PARAM: "dimml_byte14":

REFNAME: "dimml_byte14":

refname: dimml_byte14

PARAM: "dimml_byte15":
REFNAME: "dimml_byte15":

refname: dimml_byte15

PARAM: "dimml_byte16":
REFNAME: "dimml_byte16":

refname: dimml_byte16

PARAM: "dimml_byte17":
REFNAME: "dimml_byte17":

refname: dimml_byte17

PARAM: "dimml_byte18":
REFNAME: "dimml_byte18":

refname: dimml_byte18

PARAM: "dimml_byte19":
REFNAME: "dimml_byte19":

refname: dimml_byte19

PARAM: "dimml_byte20":
REFNAME: "dimml_byte20":

refname: dimml_byte20

PARAM: "dimml_byte21":
REFNAME: "dimml_byte21":

refname: dimml_byte21

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PARAM: "dimml_byte22":  
REFNAME: "dimml_byte22":
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refname: dimml_byte22
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PARAM: "dimml_byte23":  
REFNAME: "dimml_byte23":
```

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refname: dimml_byte23
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PARAM: "dimml_byte24":  
REFNAME: "dimml_byte24":
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refname: dimml_byte24
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-----  
PARAM: "dimml_byte25":  
REFNAME: "dimml_byte25":
```

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refname: dimml_byte25
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-----  
PARAM: "dimml_byte26":  
REFNAME: "dimml_byte26":
```

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refname: dimml_byte26
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-----  
PARAM: "dimml_byte27":  
REFNAME: "dimml_byte27":
```

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refname: dimml_byte27
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-----  
PARAM: "dimml_byte28":  
REFNAME: "dimml_byte28":
```

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refname: dimml_byte28
```

PARAM: "dimml_byte29":
REFNAME: "dimml_byte29":

refname: dimml_byte29

PARAM: "dimml_byte30":
REFNAME: "dimml_byte30":

refname: dimml_byte30

PARAM: "dimml_byte31":
REFNAME: "dimml_byte31":

refname: dimml_byte31

PARAM: "dimml_byte32":
REFNAME: "dimml_byte32":

refname: dimml_byte32

PARAM: "dimml_byte33":
REFNAME: "dimml_byte33":

refname: dimml_byte33

PARAM: "dimml_byte34":
REFNAME: "dimml_byte34":

refname: dimml_byte34

PARAM: "dimml_byte35":
REFNAME: "dimml_byte35":

refname: dimm1_byte35

PARAM: "dimm1_byte36":

REFNAME: "dimm1_byte36":

refname: dimm1_byte36

PARAM: "dimm1_byte37":

REFNAME: "dimm1_byte37":

refname: dimm1_byte37

PARAM: "dimm1_byte38":

REFNAME: "dimm1_byte38":

refname: dimm1_byte38

PARAM: "dimm1_byte39":

REFNAME: "dimm1_byte39":

refname: dimm1_byte39

PARAM: "dimm1_byte40":

REFNAME: "dimm1_byte40":

refname: dimm1_byte40

PARAM: "dimm1_byte41":

REFNAME: "dimm1_byte41":

refname: dimm1_byte41

PARAM: "dimm1_byte42":

REFNAME: "dimm1_byte42":

refname: dimml_byte42

PARAM: "dimml_byte43":

REFNAME: "dimml_byte43":

refname: dimml_byte43

PARAM: "dimml_byte44":

REFNAME: "dimml_byte44":

refname: dimml_byte44

PARAM: "dimml_byte45":

REFNAME: "dimml_byte45":

refname: dimml_byte45

PARAM: "dimml_byte46":

REFNAME: "dimml_byte46":

refname: dimml_byte46

PARAM: "dimml_byte47":

REFNAME: "dimml_byte47":

refname: dimml_byte47

PARAM: "dimml_byte48":

REFNAME: "dimml_byte48":

refname: dimml_byte48

PARAM: "dimml_byte49":

REFNAME: "dimml_byte49":

refname: dimm1_byte49

PARAM: "dimm1_byte50":

REFNAME: "dimm1_byte50":

refname: dimm1_byte50

PARAM: "dimm1_byte51":

REFNAME: "dimm1_byte51":

refname: dimm1_byte51

PARAM: "dimm1_byte52":

REFNAME: "dimm1_byte52":

refname: dimm1_byte52

PARAM: "dimm1_byte53":

REFNAME: "dimm1_byte53":

refname: dimm1_byte53

PARAM: "dimm1_byte54":

REFNAME: "dimm1_byte54":

refname: dimm1_byte54

PARAM: "dimm1_byte55":

REFNAME: "dimm1_byte55":

refname: dimm1_byte55

PARAM: "dimm1_byte56":

REFNAME: "dimml_byte56":

refname: dimml_byte56

PARAM: "dimml_byte57":

REFNAME: "dimml_byte57":

refname: dimml_byte57

PARAM: "dimml_byte58":

REFNAME: "dimml_byte58":

refname: dimml_byte58

PARAM: "dimml_byte59":

REFNAME: "dimml_byte59":

refname: dimml_byte59

PARAM: "dimml_byte60":

REFNAME: "dimml_byte60":

refname: dimml_byte60

PARAM: "dimml_byte61":

REFNAME: "dimml_byte61":

refname: dimml_byte61

PARAM: "dimml_byte62":

REFNAME: "dimml_byte62":

refname: dimml_byte62

```
PARAM: "dimm1_byte63":  
REFNAME: "dimm1_byte63":
```

```
refname: dimm1_byte63
```

```
-----
```

```
PARAM: "dimm2_byte0":  
REFNAME: "dimm2_byte0":
```

```
refname: dimm2_byte0
```

```
-----
```

```
PARAM: "dimm2_byte1":  
REFNAME: "dimm2_byte1":
```

```
refname: dimm2_byte1
```

```
-----
```

```
PARAM: "dimm2_byte2":  
REFNAME: "dimm2_byte2":
```

```
refname: dimm2_byte2
```

```
-----
```

```
PARAM: "dimm2_byte3":  
REFNAME: "dimm2_byte3":
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refname: dimm2_byte3
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```
PARAM: "dimm2_byte4":  
REFNAME: "dimm2_byte4":
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refname: dimm2_byte4
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PARAM: "dimm2_byte5":  
REFNAME: "dimm2_byte5":
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refname: dimm2_byte5
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PARAM: "dimm2_byte6":  
REFNAME: "dimm2_byte6":
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refname: dimm2_byte6
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PARAM: "dimm2_byte7":  
REFNAME: "dimm2_byte7":
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refname: dimm2_byte7
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PARAM: "dimm2_byte8":  
REFNAME: "dimm2_byte8":
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refname: dimm2_byte8
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PARAM: "dimm2_byte9":  
REFNAME: "dimm2_byte9":
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-----  
PARAM: "dimm2_byte10":  
REFNAME: "dimm2_byte10":
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refname: dimm2_byte10
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PARAM: "dimm2_byte11":  
REFNAME: "dimm2_byte11":
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refname: dimm2_byte11
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PARAM: "dimm2_byte12":  
REFNAME: "dimm2_byte12":
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```
refname: dimm2_byte12
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PARAM: "dimm2_byte13":
REFNAME: "dimm2_byte13":

refname: dimm2_byte13

PARAM: "dimm2_byte14":
REFNAME: "dimm2_byte14":

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REFNAME: "dimm2_byte15":

refname: dimm2_byte15

PARAM: "dimm2_byte16":
REFNAME: "dimm2_byte16":

refname: dimm2_byte16

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REFNAME: "dimm2_byte18":

refname: dimm2_byte18

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REFNAME: "dimm2_byte19":

refname: dimm2_byte19

PARAM: "dimm2_byte20":

REFNAME: "dimm2_byte20":

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refname: dimm2_byte33

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refname: dimm2_byte34

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REFNAME: "dimm2_byte45":

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REFNAME: "dimm2_byte46":

refname: dimm2_byte46

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REFNAME: "dimm2_byte47":

refname: dimm2_byte47

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REFNAME: "dimm2_byte48":

refname: dimm2_byte48

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REFNAME: "dimm2_byte49":

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REFNAME: "dimm2_byte52":

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REFNAME: "dimm2_byte53":

refname: dimm2_byte53

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PARAM: "dimm2_byte54":  
REFNAME: "dimm2_byte54":
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refname: dimm2_byte54
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PARAM: "dimm2_byte55":  
REFNAME: "dimm2_byte55":
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refname: dimm2_byte55
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PARAM: "dimm2_byte56":  
REFNAME: "dimm2_byte56":
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refname: dimm2_byte56
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PARAM: "dimm2_byte57":  
REFNAME: "dimm2_byte57":
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refname: dimm2_byte57
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PARAM: "dimm2_byte58":  
REFNAME: "dimm2_byte58":
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refname: dimm2_byte58
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PARAM: "dimm2_byte59":  
REFNAME: "dimm2_byte59":
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refname: dimm2_byte59
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PARAM: "dimm2_byte60":  
REFNAME: "dimm2_byte60":
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refname: dimm2_byte60
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PARAM: "dimm2_byte61":
REFNAME: "dimm2_byte61":

refname: dimm2_byte61

PARAM: "dimm2_byte62":
REFNAME: "dimm2_byte62":

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PARAM: "dimm2_byte63":
REFNAME: "dimm2_byte63":

refname: dimm2_byte63

PARAM: "dimm3_byte0":
REFNAME: "dimm3_byte0":

refname: dimm3_byte0

PARAM: "dimm3_byte1":
REFNAME: "dimm3_byte1":

refname: dimm3_byte1

PARAM: "dimm3_byte2":
REFNAME: "dimm3_byte2":

refname: dimm3_byte2

PARAM: "dimm3_byte3":
REFNAME: "dimm3_byte3":

refname: dimm3_byte3

PARAM: "dimm3_byte4":

REFNAME: "dimm3_byte4":

refname: dimm3_byte4

PARAM: "dimm3_byte5":

REFNAME: "dimm3_byte5":

refname: dimm3_byte5

PARAM: "dimm3_byte6":

REFNAME: "dimm3_byte6":

refname: dimm3_byte6

PARAM: "dimm3_byte7":

REFNAME: "dimm3_byte7":

refname: dimm3_byte7

PARAM: "dimm3_byte8":

REFNAME: "dimm3_byte8":

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PARAM: "dimm3_byte9":

REFNAME: "dimm3_byte9":

refname: dimm3_byte9

PARAM: "dimm3_byte10":

REFNAME: "dimm3_byte10":

refname: dimm3_byte10

PARAM: "dimm3_byte11":

REFNAME: "dimm3_byte11":

refname: dimm3_byte11

PARAM: "dimm3_byte12":

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REFNAME: "dimm3_byte52":

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REFNAME: "dimm3_byte61":

refname: dimm3_byte61

PARAM: "dimm3_byte62":

REFNAME: "dimm3_byte62":

refname: dimm3_byte62

PARAM: "dimm3_byte63":

REFNAME: "dimm3_byte63":

refname: dimm3_byte63

PARAM: "FW Size in DDR":

REFNAME: "fw_length":

Log2 of DDR memory allocated for InifniHost FW (Bytes).

This memory area should not be accessed by any external device (see PRM restrictions).

refname: fw_length

PARAM: "FW Trace Buffer Size (MB)":
REFNAME: "total_trace_buf_sz_mb":
Trace Buffer size for all iRISCs. The Trace buffer
is divided to six parts - one for each iRISC.
The trace buffer resides in DDR memory. Its allocation is
in addition to FW required length.

refname: total_trace_buf_sz_mb

PARAM: "Disable Vendor Specific MADs":
REFNAME: "vendor_specific_sup":
Enable/disable Vendor specific MAD support

refname: vendor_specific_s

PARAM: "Port1 SerDes0 OBPreAmp"
REFNAME: "port1_sd0_OBPreAmp"

PARAM="Port1 SerDes1 OBPreAmp"
refname="port1_sd1_OBPreAmp"

PARAM="Port1 SerDes2 OBPreAmp"
refname="port1_sd2_OBPreAmp"

PARAM="Port1 SerDes3 OBPreAmp"
refname="port1_sd3_OBPreAmp"

PARAM="Port2 SerDes0 OBPreAmp"
refname="port2_sd0_OBPreAmp"

PARAM="Port2 SerDes1 OBPreAmp"
refname="port2_sd1_OBPreAmp"

PARAM="Port2 SerDes2 OBPreAmp"
refname="port2_sd2_OBPreAmp"

PARAM="Port2 SerDes3 OBPreAmp"
refname="port2_sd3_OBPreAmp"

PARAM="Port1 SerDes0 OBVoltage"
refname="port1_sd0_OBVoltage"

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-----  
PARAM="Port1 SerDes1 OBVoltage"  
refname="port1_sd1_OBVoltage"  
  
-----  
PARAM="Port1 SerDes2 OBVoltage"  
refname="port1_sd2_OBVoltage"  
  
-----  
PARAM="Port1 SerDes3 OBVoltage"  
refname="port1_sd3_OBVoltage"  
  
-----  
PARAM="Port2 SerDes0 OBVoltage"  
refname="port2_sd0_OBVoltage"  
  
-----  
PARAM="Port2 SerDes1 OBVoltage"  
refname="port2_sd1_OBVoltage"  
  
-----  
PARAM="Port2 SerDes2 OBVoltage"  
refname="port2_sd2_OBVoltage"  
  
-----  
PARAM="Port2 SerDes3 OBVoltage"  
refname="port2_sd3_OBVoltage"  
  
-----  
PARAM="Port1 SerDes0 OBPreEmpPreAmp"  
refname="port1_sd0_OBPreEmpPreAmp"  
  
-----  
PARAM="Port1 SerDes1 OBPreEmpPreAmp"  
refname="port1_sd1_OBPreEmpPreAmp"  
  
-----  
PARAM="Port1 SerDes2 OBPreEmpPreAmp"  
refname="port1_sd2_OBPreEmpPreAmp"  
  
-----  
PARAM="Port1 SerDes3 OBPreEmpPreAmp"  
refname="port1_sd3_OBPreEmpPreAmp"  
  
-----  
PARAM="Port2 SerDes0 OBPreEmpPreAmp"  
refname="port2_sd0_OBPreEmpPreAmp"  
  
-----  
PARAM="Port2 SerDes1 OBPreEmpPreAmp"  
refname="port2_sd1_OBPreEmpPreAmp"  
  
-----  
PARAM="Port2 SerDes2 OBPreEmpPreAmp"
```

```
refname="port2_sd2_OBPreEmpPreAmp"

-----
PARAM="Port2 SerDes3 OBPreEmpPreAmp"
refname="port2_sd3_OBPreEmpPreAmp"

-----
PARAM="Port1 SerDes0 OBPreEmpOut"
refname="port1_sd0_OBPreEmpOut"

-----
PARAM="Port1 SerDes1 OBPreEmpOut"
refname="port1_sd1_OBPreEmpOut"

-----
PARAM="Port1 SerDes2 OBPreEmpOut"
refname="port1_sd2_OBPreEmpOut"

-----
PARAM="Port1 SerDes3 OBPreEmpOut"
refname="port1_sd3_OBPreEmpOut"

-----
PARAM="Port2 SerDes0 OBPreEmpOut"
refname="port2_sd0_OBPreEmpOut"

-----
PARAM="Port2 SerDes1 OBPreEmpOut"
refname="port2_sd1_OBPreEmpOut"

-----
PARAM="Port2 SerDes2 OBPreEmpOut"
refname="port2_sd2_OBPreEmpOut"

-----
PARAM="Port2 SerDes3 OBPreEmpOut"
refname="port2_sd3_OBPreEmpOut"

-----
PARAM="Port1 SerDes0 RX Equalization"
refname="port1_sd0_Equal"

-----
PARAM="Port1 SerDes1 RX Equalization"
refname="port1_sd1_Equal"

-----
PARAM="Port1 SerDes2 RX Equalization"
refname="port1_sd2_Equal"

-----
PARAM="Port1 SerDes3 RX Equalization"
refname="port1_sd3_Equal"
```

```
-----  
PARAM="Port2 SerDes0 RX Equalization"  
refname="port2_sd0_Equal"
```

```
-----  
PARAM="Port2 SerDes1 RX Equalization"  
refname="port2_sd1_Equal"
```

```
-----  
PARAM="Port2 SerDes2 RX Equalization"  
refname="port2_sd2_Equal"
```

```
-----  
PARAM="Port2 SerDes3 RX Equalization"  
refname="port2_sd3_Equal"
```

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