Release Notes

MT23108 InfiniHost Firmware

FW-23108 Rev 3.3.2

MT23108 InfiniHost Firmware Release Notes

Document Number:

Mellanox Technologies, Inc.
2900 Stender Way
Santa Clara, CA 95054
U.S.A.
www.Mellanox.com

Tel: (408) 970-3400
Fax: (408) 970-3403

Mellanox Technologies Ltd
PO Box 586 Hermon Building
Yokneam 20692
Israel

Tel: +972-4-909-7200
Fax: +972-4-959-3245

1 Overview

This document describes the contents of the FW-23108 Rev 3.3.2 release of InfiniHost firmware. The document consists of the following sections:

2 Major New Features

None

3 Fixes for Known Issues

The following table describes known issues of InfiniHost firmware that are fixed in this firmware release.

Table 1 - Fixed Known Issues

Issue	Description	Discovered in	Fixed in
Consumer Index corruption in a Completion Queue	When using Increment_CI doorbells, to increment the CI in more than 1, CI may advance wrongly, casing a false CQ overrun, or not detecting a real overrun (ID: 27893)	3.3.1	3.3.2

4 Known Issues

The following table describes known issues in this firmware release and possible workarounds.

Table 2 - Known Issues

Issue	Description	Current Implemented Workaround in FW	Possible Workaround in Driver	Patch Release (fix)	Scheduled Release (fix)
MSIx vectors	Writing to MSIx vectors (Address/Data/Mask) does not take immediate effect. There may be MSIx messages that leave the device according to the old vector.	NA	NA	NA	NA
QPC.Flight_LIM	QPC field – no HW limit, infinite WQEs on send.	NA	NA	NA	NA
QUERY_DDR	Query does not return JEDEC vendor ID yet. Scope of status is limited to active / not active.	NA	NA	NA	NA
RTR2RTS_QPEE; SQD2RTS_QPEE: changing optional fields rra_max and ra_buf_index is not supported.	The optional fields rra_max and ra_buf_index are not supported in the RTR2RTS_QPEE and SQD2TRS_QPEE commands.	Change requests for these fields do not take effect, and no error indication is provided.	Mask these optional fields.	NA	NA
PCI 2.3 control and status for interrupts	InfiniHost does not support PCI2.3 control and status bits for interrupts.	NA	NA	NA	NA
SW reset in memory controller mode	On PCIX systems with the bus downgraded to PCI: When the Flash image is corrupted and InfiniHost comes up as a memory controller and the I2C connector is attached, a SW reset may hang the system.	NA	1. Reboot the system. 2. Disconnect I2C when issuing a SW reset.	NA	NA
Config cycles during sys_en	PCIX cfg cycles issued while the system-enable command is in progress may take a long time to complete. This causes some ServerWork chipsets to time-out and hang the system.	NA	Do not issue config cycles during a sys_en command.	NA	NA

4.1 PRM (v1.0) Changes not yet Supported

The following features are not scheduled to be supported:

1. Flight lim value in QPC may show a value other than 0’1111, though it is unlimited usage.

5 IS Changes / Fixes

Issue	Description	DIscovered in	Fixed in
FailSafe failure report	Corruption of FW image in NVRAM does not result in a correct PCI cfg syndrome in register 20 as required. (ID:15912)	1.16.0000	1.18.0000
Header corruption on boot2 section.	If one of the first two words in the image is corrupted to 0, FailSafe code cannot recover nor answer configuration cycles.(ID:16181)	1.16.0000	1.18.0000
IS memory controller non-PCIX compliant	On PCIX systems, when InfiniHost comes up as a memory controller, a SW reset may hang the system.(ID:16181)	1.16.0000	1.18.0000
FailSafe when two images are damaged	In Failsafe mode, when both the primary and secondary images are damaged, InfiniHost does not come up as a memory controller.	1.16.0000	1.16.0008

6 Appendix: InfiniHost FW parameters with “refnames”

PARAM: "Adapter Vendor ID":
REFNAME: "adapter_vendor_id":
Adapter Vendor ID reported to QUERY_ADAPTER query by Driver

refname: adapter_vendor_id

PARAM: "Adapter Device ID":
REFNAME: "adapter_dev_id":
Adapter Device ID reported to QUERY_ADAPTER query by Driver

refname: adapter_dev_id

PARAM: "Adapter Revision ID":
REFNAME: "adapter_rev_id":
Adapter Revision ID reported to QUERY_ADAPTER query by Driver

refname: adapter_rev_id

PARAM: "Adapter VSD":
REFNAME: "adapter_vsd":
Vendor Specific Data on flash

refname: adapter_vsd

PARAM: "PSID":
REFNAME: "PSID":
Parameter Set IDentification

refname: PSID

PARAM: "Adapter I2C Slave Address":
REFNAME: "adapt_i2c_slv_addr":
Adapter I2C Slave Address

refname: adapt_i2c_slv_addr

PARAM: "Adapter I2C Slave Enable":
REFNAME: "adapt_i2c_slv_ena":
Enables/disables I2C Slave

refname: adapt_i2c_slv_ena

PARAM: "Adapter DRAM and Core Reference Clock (KHz)":
REFNAME: "adapter_ref_clock_khz":
Adapter DRAM and Core Reference clock (KHz)

refname: adapter_ref_clock_khz

PARAM: "INTA# Pin ID":
REFNAME: "INTA":
Device GPIO pin number which is connected
to INTA# on the adapter. If INTO# pin is
connected to INTA#, set value to 63.

refname: INTA

PARAM: "INTB# Pin ID":
REFNAME: "INTB":
Device GPIO pin number which is connected
to INTB# on the adapter.

refname: INTB

PARAM: "INTC# Pin ID":
REFNAME: "INTC":
Device GPIO pin number which is connected
to INTC# on the adapter.

refname: INTC

PARAM: "INTD# Pin ID":
REFNAME: "INTD":
Device GPIO pin number which is connected
to INTD# on the adapter.

refname: INTD

PARAM: "SERR":
REFNAME: "report_catastrophic_error_serr":
Enables/Disables the pulling of SERR
interrupt pin upon catastrophic error.

refname: report_catastrophic_error_serr

PARAM: "INTO":
REFNAME: "report_catastrophic_error_into":
Enables/Disables the pulling of INTO
interrupt pin upon catastrophic error.

refname: report_catastrophic_error_into

PARAM: "INTB":
REFNAME: "report_catastrophic_error_intb":
Enables/Disables the pulling of INTB
interrupt pin upon catastrophic error.

refname: report_catastrophic_error_intb

PARAM: "SERR":
REFNAME: "unreport_catastrophic_error_serr":
Enables/Disables the pulling of SERR
interrupt pin upon catastrophic error.

refname: unreport_catastrophic_error_serr

PARAM: "INTO":
REFNAME: "unreport_catastrophic_error_into":
Enables/Disables the pulling of INTO
interrupt pin upon catastrophic error.

refname: unreport_catastrophic_error_into

PARAM: "INTB":
REFNAME: "unreport_catastrophic_error_intb":
Enables/Disables the pulling of INTB
interrupt pin upon catastrophic error.

refname: unreport_catastrophic_error_intb

PARAM: "Full/Half Swing":
REFNAME: "port1_full_half_swing":

Sets the port to half or full swing

refname: port1_full_half_swing

PARAM: "Full/Half Swing":
REFNAME: "port2_full_half_swing":

Sets the port to port half or full swing

refname: port2_full_half_swing

PARAM: "Tx Pre Emphasis":
REFNAME: "port1_tx_emp_en":

Enables/disables the Pre Emphasis amplifier

refname: port1_tx_emp_en

PARAM: "Tx Pre Emphasis":
REFNAME: "port2_tx_emp_en":

Enables/disables the Pre Emphasis amplifier

refname: port2_tx_emp_en

PARAM: "Enable Equalization":
REFNAME: "port1_equ_en":

Enables/disables the equalization

refname: port1_equ_en

PARAM: "Enable Equalization":
REFNAME: "port2_equ_en":

Enables/disables the equalization

refname: port2_equ_en

PARAM: "Interrupt Coalescing Delay":
REFNAME: "int_coalsing_delay":
Min delay between two consecutive interrupts generated by HCA (in clock units)

refname: int_coalsing_delay

PARAM: "Expansion ROM Enable":
REFNAME: "exp_rom_en":
Enable Expansion ROM BAR.

refname: exp_rom_en

PARAM: "VPD Enable":
REFNAME: "vpd_enable":
Disable/enable the VPD support

refname: vpd_enable

PARAM: "VPD size":
REFNAME: "vpd_size":
VPD size in bytes.

refname: vpd_size

PARAM: "Log2 VPD EEPROM size":
REFNAME: "log2_vpd_eeprom_size":
size of each one of EEPROM slaves of the VPD

refname: log2_vpd_eeprom_size

PARAM: "Num of VPD EEPROMs":
REFNAME: "vpd_num_of_eeproms":
number of EEPROM slaves that contain the VPD

refname: vpd_num_of_eeproms

PARAM: "VPD EEPROM addr":
REFNAME: "vpd_address":
i2c slave address of EEPROM. (first EEPROM if there are multiple addresses. Other EEPROM’s i2c addresses are successive.

refname: vpd_address

PARAM: "VPD EEPROM offset":
REFNAME: "vpd_offset":
offset in EEPROM.

refname: vpd_offset

PARAM: "VPD i2c width 16 bits":
REFNAME: "vpd_i2c_16bit":
i2c bit width is 16 bits (rather than 8 bits)

refname: vpd_i2c_16bit

PARAM: "HCA Vendor ID":
REFNAME: "hca_header_vendor_id":
Mellanox HCA Vendor ID reported
to system sweep process.

refname: hca_header_vendor_id

PARAM: "HCA Device ID":
REFNAME: "hca_header_device_id":
Mellanox InfiniHost Device ID
reported to system sweep process.

refname: hca_header_device_id

PARAM: "HCA Revision ID":
REFNAME: "hca_rev_id":
Mellanox InfiniHost Revision ID
reported to system sweep process.

refname: hca_rev_id

PARAM: "SubSystem Vendor ID":
REFNAME: "hca_header_subsystem_vendor_id":
Mellanox subsystem HCA Vendor ID
reported to system sweep process.

refname: hca_header_subsystem_vendor_id

PARAM: "SubSystem Device ID":
REFNAME: "hca_header_subsystem_id":
Mellanox subsystem HCA ID
reported to system sweep process.

refname: hca_header_subsystem_id

PARAM: "HCA 66 MHZ Capable":
REFNAME: "hca_66mhz_capable":
Mellanox HCA support of 66 MHZ reported to system sweep process.

refname: hca_66mhz_capable

PARAM: "Log2 UAR Size (in pages)":
REFNAME: "db_area_size":
Log2 of Maximum Number of UARs
to be used to access the device.

refname: db_area_size

PARAM: "Log2 of System Page Size":
REFNAME: "page_size":
Log2 of Page size of both the System and
the internal North Switch bus on the InfiniHost device.

refname: page_size

PARAM: "SRQ enable ":
REFNAME: "srq_enable":
Disable/enable the SRQ support.

refname: srq_enable

PARAM: "Log max SRQ":
REFNAME: "log_max_srqs":
Log 2 max SRQ supported

refname: log_max_srqs

PARAM: "IEEE Vendor ID":
REFNAME: "nodeinfo_vendor_id":
Mellanox IB Vendor ID.
A part of the Node Information that may be queried
by the Subnet Manager (SM)

refname: nodeinfo_vendor_id

PARAM: "Device ID":
REFNAME: "nodeinfo_ib_dev":
Mellanox IB Device ID.
A part of the Node Information that may be
queried by the Subnet Manager (SM)

refname: nodeinfo_ib_dev

PARAM: "Revision ID":
REFNAME: "nodeinfo_ibrev_id":
HW Revision ID.
A part of the Node Information that may be queried
by the Subnet Manager (SM)

refname: nodeinfo_ibrev_id

PARAM: "Base Version":
REFNAME: "nodeinfo_base_ver":
Supported MAD Base Version.
A part of the Node Information that may be
queried by the Subnet Manager (SM).

refname: nodeinfo_base_ver

PARAM: "Class Version":
REFNAME: "nodeinfo_class_ver":
Supported Subnet Management Class Version.
A part of the Node Information that may be
queried by the Subnet Manager (SM).

refname: nodeinfo_class_ver

PARAM: "Node Type":
REFNAME: "nodeinfo_node_type":

IB Node type.
A part of the Node Information that may be queried
by the Subnet Manager (SM).

refname: nodeinfo_node_type

PARAM: "Num of Ports":
REFNAME: "nodeinfo_num_ports":
Number of operating ports.

refname: nodeinfo_num_ports

PARAM: "Log2 Partition Capability":
REFNAME: "nodeinfo_log_partition_cap":
Log 2 of Partition Table size supported by each port.
Maximum number of entries per port in InfiniHost is 64.

refname: nodeinfo_log_partition_cap

PARAM: "DD":
REFNAME: "DD":

refname: DD

PARAM: "MM":
REFNAME: "MM":

refname: MM

PARAM: "YY":
REFNAME: "YY":

refname: YY

PARAM: "-":
REFNAME: "NUM":

refname: NUM

PARAM: "Node GUID [39:32]":

REFNAME: "nodeguid_39_32":
Bits [39:32] of Mellanox HCA Node GUID
Part of the Node information that may be queried
by the Subnet Manager (SM).

refname: nodeguid_39_32

PARAM: "SystemImageGUID [39:32]":
REFNAME: "systemimageguid_39_32":
Bits [39:32] of SystemImageGUID of NodeInfo.
Enables system software to indicate the availability of
multiple paths to the same destination via multiple nodes.
Set to zero if indication of node association is not desired.

refname: systemimageguid_39_32

PARAM: "SystemImageGUID [31:0]":
REFNAME: "systemimageguid_31_0":
Lower 32 bits of SystemImageGUID of NodeInfo.
Enables system software to indicate the availability of
multiple paths to the same destination via multiple nodes.
Set to zero if indication of node association is not desired.

refname: systemimageguid_31_0

PARAM: "Node Description":
REFNAME: "node_desc":
Mellanox InfiniHost node description.
A part of the NodeDescription that may be queried
by the Subnet Manager (SM).

refname: node_desc

PARAM: "Number of Enabled Ports":
REFNAME: "num_of_ports":
Enable or Disable the InfiniHost Ports.
The Node information given by the Device
reflects port availability.

refname: num_of_ports

PARAM: "Ports Width Capability":
REFNAME: "ports_link_width_max":

PortWidth supported as defined by IB spec.
Ports may be opened as supporting either 1x, 4x or both.

refname: ports_link_width_max

PARAM: "Port1 GUID [39:32]":
REFNAME: "port1guid_39_32":
Bits [39:32] of Port Guid parameter.
The PortGUID is the first entry in the GUID table,
which may be queried by the Subnet Manager (SM).

refname: port1guid_39_32

PARAM: "Port2 GUID [39:32]":
REFNAME: "port2guid_39_32":
Bits [39:32] of Port Guid parameter.
The PortGUID is the first entry in the GUID table,
which may be queried by the Subnet Manager (SM).

refname: port2guid_39_32

PARAM: "Port1 GUID [31:0]":
REFNAME: "port1guid_31_0":
LSbits of Port Guid parameter.
Port GUID value for each port. The PortGUID is the first
entry in the GUID table, that may be queried by the Subnet Manager (SM).

refname: port1guid_31_0

PARAM: "Port2 GUID [31:0]":
REFNAME: "port2guid_31_0":
LSbits of Port Guid parameter.
Port GUID value for each port. The PortGUID is the first
entry in the GUID table, that may be queried by the Subnet Manager (SM).

refname: port2guid_31_0

PARAM: "Tx Lane Polarity":
REFNAME: "tx_lane_polarity_port1":
When set, the serial input data on lane X on this port
will be inverted. This is equivalent to flipping the
differential input of the SERDES.
Each bit relates to Lane X where X=0,1,2,3.

refname: tx_lane_polarity_port1

PARAM: "Tx Lane Polarity":
REFNAME: "tx_lane_polarity_port2":
When set, the serial input data on lane X on this port
will be inverted. This is equivalent to flipping the
differential input of the SERDES.
Each bit relates to Lane X where X=0,1,2,3.

refname: tx_lane_polarity_port2

PARAM: "Rx Lane Polarity":
REFNAME: "rx_lane_polarity_port1":
When set, the serial input data on lane X on this port will be inverted. This is equivalent to flipping the differential input of the SERDES.
Each bit relates to Lane X where X=0,1,2,3.

refname: rx_lane_polarity_port1

PARAM: "Rx Lane Polarity":
REFNAME: "rx_lane_polarity_port2":
When set, the serial input data on lane X on this port will be inverted. This is equivalent to flipping the differential input of the SERDES.
Each bit relates to Lane X where X=0,1,2,3.

refname: rx_lane_polarity_port2

PARAM: "Tx Lane Reverse":
REFNAME: "tx_rev_lane_port1":
When set, the serial input data on lane X on this port will be reversed.
Each bit relates to Lane X where X=0,1,2,3.

refname: tx_rev_lane_port1

PARAM: "Tx Lane Reverse":
REFNAME: "tx_rev_lane_port2":
When set, the serial input data on lane X on this port will be reversed.
Each bit relates to Lane X where X=0,1,2,3.

refname: tx_rev_lane_port2

PARAM: "Rx Lane Reverse":
REFNAME: "rx_rev_lane_port1":
When set, the serial input data on lane X on this port will be reversed.
Each bit relates to Lane X where X=0,1,2,3.

refname: rx_rev_lane_port1

PARAM: "Rx Lane Reverse":
REFNAME: "rx_rev_lane_port2":
When set, the serial input data on lane X on this port will be reversed.

Each bit relates to Lane X where X=0,1,2,3.

refname: rx_rev_lane_port2

PARAM: "Phy LED GPIO":
REFNAME: "port1_phy_led_gpio":
0-0xff : GPIO number connected to the LED indicating physical/logical state of the port.
NOTE: if Self-Refresh is enabled, GPIO13 and GPIO8 cannot be used.

refname: port1_phy_led_gpio

PARAM: "Phy LED GPIO":
REFNAME: "port2_phy_led_gpio":
0-0xff : GPIO number connected to the LED indicating physical/logical state of the port
NOTE: if Self-Refresh is enabled, GPIO13 and GPIO8 cannot be used.

refname: port2_phy_led_gpio

PARAM: "Log LED GPIO":
REFNAME: "port1_log_led_gpio":
0-0xff : GPIO number connected to the LED indicating physical/logical state of the port
NOTE: if Self-Refresh is enabled, GPIO13 and GPIO8 cannot be used.

refname: port1_log_led_gpio

PARAM: "Log LED GPIO":
REFNAME: "port2_log_led_gpio":
0-0xff : GPIO number connected to the LED indicating physical/logical state of the port
NOTE: if Self-Refresh is enabled, GPIO13 and GPIO8 cannot be used.

refname: port2_log_led_gpio

PARAM: "Disable LEDS blinking":
REFNAME: "disable_leds_blink":

refname: disable_leds_blink

PARAM: "Bridge Device Enable":
REFNAME: "bridge_en":

Enable Bridge Device operation. UAR and DDR bars must be the same size
and be adjacent for HCA to work with bridge disabled.

refname: bridge_en

PARAM: "PCIX Bridge Vendor ID":
REFNAME: "bridge_header_vendor_id":
Mellanox PCIX Bridge Vendor ID reported to system sweep process.

refname: bridge_header_vendor_id

PARAM: "PCIX Bridge Device ID":
REFNAME: "bridge_header_device_id":
Mellanox PCIX Bridge Device ID reported to system sweep process.

refname: bridge_header_device_id

PARAM: "PCIX Bridge Revision ID":
REFNAME: "pcu_rev_id":
Mellanox PCIX Bridge Revision ID reported to system sweep process.

refname: pcu_rev_id

PARAM: "PCIX Bridge 66 MHZ capable":
REFNAME: "pcu_66mhz_capable":
Mellanox Bridge PCIX support of 66 MHZ reported to system sweep process.

refname: pcu_66mhz_capable

PARAM: "PCIX Bridge new Capability List Enable":
REFNAME: "pcu_new_capability_list":
Mellanox PCIX Bridge support for new capability list reported to system sweep process.

refname: pcu_new_capability_list

PARAM: "PCI Max Outstanding Reads":
REFNAME: "max_outstanding_split_trans":

(This register was previously called PCI Max outstanding Reads on the PCI bridge).
This setting affects the
Designed Maximum Outstanding Split Transactions register
in the PCI-X Status Register,
and the reset value of the Maximum Outstanding Split Transactions Register
in the PCI-X Command Register.
For best performance, select a value 0-6, and let the software tune the value
in the Maximum Outstanding Split Transactions register.
Select the value 7 for backwards compatibility.
Register Maximum Outstanding

0 1
1 2
2 3
3 4
4 8
5 12
6 16
7 compatibility mode

refname: max_outstanding_split_trans

PARAM: "PCI-X Max Memory Read ByteCount.":
REFNAME: "hca_max_mem_r_bc":
Initial value for PCI-X Maximum Memory Read ByteCount Register
(in PCI-X Command Register) .
Set to 4 for backwards compatibility.
Set to 0 for strict PCI-X compliance.
Register Maximum Byte Count
0 512
1 1024
2 2048
3 4096
4 4096, the register is read-only

refname: hca_max_mem_r_bc

PARAM: "Non-Prefetchable Bar Type: 64/32 bit":
REFNAME: "non_prefetchable_bar_type":

Option to make a non-prefetchable bar in HCA 32 bit (type 00).
For Bridge-less configurations only.

refname: non_prefetchable_bar_type

PARAM: "SHRIMP Device Enable":
REFNAME: "shrimp_en":
Enable SHRIMP device operation.

refname: shrimp_en

PARAM: "Clock Rate Divider":
REFNAME: "cr_div":
When EEPROM/Flash present, set the desired serial clock rate
for reading the remaining part of a PLL configuration record.

refname: cr_div

PARAM: "Bypass":
REFNAME: "pllc_bp":

When set, the PLL Core clock is bypassed.
Used only in special debug modes.

refname: pllc_bp

PARAM: "Output Enable #":
REFNAME: "pllc_oe":
When selected, disables core clock output; when cleared, enables core clock output.

refname: pllc_oe

PARAM: "Enable Testing Signal Out":
REFNAME: "ecout":
Enables testing signal out, in order to sample core
clock signal on the board through a dedicated pin.
The sampled signal is half of the output frequency.

refname: ecout

PARAM: "Output Divider (OD)":
REFNAME: "pllc_od":
Divider used to calculate board core clock.

refname: pllc_od

PARAM: "Divider Denominator (R)":
REFNAME: "pllc_r":
Divider Denominator used to calculate board core clock.

refname: pllc_r

PARAM: "Divider Numerator (F)":
REFNAME: "pllc_f":
Divider Numerator used to
calculate board core clock.

refname: pllc_f

PARAM: "Frequency Output":
REFNAME: "board_frequency":
Core Clock that is pushed into the InfiniHost.

refname: board_frequency

PARAM: "Bypass":
REFNAME: "plld_bp":
When set, the DMU clock is bypassed.

Used only in special debug modes.

refname: plld_bp

PARAM: "Output Enable #":
REFNAME: "plld_oe":
When selected, disables DRAM clock output; when cleared, enables DRAM clock output.

refname: plld_oe

PARAM: "Enable Testing Signal Out":
REFNAME: "edout":
Enables testing signal out, in order to sample DMU
clock signal on the board through a dedicated pin.
The sampled signal is half of the output frequency.

refname: edout

PARAM: "Output Divider (OD)":
REFNAME: "plld_od":
Divider used for calculation of the DMU clock.

refname: plld_od

PARAM: "Divider Denominator (R)":
REFNAME: "plld_r":
Divider Denominator used for
calculation of the DMU clock.

refname: plld_r

PARAM: "Divider Numerator (F)":
REFNAME: "plld_f":
Divider Numerator used for
calculation of the DMU clock.

refname: plld_f

PARAM: "Bypass Input Divider (BPNR)":
REFNAME: "plld_bpnr":
When set, the intput divider is bypassed.

refname: plld_bpnr

PARAM: "Frequency Output":
REFNAME: "dram_frequency_2x_khz":
On board DIMMs frequency (KHz)

refname: dram_frequency_2x_khz

PARAM: "LDIV":
REFNAME: "pllr_ldiv":
Sets the ratio between the frequency
of the pins of an external Ref clock and the SERDES
deferential clock

refname: pllr_ldiv

PARAM: "Enable Testing Signal Out":
REFNAME: "erout":
Enables testing signal out, in order to sample PLL Ref
clock signal on the board through a dedicated pin.

refname: erout

PARAM: "Bypass":
REFNAME: "pllr_bp":
When set, PLL Reference clock is bypassed.
Used only in special debug modes.

refname: pllr_bp

PARAM: "PLL PCI Clock Enable Testing Signal Out":
REFNAME: "epout":
Enables testing signal out, in order to sample PLL PCI
clock signal on the board, through a dedicated pin.

refname: epout

PARAM: "PLL Stabilization Time":
REFNAME: "pll_st":
Specifies the time, in units of external clocks,
multiplied by 1024.
Required for stabilizing the internal PLLs.

refname: pll_st

PARAM: "Log DDR Max Size":
REFNAME: "log2_ddr_size":
Log 2 of DDR Maximum size.
DDR Maximum Size parameter enables the user to
limit the use of the attached memory (DRAM) to
less than actuall size.

refname: log2_ddr_size

PARAM: "ECC Mode":
REFNAME: "ecc_mode":

Determines type of attached DIMMs EEC mode

refname: ecc_mode

PARAM: "Auto Precharge Mode":
REFNAME: "auto_precharge_mode":

Determines Auto Precharge mode

refname: auto_precharge_mode

PARAM: "Cmd Gap Rate0":
REFNAME: "cmd_gap_rate0":
Minimum gap (in clocks) between execution of 2 requests (RD or WR) from the PCI port.
This value affects performance.

refname: cmd_gap_rate0

PARAM: "Cmd Gap Rate1":
REFNAME: "cmd_gap_rate1":
Minimum gap (in clocks) between execution of 2 requests (RD or WR) from the HCA port.
This value affects performance.

refname: cmd_gap_rate1

PARAM: "Hide DDR":
REFNAME: "hide_ddr_en":
Enables/disables the DDR BAR.

refname: hide_ddr_en

PARAM: "DDR Address Lsb":
REFNAME: "ddr_addr_lsb":
[31:0] bits address of ddr space given by user.

refname: ddr_addr_lsb

PARAM: "DDR Address Msb":
REFNAME: "ddr_addr_msb":
[63:32] bits address of ddr space given by user.

refname: ddr_addr_msb

PARAM: "Exit SR WAITING PERIOD[DCLK]":
REFNAME: "xsr_dclk_wait":
Numer of dram clocks InfiniHost waits before exiting
after Self-Refresh has been activated.

refname: xsr_dclk_wait

PARAM: "SPD Address":
REFNAME: "SPD0_addr":
First DIMM slot address on board.
Please specify the following values:
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.
NOT PRESSENT: 0x100 - DIMMs not present in any form.
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD0_addr

PARAM: "SPD Address":
REFNAME: "SPD1_addr":
Second Dimm slot address on board.
Please specify the following values:
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.
NOT PRESSENT: 0x100 - DIMMs not present in any form.
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD1_addr

PARAM: "SPD offset":
REFNAME: "SPD0_offset":
first Dimm slot offset on EEPROM (valid only if address is from EEPROM).

refname: SPD0_offset

PARAM: "SPD Offset":
REFNAME: "SPD1_offset":
Second Dimm slot address EEPROM (valid only if address is from EEPROM).

refname: SPD1_offset

PARAM: "SPD 16 bit addr ":
REFNAME: "SPD0_width":
First Dimm slot EEPROM address width (valid only if address is from EEPROM).

refname: SPD0_width

PARAM: "SPD 16 bit addr ":
REFNAME: "SPD1_width":

Second Dimm slot EEPROM address width (valid only if address is from EEPROM).

refname: SPD1_width

PARAM: "WriteOnly DIMM":
REFNAME: "dimm0_writeonly":

refname: dimm0_writeonly

PARAM: "WriteOnly DIMM":
REFNAME: "dimm1_writeonly":

refname: dimm1_writeonly

PARAM: "Supported Dimm Types":
REFNAME: "dimm0_types":

refname: dimm0_types

PARAM: "Supported Dimm Types":
REFNAME: "dimm1_types":

refname: dimm1_types

PARAM: "SPD Address":
REFNAME: "SPD2_addr":
Third Dimm slot address on board.
Please specify the following values:
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.
NOT PRESSENT: 0x100 - DIMMs not present in any form.
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD2_addr

PARAM: "SPD Address":
REFNAME: "SPD3_addr":
Fourth Dimm slot address on board.
Please specify the following values:
DIMM EEPROM : 0-0x96 - Valid address for reading via I2C from DIMMs EEPROM.
NOT PRESSENT: 0x100 - DIMMs not present in any form.
SPDLESS : 0x101 - Read DIMMs values from InfiniBurn pre-set values

refname: SPD3_addr

PARAM: "SPD offset":
REFNAME: "SPD2_offset":
first Dimm slot offset on EEPROM (valid only if address is from EEPROM).

refname: SPD2_offset

PARAM: "SPD Offset":
REFNAME: "SPD3_offset":
Second Dimm slot address EEPROM (valid only if address is from EEPROM).

refname: SPD3_offset

PARAM: "SPD 16 bit addr ":
REFNAME: "SPD2_width":
Third Dimm slot EEPROM address width (valid only if address is from EEPROM).

refname: SPD2_width

PARAM: "SPD 16 bit addr ":
REFNAME: "SPD3_width":
Forth Dimm slot EEPROM address width (valid only if address is from EEPROM).

refname: SPD3_width

PARAM: "WriteOnly DIMM":
REFNAME: "dimm2_writeonly":

refname: dimm2_writeonly

PARAM: "WriteOnly DIMM":
REFNAME: "dimm3_writeonly":

refname: dimm3_writeonly

PARAM: "Supported Dimm Types":
REFNAME: "dimm2_types":

refname: dimm2_types

PARAM: "Supported Dimm Types":
REFNAME: "dimm3_types":

refname: dimm3_types

PARAM: "dimm0_byte0":
REFNAME: "dimm0_byte0":

refname: dimm0_byte0

PARAM: "dimm0_byte1":
REFNAME: "dimm0_byte1":

refname: dimm0_byte1

PARAM: "dimm0_byte2":
REFNAME: "dimm0_byte2":

refname: dimm0_byte2

PARAM: "dimm0_byte3":
REFNAME: "dimm0_byte3":

refname: dimm0_byte3

PARAM: "dimm0_byte4":
REFNAME: "dimm0_byte4":

refname: dimm0_byte4

PARAM: "dimm0_byte5":
REFNAME: "dimm0_byte5":

refname: dimm0_byte5

PARAM: "dimm0_byte6":
REFNAME: "dimm0_byte6":

refname: dimm0_byte6

PARAM: "dimm0_byte7":
REFNAME: "dimm0_byte7":

refname: dimm0_byte7

PARAM: "dimm0_byte8":
REFNAME: "dimm0_byte8":

refname: dimm0_byte8

PARAM: "dimm0_byte9":
REFNAME: "dimm0_byte9":

refname: dimm0_byte9

PARAM: "dimm0_byte10":
REFNAME: "dimm0_byte10":

refname: dimm0_byte10

PARAM: "dimm0_byte11":
REFNAME: "dimm0_byte11":

refname: dimm0_byte11

PARAM: "dimm0_byte12":
REFNAME: "dimm0_byte12":

refname: dimm0_byte12

PARAM: "dimm0_byte13":
REFNAME: "dimm0_byte13":

refname: dimm0_byte13

PARAM: "dimm0_byte14":
REFNAME: "dimm0_byte14":

refname: dimm0_byte14

PARAM: "dimm0_byte15":
REFNAME: "dimm0_byte15":

refname: dimm0_byte15

PARAM: "dimm0_byte16":
REFNAME: "dimm0_byte16":

refname: dimm0_byte16

PARAM: "dimm0_byte17":
REFNAME: "dimm0_byte17":

refname: dimm0_byte17

PARAM: "dimm0_byte18":
REFNAME: "dimm0_byte18":

refname: dimm0_byte18

PARAM: "dimm0_byte19":
REFNAME: "dimm0_byte19":

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PARAM: "dimm0_byte20":
REFNAME: "dimm0_byte20":

refname: dimm0_byte20

PARAM: "dimm0_byte21":
REFNAME: "dimm0_byte21":

refname: dimm0_byte21

PARAM: "dimm0_byte22":
REFNAME: "dimm0_byte22":

refname: dimm0_byte22

PARAM: "dimm0_byte23":
REFNAME: "dimm0_byte23":

refname: dimm0_byte23

PARAM: "dimm0_byte24":
REFNAME: "dimm0_byte24":

refname: dimm0_byte24

PARAM: "dimm0_byte25":
REFNAME: "dimm0_byte25":

refname: dimm0_byte25

PARAM: "dimm0_byte26":
REFNAME: "dimm0_byte26":

refname: dimm0_byte26

PARAM: "dimm0_byte27":
REFNAME: "dimm0_byte27":

refname: dimm0_byte27

PARAM: "dimm0_byte28":
REFNAME: "dimm0_byte28":

refname: dimm0_byte28

PARAM: "dimm0_byte29":
REFNAME: "dimm0_byte29":

refname: dimm0_byte29

PARAM: "dimm0_byte30":
REFNAME: "dimm0_byte30":

refname: dimm0_byte30

PARAM: "dimm0_byte31":
REFNAME: "dimm0_byte31":

refname: dimm0_byte31

PARAM: "dimm0_byte32":
REFNAME: "dimm0_byte32":

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PARAM: "dimm0_byte33":
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PARAM: "dimm0_byte34":
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PARAM: "dimm0_byte35":
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PARAM: "dimm0_byte36":
REFNAME: "dimm0_byte36":

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PARAM: "dimm0_byte37":
REFNAME: "dimm0_byte37":

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PARAM: "dimm0_byte38":

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PARAM: "dimm0_byte39":
REFNAME: "dimm0_byte39":

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PARAM: "dimm0_byte40":
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PARAM: "dimm0_byte41":
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PARAM: "dimm0_byte42":
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PARAM: "dimm0_byte43":
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PARAM: "dimm0_byte45":
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PARAM: "dimm0_byte46":
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PARAM: "dimm0_byte47":
REFNAME: "dimm0_byte47":

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PARAM: "dimm0_byte48":
REFNAME: "dimm0_byte48":

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PARAM: "dimm0_byte49":
REFNAME: "dimm0_byte49":

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PARAM: "dimm0_byte50":
REFNAME: "dimm0_byte50":

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PARAM: "dimm0_byte51":
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PARAM: "dimm1_byte0":
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PARAM: "dimm1_byte1":
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PARAM: "dimm1_byte46":
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PARAM: "dimm1_byte47":
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PARAM: "dimm1_byte48":
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PARAM: "dimm1_byte49":
REFNAME: "dimm1_byte49":

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PARAM: "dimm1_byte50":
REFNAME: "dimm1_byte50":

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PARAM: "dimm1_byte51":
REFNAME: "dimm1_byte51":

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PARAM: "dimm1_byte52":
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PARAM: "dimm1_byte58":
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PARAM: "dimm1_byte59":
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PARAM: "dimm1_byte60":
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PARAM: "dimm1_byte61":
REFNAME: "dimm1_byte61":

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PARAM: "dimm1_byte62":
REFNAME: "dimm1_byte62":

refname: dimm1_byte62

PARAM: "dimm1_byte63":
REFNAME: "dimm1_byte63":

refname: dimm1_byte63

PARAM: "dimm2_byte0":
REFNAME: "dimm2_byte0":

refname: dimm2_byte0

PARAM: "dimm2_byte1":
REFNAME: "dimm2_byte1":

refname: dimm2_byte1

PARAM: "dimm2_byte2":
REFNAME: "dimm2_byte2":

refname: dimm2_byte2

PARAM: "dimm2_byte3":
REFNAME: "dimm2_byte3":

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PARAM: "dimm2_byte4":
REFNAME: "dimm2_byte4":

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PARAM: "dimm2_byte5":
REFNAME: "dimm2_byte5":

refname: dimm2_byte5

PARAM: "dimm2_byte6":
REFNAME: "dimm2_byte6":

refname: dimm2_byte6

PARAM: "dimm2_byte7":
REFNAME: "dimm2_byte7":

refname: dimm2_byte7

PARAM: "dimm2_byte8":
REFNAME: "dimm2_byte8":

refname: dimm2_byte8

PARAM: "dimm2_byte9":
REFNAME: "dimm2_byte9":

refname: dimm2_byte9

PARAM: "dimm2_byte10":
REFNAME: "dimm2_byte10":

refname: dimm2_byte10

PARAM: "dimm2_byte11":
REFNAME: "dimm2_byte11":

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PARAM: "dimm2_byte12":
REFNAME: "dimm2_byte12":

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PARAM: "dimm2_byte13":
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PARAM: "dimm2_byte14":
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REFNAME: "dimm2_byte15":

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PARAM: "dimm2_byte16":
REFNAME: "dimm2_byte16":

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PARAM: "dimm2_byte17":
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PARAM: "dimm2_byte19":
REFNAME: "dimm2_byte19":

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PARAM: "dimm2_byte20":
REFNAME: "dimm2_byte20":

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PARAM: "dimm2_byte21":
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REFNAME: "dimm2_byte22":

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PARAM: "dimm2_byte23":
REFNAME: "dimm2_byte23":

refname: dimm2_byte23

PARAM: "dimm2_byte24":
REFNAME: "dimm2_byte24":

refname: dimm2_byte24

PARAM: "dimm2_byte25":
REFNAME: "dimm2_byte25":

refname: dimm2_byte25

PARAM: "dimm2_byte26":
REFNAME: "dimm2_byte26":

refname: dimm2_byte26

PARAM: "dimm2_byte27":
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PARAM: "dimm2_byte28":
REFNAME: "dimm2_byte28":

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PARAM: "dimm2_byte29":
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PARAM: "dimm2_byte30":
REFNAME: "dimm2_byte30":

refname: dimm2_byte30

PARAM: "dimm2_byte31":
REFNAME: "dimm2_byte31":

refname: dimm2_byte31

PARAM: "dimm2_byte32":
REFNAME: "dimm2_byte32":

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PARAM: "dimm2_byte34":
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refname: dimm2_byte34

PARAM: "dimm2_byte35":
REFNAME: "dimm2_byte35":

refname: dimm2_byte35

PARAM: "dimm2_byte36":
REFNAME: "dimm2_byte36":

refname: dimm2_byte36

PARAM: "dimm2_byte37":
REFNAME: "dimm2_byte37":

refname: dimm2_byte37

PARAM: "dimm2_byte38":
REFNAME: "dimm2_byte38":

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PARAM: "dimm2_byte39":
REFNAME: "dimm2_byte39":

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PARAM: "dimm2_byte40":
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PARAM: "dimm2_byte41":
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refname: dimm2_byte41

PARAM: "dimm2_byte42":
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PARAM: "dimm2_byte43":
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PARAM: "dimm2_byte45":
REFNAME: "dimm2_byte45":

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PARAM: "dimm2_byte46":
REFNAME: "dimm2_byte46":

refname: dimm2_byte46

PARAM: "dimm2_byte47":
REFNAME: "dimm2_byte47":

refname: dimm2_byte47

PARAM: "dimm2_byte48":
REFNAME: "dimm2_byte48":

refname: dimm2_byte48

PARAM: "dimm2_byte49":
REFNAME: "dimm2_byte49":

refname: dimm2_byte49

PARAM: "dimm2_byte50":
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refname: dimm2_byte50

PARAM: "dimm2_byte51":
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PARAM: "dimm2_byte52":
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PARAM: "dimm2_byte61":
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PARAM: "dimm2_byte62":
REFNAME: "dimm2_byte62":

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PARAM: "dimm2_byte63":
REFNAME: "dimm2_byte63":

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PARAM: "dimm3_byte0":
REFNAME: "dimm3_byte0":

refname: dimm3_byte0

PARAM: "dimm3_byte1":
REFNAME: "dimm3_byte1":

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PARAM: "dimm3_byte2":
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PARAM: "dimm3_byte3":
REFNAME: "dimm3_byte3":

refname: dimm3_byte3

PARAM: "dimm3_byte4":
REFNAME: "dimm3_byte4":

refname: dimm3_byte4

PARAM: "dimm3_byte5":
REFNAME: "dimm3_byte5":

refname: dimm3_byte5

PARAM: "dimm3_byte6":
REFNAME: "dimm3_byte6":

refname: dimm3_byte6

PARAM: "dimm3_byte7":
REFNAME: "dimm3_byte7":

refname: dimm3_byte7

PARAM: "dimm3_byte8":

REFNAME: "dimm3_byte8":

refname: dimm3_byte8

PARAM: "dimm3_byte9":
REFNAME: "dimm3_byte9":

refname: dimm3_byte9

PARAM: "dimm3_byte10":
REFNAME: "dimm3_byte10":

refname: dimm3_byte10

PARAM: "dimm3_byte11":
REFNAME: "dimm3_byte11":

refname: dimm3_byte11

PARAM: "dimm3_byte12":
REFNAME: "dimm3_byte12":

refname: dimm3_byte12

PARAM: "dimm3_byte13":
REFNAME: "dimm3_byte13":

refname: dimm3_byte13

PARAM: "dimm3_byte14":
REFNAME: "dimm3_byte14":

refname: dimm3_byte14

PARAM: "dimm3_byte15":
REFNAME: "dimm3_byte15":

refname: dimm3_byte15

PARAM: "dimm3_byte16":
REFNAME: "dimm3_byte16":

refname: dimm3_byte16

PARAM: "dimm3_byte17":
REFNAME: "dimm3_byte17":

refname: dimm3_byte17

PARAM: "dimm3_byte18":
REFNAME: "dimm3_byte18":

refname: dimm3_byte18

PARAM: "dimm3_byte19":
REFNAME: "dimm3_byte19":

refname: dimm3_byte19

PARAM: "dimm3_byte20":
REFNAME: "dimm3_byte20":

refname: dimm3_byte20

PARAM: "dimm3_byte21":
REFNAME: "dimm3_byte21":

refname: dimm3_byte21

PARAM: "dimm3_byte22":
REFNAME: "dimm3_byte22":

refname: dimm3_byte22

PARAM: "dimm3_byte23":
REFNAME: "dimm3_byte23":

refname: dimm3_byte23

PARAM: "dimm3_byte24":
REFNAME: "dimm3_byte24":

refname: dimm3_byte24

PARAM: "dimm3_byte25":
REFNAME: "dimm3_byte25":

refname: dimm3_byte25

PARAM: "dimm3_byte26":
REFNAME: "dimm3_byte26":

refname: dimm3_byte26

PARAM: "dimm3_byte27":
REFNAME: "dimm3_byte27":

refname: dimm3_byte27

PARAM: "dimm3_byte28":
REFNAME: "dimm3_byte28":

refname: dimm3_byte28

PARAM: "dimm3_byte29":
REFNAME: "dimm3_byte29":

refname: dimm3_byte29

PARAM: "dimm3_byte30":
REFNAME: "dimm3_byte30":

refname: dimm3_byte30

PARAM: "dimm3_byte31":
REFNAME: "dimm3_byte31":

refname: dimm3_byte31

PARAM: "dimm3_byte32":
REFNAME: "dimm3_byte32":

refname: dimm3_byte32

PARAM: "dimm3_byte33":
REFNAME: "dimm3_byte33":

refname: dimm3_byte33

PARAM: "dimm3_byte34":
REFNAME: "dimm3_byte34":

refname: dimm3_byte34

PARAM: "dimm3_byte35":
REFNAME: "dimm3_byte35":

refname: dimm3_byte35

PARAM: "dimm3_byte36":
REFNAME: "dimm3_byte36":

refname: dimm3_byte36

PARAM: "dimm3_byte37":
REFNAME: "dimm3_byte37":

refname: dimm3_byte37

PARAM: "dimm3_byte38":
REFNAME: "dimm3_byte38":

refname: dimm3_byte38

PARAM: "dimm3_byte39":
REFNAME: "dimm3_byte39":

refname: dimm3_byte39

PARAM: "dimm3_byte40":
REFNAME: "dimm3_byte40":

refname: dimm3_byte40

PARAM: "dimm3_byte41":
REFNAME: "dimm3_byte41":

refname: dimm3_byte41

PARAM: "dimm3_byte42":
REFNAME: "dimm3_byte42":

refname: dimm3_byte42

PARAM: "dimm3_byte43":
REFNAME: "dimm3_byte43":

refname: dimm3_byte43

PARAM: "dimm3_byte44":
REFNAME: "dimm3_byte44":

refname: dimm3_byte44

PARAM: "dimm3_byte45":
REFNAME: "dimm3_byte45":

refname: dimm3_byte45

PARAM: "dimm3_byte46":
REFNAME: "dimm3_byte46":

refname: dimm3_byte46

PARAM: "dimm3_byte47":
REFNAME: "dimm3_byte47":

refname: dimm3_byte47

PARAM: "dimm3_byte48":
REFNAME: "dimm3_byte48":

refname: dimm3_byte48

PARAM: "dimm3_byte49":
REFNAME: "dimm3_byte49":

refname: dimm3_byte49

PARAM: "dimm3_byte50":
REFNAME: "dimm3_byte50":

refname: dimm3_byte50

PARAM: "dimm3_byte51":
REFNAME: "dimm3_byte51":

refname: dimm3_byte51

PARAM: "dimm3_byte52":
REFNAME: "dimm3_byte52":

refname: dimm3_byte52

PARAM: "dimm3_byte53":
REFNAME: "dimm3_byte53":

refname: dimm3_byte53

PARAM: "dimm3_byte54":
REFNAME: "dimm3_byte54":

refname: dimm3_byte54

PARAM: "dimm3_byte55":
REFNAME: "dimm3_byte55":

refname: dimm3_byte55

PARAM: "dimm3_byte56":
REFNAME: "dimm3_byte56":

refname: dimm3_byte56

PARAM: "dimm3_byte57":
REFNAME: "dimm3_byte57":

refname: dimm3_byte57

PARAM: "dimm3_byte58":
REFNAME: "dimm3_byte58":

refname: dimm3_byte58

PARAM: "dimm3_byte59":
REFNAME: "dimm3_byte59":

refname: dimm3_byte59

PARAM: "dimm3_byte60":
REFNAME: "dimm3_byte60":

refname: dimm3_byte60

PARAM: "dimm3_byte61":
REFNAME: "dimm3_byte61":

refname: dimm3_byte61

PARAM: "dimm3_byte62":

REFNAME: "dimm3_byte62":

refname: dimm3_byte62

PARAM: "dimm3_byte63":
REFNAME: "dimm3_byte63":

refname: dimm3_byte63

PARAM: "NTU 66 MHZ Capable":
REFNAME: "ntu_66mhz_capable":
Mellanox NTU support of 66 MHZ reported to system sweep process.

refname: ntu_66mhz_capable

PARAM: "FW Size in DDR":
REFNAME: "fw_length":
Log2 of DDR memory allocated for InifniHost FW (Bytes).
This memory area should not be accessed by any
external device (see PRM restrictions).

refname: fw_length

PARAM: "FW Trace Buffer Size (MB)":
REFNAME: "total_trace_buf_sz_mb":
Trace Buffer size for all iRISCs. The Trace buffer
is divided to six parts - one for each iRISC.
The trace buffer resides in DDR memory. Its allocation is
in addition to FW required length.

refname: total_trace_buf_sz_mb

PARAM: "Disable Vendor Specific MADs":
REFNAME: "vendor_specific_sup":
Enables/disable Vendor specific MAD support

refname: vendor_specific_sup