INTERFACING THE RC30XX FAMILY WITH GT32011

Technical Note TN-44

Introduction

IDT's RC30XX RISController™ family of microprocessors—comprised of the RC3041, RC3051, RC3052 and RC3081—are 32-bit microprocessors that implement the MIPS Instruction Set Architecture. The family offers a wide variety of processors with a broad set of features enabling cost and performance optimization of embedded systems.

Galileo Technology's GT32011 is a low-cost system controller designed for use with the RC30XX family of processors. The GT32011 offers memory control, DMA interfaces, timers and system control logic to complement IDT's RC30XX family.

This application note focuses on interfacing IDT's RC30XX family of microprocessors with the Galileo Technology's GT32011. In particular, this application note will focus on system design considerations, including cautions and recommendations, to avoid or alleviate bus interface errors when transmitting address information from an RC30XX to a GT32011.

RC30XX Family Timing Overview

There are two timing parameters that will be discussed. In the IDT data sheets, for the RC30XX family, the parameters are referred to as t8 and t10, which are illustrated in Figure 1.

t8: The timing parameter t8 is the measurement of time between the rising edge of SYSCLK and the assertion of ALE.

t10: The timing parameter t10 is the measurement of hold time of the address on the SYSAD bus following ALE negation.

IDT specifies a maximum value for t8 which varies with processor and frequency. No minimum value is specified. Both SYSCLK and ALE are independently generated by an internal clocking mechanism. ALE is not produced or driven by SYSCLK. Therefore, a minimum value for t8 cannot be guaranteed as this value can be affected by system design. Most notably, unequal capacitive loading on SYSCLK and ALE can force reductions in t8 and in some systems can cause the value to appear negative. IDT specifies a minimum value for t10.

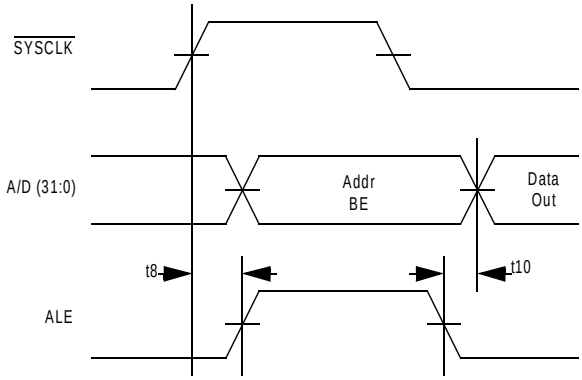

Figure 1 t8 and t10 parameters for RC30XX

GT32011 Timing Overview

Galileo Technology's data sheet for the GT32011 specifies t15 as the minimum time between the rising edge of SYSCLK and ALE assertion (this is the same as the IDT parameter labeled t8). This value is required to be no less than 0ns; therefore, the rising edge of SYSCLK must lead or coincide with the rising edge of ALE. If this relationship is not maintained, logic in the GT32011 will detect ALE and latch processor state one positive edge of SYSCLK prematurely, causing a system failure.

RC30XX and GT32011 Interface

Given that IDT does not specify a minimum value for t8 on the RC30XX family of processors, and that the GT32011 requires this value be no less than 0ns, an RC30XX processor operating within specification can violate the timing requirements of the GT32011 in certain applications.

ALE can lead SYSCLK in systems that place a heavier capacitive load on SYSCLK than ALE. This inhibits the GT32011 from properly triggering on ALE with respect to SYSCLK. Additionally, temperature increases in a system may exacerbate any improper loading. As temperature rises in the RC30XX, both SYSCLK and ALE will become slower. If SYSCLK is more heavily loaded than ALE, SYSCLK will slow even further with respect to ALE. Systems operating without error at nominal system temperatures may exhibit timing violations as system temperature increases.

IDT does not recommend that ALE be used to enable any logic to latch any processor state. ALE should only be use to latch the address from the processor. IDT recommends that designs using an RC30XX use control signals to inform the system control state machine that a bus transaction has begun. The state machine should be programmed to generate a cycle end signal at the end of a bus transaction. This signal can be derived by programming the system control state machine to count the number of cycles in a given transaction. This removes the burden from the system control logic to sample RC30XX control signals at the end of a bus transaction. The Galileo GT32011 uses ALE to latch RC30XX control signals, and when ALE leads SYSCLK, control signals can be sampled one rising edge of SYSCLK prematurely, causing the GT32011 to mal-function.

Design Considerations and Impacts

New Designs

Loading of the SYSCLK and ALE outputs is the key factor in decreasing the chance of the timing violation between ALE and SYSCLK on the GT32011. In a typical system, SYSCLK from the RC30XX will be loaded by the GT32011 as well as other system components. ALE however, is typically loaded only by the GT32011. Matching the loading on SYSCLK and ALE will help to ensure similar delays of the rising edges due to loading. For more margin, ALE should be loaded by a total equivalent capacitance which exceeds the loading on SYSCLK by 25pF.

Upgrading Existing Designs

An existing system implementing an RC30XX and GT32011 can be retrofitted to ensure that this problem does not appear in the future and can correct the issue in systems exhibiting timing violations. By adding the capacitive load to ALE as described above (25pF greater than the total load on SYSCLK), ALE should be delayed sufficient to ensure timing which meets the requirements of the GT32011.

Impacts to the RC30XX

Adding what essentially amounts as a delay of ALE with respect to SYSCLK into a design has no deleterious impact on other RC30XX timing parameters. Of most concern would be t10, the hold time of the address on the SYSAD bus after negation of ALE. In the timing diagram, it appears that if the ALE pulse is moved to the right with respect to the edge of SYSCLK, t10 will be shortened by the amount ALE was delayed.

However, the timing generation unit of the RC30XX family was designed to ensure proper relationship and hold times after ALE negation. This is guaranteed in two ways. First, the phase lock loop (PLL) that is used to generate SYSCLK does not sample the output therefore, the PLL and SYSCLK are decoupled. Second, ALE is fed back into the SYSAD circuitry and sampled to trigger the transition on the SYSAD bus. Address hold time is preserved and remains constant regardless of system configuration.