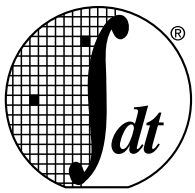

Integrated Device Technology, Inc.

Integrated Device Technology RISController and CPU Performance Report September 1997

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Integrated Device Technology, Inc.

IDT Performance Report
September 1997

Introduction

Integrated Device Technology, Inc. is dedicated to providing complete RISC design solutions by combining expertise in silicon process with leadership products in development systems and software. The 32-bit R30xx RISController family consists of R3041, R3051, R3052 and the R3081. The 64-bit Orion CPU family includes the R4640, R4650, R4700 and the R5000.

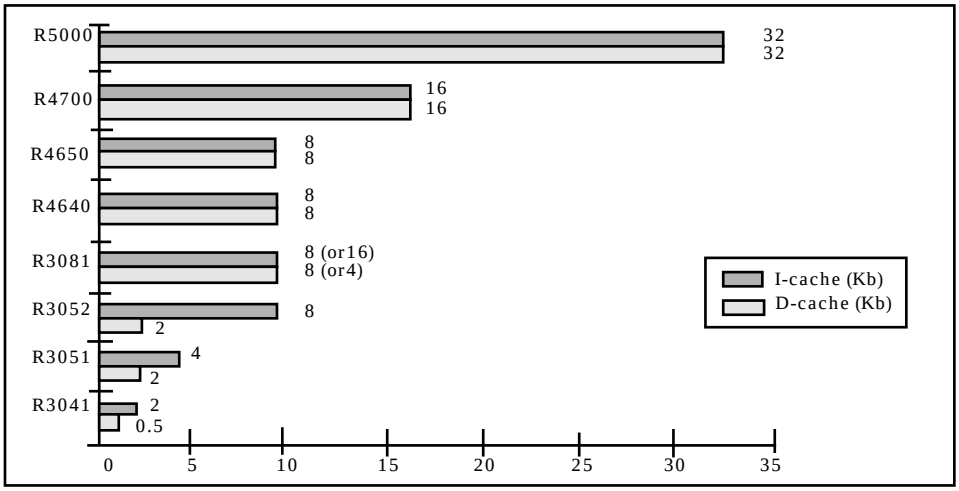
This report presents the results of performance benchmarks executed on a variety of IDT RISControllers and CPUs residing in a variety of IDT RISC evaluation boards.

While it is highly recommended that system and software designers run their own specific benchmarks—which simulate their own specific needs—prior to reaching a decision regarding choice of processor, it is recognized that such an exercise is not always feasible. Under these circumstances, a set of benchmark data—for well known benchmarks—can prove to be invaluable while attempting to scope the strengths and/or weaknesses of processors under consideration.

The majority of standard embedded benchmarks is small enough that their entire code and data fit in the caches of processors from IDT as well as its competitors. One of the strengths of IDT's processors, their large cache sizes, is consequently under-represented by the benchmarks. It is important that potential systems and software designers give due consideration to this limitation of standard benchmarks. A large benchmark such as "LINPACK" may offer a better view of cache size effects, even if it does not simulate a designer's intended application.

Processors and RISControllers

PART	D-cache (Kb)	I-cache (Kb)	Max F (MHz)	Comments
R3041	0.5	2	33	No FPA, 8/16/32 bit bus interface
R3051	2	4	40	No FPA
R3052	2	8	40	No FPA
R3081	8 (or 4)	8 (or 16)	50	D/I cache configurable, _ freq. bus support
R4640	8	8	133	DSP, 32-bit external bus, Single Precision FPA
R4650	8	8	133	DSP, 32 or 64-bit external bus, Single Precision FPA
R4700	16	16	175	Divide by 2..8 bus, true 64-bit everything, faster FPA
R5000	32	32	200	DSP, MIPS-4, super scalar, secondary cache controller



Target Evaluation Boards

A total of five evaluation boards were used as targets for the benchmark exercise. The 79S381 board works with any member of the R30xx RISController family. The 79S465 serves as the mother board for a number of daughter cards which host the R4xxx and R5000 CPUs. The 79S466 daughter card hosts the R4700 CPU. The 79S440 daughter card hosts both the R4640 and R4650 CPUs on a single card and allows the user to select a few hardware jumper connector options.

Memory System Characteristics Of IDT's Evaluation Boards

Board	Block-read	Single-read	Block-write	Single-write	Frequency MHz (CPU/SYS)	Comments
79S381	5(9)-1-2-1- 2-1-1-1	5(9) 2		6(9) 2	33/33	DRAM 0 wait-state SRAM
79S465	7-1-1-1+1* 3-1-1-1+1*	6+1* 3+1*	2-1-3-1+2** 2-1-1-1	6 4	See daughter boards below	DRAM SRAM
79S466	See Comments	See Comments	See Comments	See Comments	175/44.33	daughter boards for 79S465 memory latencies same as those for the motherboard
79S440	See Comments	See Comments	See Comments	See Comments	133/44/33	
79S500	See Comments	See Comments	See Comments	See Comments	200/50	

Notes: *extra turnaround cycle at end of read access
**2 extra clock cycles at end of block write for DRAM

IDT79S381

The IDT79S381 is a high performance stand-alone RISC evaluation board, designed primarily for executing benchmarks and for RISController architecture evaluation. Its 33 MHz zero wait-state memory permits true evaluation of the processing units. Parts such as the R3081(E) can be run at up to 50 MHz using their half-speed-bus modes. The board design is an example of using an integrated DRAM controller.

Major features of the 79S381 are: 33 MHz system operation, 2/4/6/16 MB interleaved DRAM, 256K zero wait-state SRAM, 512 KB to 2 MB EPROM, 2 serial ports, IEEE 802.3 ethernet subsystem with 8 KB dual port memory, 1024 bit serial EPROM, 3 external user timers on DUART, ethernet, and DRAM controller, IDT/sim monitor and debug software in EPROMs.

High speed SRAM, ethernet controller and associated circuitry make this board high-cost but the goal of creating a benchmark and software development/evaluation platform precluded cost considerations. Also, note that the DRAM controller used was actually intended for a different CPU; an ASIC or FPGA could easily offer higher DRAM performance.

IDT79S465

The IDT79S465 is a stand-alone evaluation vehicle for the R4xx0 CPUs. Major features of the S465 board are: 50 MHz system interface design allowing 200 MHz CPU testing, 4 to 64 MB of interleaved DRAM, 4 MB of zero wait-state interleaved SRAM, 2 MB of non-interleaved, cacheable Flash memory, ethernet interface, a SCSI-II port, 2 serial ports, a Centronics parallel port, system monitor with low level debugging support Flash. The 79S465 board has a variety of daughter card attachments including the 79S466 for the R4650 or the R4700; the 79S440 for the R4640 and the R4650 on the same card; and the 79S500 for the R5000.

IDT79S466

The IDT79S466 is a daughter card attachment to the IDT79S465 evaluation board. This small module supports the R4700 PGA and PQFP foot prints and the R4650 PQFP foot prints. Both 32-bit and 64-bit interfaces are supported. Both 3.3V and 5V operations are supported. Selecting between the R4700 and the R4650 is accomplished through hardware jumpers, and only one CPU can be plugged into the board at a time.

IDT79S440

The IDT79S440 is a daughter card attachment to the IDT79S465 evaluation board. This small module supports the R4650 PQFP foot prints and the R4640 PQFP foot prints. Both 32-bit and 64-bit interfaces are supported. Both 3.3V and 5V operations are supported. Selecting between the R4650 and the R4640 is accomplished through hardware jumpers and both CPUs can be plugged into the board at the same time. The IDT79S440 plugs directly into the PGA socket of the R4700 in the IDT79S465 board.

IDT79S500

The IDT79S500 is a daughter card attachment to the IDT79S465 evaluation board. This small module supports the R5000 PGA foot prints. 64-bit interface is supported. Both 3.3V operation is supported. The IDT79S500 plugs directly into the PGA socket of the R4700 in the IDT79S465 board. 2MB level 2 (L2) cache support is provided. Unlike some of the other daughter cards, the IDT79S500 needs to be connected to the power supply itself. A different “Reset Controller” EPLD needs to replace the standard EPLD provided with the IDT79S465 board. Versions of IDT/sim older than 7.0 do not recognize the IDT79S500.

Benchmark Programs

This section describes each of the benchmarks executed in some detail. Some of the information has been obtained from the comments in the benchmarks' source code. The remaining information has been obtained from published material or from internet resources. Source code for the benchmarks may be obtained from a variety of sources on the internet or directly from IDT.

Whetstone

Unit of measure: Millions of Whetstones / Second. (larger is better)

The Whetstone benchmark is used to test floating point performance of the target. It is a synthetic mix of floating point and integer arithmetic, function calls, array indexing, conditional jumps, and transcendental functions. The benchmark comprises of 10 modules which when put together amount to 1 million Whetstone instructions. The benchmark exercises a number of compiler features including local common sub-expression elimination, conditional jump optimization, array elements arithmetic, passing array as a parameter, integer arithmetic, trigonometric functions, array references, etc.

This benchmark has been carefully arranged to defeat vectorizing and a number of compiler optimizations. The code and data sizes are moderate and can help in differentiating processors with different cache sizes. With the newer and faster processors of today, the low resolution of the timers tend to have adverse effect on the measured times. It is, therefore, common to increase the loop counts in the code to increase the running time of the benchmark and then to scale the results appropriately.

Stanford

Unit of Measure: Stanford integer composite and Stanford floating point composite. (smaller is better)

Stanford measures both integer and floating point performance of the target. A weighted measure of integer and floating point components of a number of different independent programs is accumulated and presented as the final result. A total of 10 problems are solved with primary emphasis on heavily recursive code and integer as well as floating point math on elements of large arrays. Some of these problems are Towers of Hanoi, matrix multiplication, permutation, eight queens, quick sort, tree sort, bubble sort, fast Fourier transform.

Stanford benchmarks are popular because they are small enough to simulate, and are responsive to compiler optimizations. The floating point components are relevant to those that use tight loops and a high proportion of actual floating point code. This is different from Linpack which also tends to depend on memory system performance as seen in the section.

Linpack

Unit of measure: KiloFlops (larger is better)

The LINPACK benchmark is one of the most widely used benchmarks to predict relative performance in scientific and engineering environments. LINPACK is a linear equations package that particularly emphasizes floating point addition and multiplication. It does Single and Double precision matrix and vector multiplication. It factors a matrix by Gaussian Elimination with partial pivoting.

The data size of this benchmark is very large and unless it fits entirely in the data cache, this benchmark can also be a test of the memory system design. Experimenting with the array sizes in the code can reveal the effects of memory system dependency. The data section of the unmodified Linpack benchmark does not fit in data caches of any of IDT's parts. However, the powerful floating point units in IDT's parts (those that have it) reduce the impact of memory system dependency on the results.

Dhrystone (versions 1.1 and 2.1)

Unit of measure: Dhrystones / Second (larger is better)

The Dhrystone benchmark tests the compiler using a balanced set of C statements. The following 3 aspects are balanced: statement type, operand type, operand locality (global, local, parameter or constant). The code does not do anything useful but the statements are generally broken down as approximately 53% of assignment statements, 33% of control statements, and 14% of procedure or function calls; the code is syntactically and semantically correct.

Version 1.1 is considered to be obsolete and is covered only for the sake of completeness and fairness towards older processors from other manufacturers who can only provide data for older versions of the benchmark. Most of the newer optimizing compilers simply throw away "do-nothing" type of "dead code" during compiling. Dhrystone version 1.1 had some "dead code" in it, and version 2.1 tried to fix this problem.

A variety of performance indicators generically called Mips-ratings have been around for a number of years. One of the more popular Mips-rating is VAX-Dhrystone-mips, a number obtained by dividing your dhrystone/second number by 1757, the number attributed to a VAX-11/780 with some version of the VAX/VMS compiler. VAX-Dhrystone-mips number is also commonly (and somewhat inaccurately) referred to as VAX-mips or VMIPS.

While it is true that Dhrystone is one of the more well-known integer benchmarks, the results should be treated with care, especially if this is the only benchmark that is likely to lead to a decision regarding processor selection. This benchmark has an unusually low number of instructions per function call, or in other words, it does more function calls than usual. The dynamic nesting depth of function calls inside the timed part of Dhrystone is low, thus under-utilizing the large number of registers which some of the RISC processors offer.

Dhrystone spends 30 to 40 percent of its time in the strcpy() function, copying atypically long strings of 30 characters or so, which also happen to be align-able on word boundaries. Most realistic applications deal with smaller strings and those which are not necessarily word aligned. Lastly, Dhrystone is a fairly small benchmark and will fit into almost any instruction cache. This is unfair to processors with large caches, one of the most important features of most of IDT's RISControllers and CPUs.

Benchmark Development Platforms

This section briefly describes the hardware and software that are used to perform the benchmarks.

Machine

All benchmarks were compiled on a Pentium-based IBM-PC compatible machine running Microsoft Windows-95 operating system in a DOS window. The target boards were connected to the PC using a serial cable. Microsoft Windows-95 “HyperTerminal” program was use to send text files (the S-record files which are ascii text) from the PC to the evaluation target boards. A PC standard switching power supply was required for the evaluation boards. A variety of clock crystals were required to perform the benchmarks at number of different frequencies.

Compiler

All benchmarks were compiled with IDT/C 7.0.IDT/C 7.0 generates MIPS-I, II, III, IV ISA code in ELF file format. Different MIPS levels are indicated to the compiler by the command line switches -mips1, -mips2, -mips3, -mips4. For processors without floating point units, to run floating point code, the GOFAST (register interface) floating point math emulation library from U. S. Software Corporation was used. The library is available as a part of IDT/C 7.0.

Two runs were performed for each set-up of each benchmark - one with default optimization (-O compile time switch) and another with high optimization (-O2 compile time switch). Both sets of results are presented in this document.

Without `-O', the compiler's goal is to reduce the cost of compilation and to make debugging produce the expected results. Statements are independent: if you stop the program with a breakpoint between statements, you can then assign a new value to any variable or change the program counter to any other statement in the function and get exactly the results you would expect from the source code.

Without `-O', the compiler only allocates variables declared `register' in registers. The resulting compiled code is a little worse than produced by PCC without `-O'.

With `-O', the compiler tries to reduce code size and execution time.

When you specify `-O', the compiler turns on `-fthread-jumps', `-fdefer-pop', `-fdelayed-branch', and `-fomit-frame-pointer'. Some other less important flags are also turned on.

The `-O2’ switch optimizes even more. The compiler performs nearly all supported optimizations that do not involve a space-speed tradeoff. The compiler does not perform loop unrolling or function in-lining with `-O2'. As compared to `-O', this option increases both compilation time and the performance of the generated code.

Benchmark Result Tables

Two sets of tables are provided. The first set is made up of a single table (broken into two parts to fit the page) which presents the best performance numbers for all benchmarks on all processors.

The second set is made up of 10 tables, one table per benchmark, with more detailed information for each run of the benchmark.

Best Results - All processors, All benchmarks

CPU/Bus Frequencies		**Dhry-1**	**Dhry-2**	**Whet-S**	**Whet-D**
Units =>	MHz	Dhrystones/S	Dhrystones/S	Mwhets/S	Mwhets/S
R5000-L2	180/45/45	367,341	399,103	79.18	77.45
R5000	180/45	367,341	399,102	79.19	77.45
R4700	175/44	365,849	393,007	61.64	58.57
R4650	133/44	279,385	301,558	20.64	12.56
R4640	150/50	279,401	301,575	20.32	12.56
R3081	50/25	76,799	94,688	12.31	11.88
R3052	40/20	56,405*	66,525*	1.90	1.73
R3051	40/20	56,405*	66,525*	1.74	1.60
R3041	33/33	56,793	40,142	1.61	1.33

*CPU/Bus Frequencies 33/33 MHz

DRAM Memory System
SRAM Memory System

CPU/Bus Frequencies		**Lin-US**	**Lin-RS**	**Lin-UD**	**Lin-RD**	**StanInt**	**StanFP**
Units =>	MHz	Kflops/S	Kflops/S	Kflops/S	Kflops/S	Time	Time
R5000-L2	180/45/45	34,674	26,432	22,220	20,448	13.92	19.19
R5000	180/45	31,278	24,461	15,539	14,669	14.42	19.69
R4700	175/44	23,745	22,029	18,914	17,455	14.52	21.74
R4650	133/44	11,884	11,260	2,103	2,048	19.76	33.22
R4640	150/50	11,478	10,895	2,082	2,044	20.42	34.00
R3081	50/25	4,898	4,912	2,362	2,408	95.20	123.2
R3052	40/22	566	560	299	301	92.27	309.1
R3051	40/22	560	557	297	298	90.70	342.0
R3041	33/33	459	450	241	203	137.10	498.8

Key to benchmark names:

Dhry-1:	Dhrystone 1.1	
Dhry-2:	Dhrystone 2.1	
Whet-S:	Whetstone,	Single Precision
Whet-D:	Whetstone,	Double Precision
Lin-US:	Linpack-c,	Unrolled, Single Precision
Lin-RS:	Linpack-c,	Rolled, Single Precision
Lin-UD:	Linpack-c,	Unrolled, Double Precision
Lin-RD:	Linpack-c,	Rolled, Double Precision
StanInt:	Stanford integer component	
StanFP:	Stanford floating point component	

Dhrystone 1.1

Part	Freq. (P/B)	Mem.	Icache	Dcache	Optimization Switches	Dhrys./S	Comments
R5000	180/45/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000	367,341	512K L2 cache
R5000	180/45/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	359,149	512K L2 cache
R5000	180/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000	367,341	L2 cache off
R5000	180/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	359,275	L2 cache off
R4700	180/45	SRAM	16K	16K	-O2 -mips3 -G 0	365,849	64-bit everything
R4700	180/45	SRAM	16K	16K	-O -mips3 -G 0	357,139	64-bit everything
R4700	100/33	SRAM	16K	16K	-O2 -mips3 -G 0	203,252	64-bit everything
R4700	100/33	SRAM	16K	16K	-O -mips3 -G 0	198,413	64-bit everything
R4650	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650	279,385	SP FPA
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -G 0 -m4650	272,516	SP FPA
R4650	100/50	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650	210,084	SP FPA
R4650	100/50	SRAM	8K	8K	-O -mips3 -G 0 -m4650	204,918	SP FPA
R4640	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650	279,401	SP FPA, 32bit external
R4640	133/44.33	SRAM	8K	8K	-O -mips3 -G 0 -m4650	272,533	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650	201,683	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O -mips3 -G 0 -m4650	196,723	SP FPA, 32bit external
R3081	50/25	SRAM	8K	8K	-O2 -mips1 -G 0	76,799	DB-Refill = 1
R3081	50/25	SRAM	8K	8K	-O -mips1 - G 0	74,289	DB-Refill = 1
R3081	33/33	SRAM	8K	8K	-O2 -mips1 -G 0	57,187	DB-Refill = 1
R3081	33/33	SRAM	8K	8K	-O -mips1 -G 0	55,550	DB-Refill = 1
R3052	33/33	SRAM	8K	2K	-O2 -mips1 -G 0	56,405	Software FP emulation
R3052	33/33	SRAM	8K	2K	-O -mips1 -G 0	54,900	Software FP emulation
R3051	33/33	SRAM	4K	2K	-O2 -mips1 -G 0	56,405	Software FP emulation
R3051	33/33	SRAM	4K	2K	-O -mips1 -G 0	54,812	Software FP emulation
R3041	33/33	SRAM	2K	0.5K	-O2 -mips1 -G 0	56,793	DB-Refill = 1
R3041	33/33	SRAM	2K	0.5K	-O -mips1 -G 0	54,812	DB-Refill = 1

Dhrystone 2.1

Part	Freq. (P/B)	Mem.	Icache	Dcache	Optimization Switches	Dhrys./S	Comments
R5000	180/45/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000	399,101	512K L2 cache
R5000	180/45/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	387,088	512K L2 cache
R5000	180/45	DRAM	32K	32K	-O2 -mips4 -G 8092 -m5000	399,102	L2 cache off
R5000	180/45	DRAM	32K	32K	-O -mips4 -G 8092 -m5000	387,086	L2 cache off
R4700	180/45	SRAM	16K	16K	-O2 -mips3 -G 8092	393,007	64-bit everything
R4700	180/45	SRAM	16K	16K	-O -mips3 -G 8092	378,941	64-bit everything
R4700	100/33	SRAM	16K	16K	-O2 -mips3 -G 8092	218,340	64-bit everything
R4700	100/33	SRAM	16K	16K	-O -mips3 -G 8092	210,526	64-bit everything
R4650	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 8092 -m4650	301,558	SP FPA
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -G 8092 -m4650	291,637	SP FPA
R4650	100/50	SRAM	8K	8K	-O2 -mips3 -G 8092 -m4650	226,758	SP FPA
R4650	100/50	SRAM	8K	8K	-O -mips3 -G 8092 -m4650	219,298	SP FPA
R4640	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 8092 -m4650	301,575	SP FPA, 32bit external
R4640	133/44.33	SRAM	8K	8K	-O -mips3 -G 8092 -m4650	291,655	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O2 -mips3 -G 8092 -m4650	217,686	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O -mips3 -G 8092 -m4650	210,525	SP FPA, 32bit external
R3081	50/25	SRAM	8K	8K	-O2 -mips1 -G 8092	94,688	DB-Refill = 1
R3081	50/25	SRAM	8K	8K	-O -mips1 -G 8092	91,567	DB-Refill = 1
R3081	33/33	SRAM	8K	8K	-O2 -mips1 -G 8092	66,525	DB-Refill = 1
R3081	33/33	SRAM	8K	8K	-O -mips1 -G 8092	64,071	DB-Refill= 1
R3052	33/33	SRAM	8K	2K	-O2 -mips1 -G 8092	66,525	Software FP emulation
R3052	33/33	SRAM	8K	2K	-O -mips1 -G 8092	64,102	Software FP emulation
R3051	33/33	SRAM	4K	2K	-O2 -mips1 -G 8092	66,525	Software FP emulation
R3051	33/33	SRAM	4K	2K	-O -mips1 -G 8092	64,071	Software FP emulation
R3041	33/33	SRAM	2K	0.5K	-O2 -mips1 -G 8092	40,142	DB-Refill = 4
R3041	33/33	SRAM	2K	0.5K	-O -mips1 -G 8092	39,142	DB-Refill = 4

Whetstone Single Precision

Part	Freq. (P/B)	Mem.	Icache	Dcache	Optimization Switches	Mwhet/S	Comments
R5000	180/45/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000 -funroll-all-loops -fomit-frame-pointer	79.18	512K L2 cache
R5000	180/45/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	75.74	512K L2 cache
R5000	180/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000 -funroll-all-loops -fomit-frame-pointer	79.19	L2 cache off
R5000	180/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	75.74	L2 cache off
R4700	180/45	SRAM	16K	16K	-O2 -mips3 -G 0 -funroll-all-loops-fomit-frame-pointer	61.64	64-bit everything
R4700	180/45	SRAM	16K	16K	-O -mips3 -G 0	59.60	64-bit everything
R4700	100/33	SRAM	16K	16K	-O2 -mips3 -G 0 -funroll-all-loops -fomit-frame-pointer	35.86	64-bit everything
R4700	100/33	SRAM	16K	16K	-O -mips3 -G 0	34.62	64-bit everything
R4650	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-all-loops -fomit-frame-pointer	20.64	SP FPA
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -G 0 -m4650	20.57	SP FPA
R4650	100/50	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-all-loops -fomit-frame-pointer	15.81	SP FPA
R4650	100/50	SRAM	8K	8K	-O -mips3 -G 0 -m4650	15.63	SP FPA
R4640	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-all-loops -fomit-frame-pointer	20.32	SP FPA 32bit external
R4640	133/44.33	SRAM	8K	8K	-O -mips3 -G 0 -m4650	20.25	SP FPA 32bit external
R4640	96/32	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-all-loops-fomit-frame-pointer	14.63	SP FPA 32bit external
R4640	96/32	SRAM	8K	8K	-O -mips3 -G 0 -m4650	14.55	SP FPA 32bit external
R3081	50/25	SRAM	8K	8K	-O2 -mips1 -G 0	12.31	DB-Refill = 1
R3081	50/25	SRAM	8K	8K	-O -mips1 -G 0	11.83	DB-Refill = 1
R3081	33/33	SRAM	8K	8K	-O2 -mips1 -G 0	8.2	DB-Refill = 1
R3081	33/33	SRAM	8K	8K	-O -mips1 -G 0	7.89	DB-Refill = 1
R3052	40/20	DRAM	8K	2K	-O2 -mips1 -G 0	1.9	Software FP emulation
R3052	40/20	DRAM	8K	2K	-O -mips1 -G 0	1.88	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O2 -mips1 -G 0	1.74	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O -mips1 -G 0	1.69	Software FP emulation
R3041	33/33	DRAM	2K	0.5K	-O2 -mips1 -G 0	1.61	DB-Refill = 4
R3041	33/33	DRAM	2K	0.5K	-O -mips1 -G 0	1.56	DB-Refill = 4

Whetstone Double Precision

Part	Freq. (P/B)	Mem.	Icache	Dcache	Optimization Switches	Mwhet/S	Comments
R5000	180/45/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000 -funroll-all-loops -fomit-frame-pointer	77.45	512K L2 cache
R5000	180/45/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	74.07	512K L2 cache
R5000	180/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000 -funroll-all-loops -fomit-frame-pointer	77.45	L2 cache off
R5000	180/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	74.07	L2 cache off
R4700	180/45	SRAM	16K	16K	-O2 -mips3 -G 0 -funroll-all-loops -fomit-frame-pointer	58.57	64-bit everything
R4700	180/45	SRAM	16K	16K	-O -mips3 -G 0	56.78	64-bit everything
R4700	100/33	SRAM	16K	16K	-O2 -mips3 -G 0 -funroll-all-loops -fomit-frame-pointer	33.99	64-bit everything
R4700	100/33	SRAM	16K	16K	-O -mips3 -G 0	32.91	64-bit everything
R4650	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-all-loops -fomit-frame-pointer	12.56	SP FPA
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -G 0 -m4650	12.49	SP FPA
R4650	100/50	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-all-loops -fomit-frame-pointer	9.44	SP FPA
R4650	100/50	SRAM	8K	8K	-O -mips3 -G 0 -m4650	9.39	SP FPA
R4640	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-all-loops -fomit-frame-pointer	12.56	SP FPA, 32bit external
R4640	133/44.33	SRAM	8K	8K	-O -mips3 -G 0 -m4650	12.49	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-all-loops -fomit-frame-pointer	9.07	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O -mips3 -G 0 -m4650	9.02	SP FPA, 32bit external
R3081	50/25	SRAM	8K	8K	-O2 -mips1 -G 0	11.88	DB-Refill = 1
R3081	50/25	SRAM	8K	8K	-O -mips1 -G 0	11.63	DB-Refill = 1
R3081	33/33	SRAM	8K	8K	-O2 -mips1 -G 0	7.9	DB-Refill = 1
R3081	33/33	SRAM	8K	8K	-O -mips1 -G 0	7.75	DB-Refill = 1
R3052	40/20	DRAM	8K	2K	-O2 -mips1 -G 0	1.73	Software FP emulation
R3052	40/20	DRAM	8K	2K	-O -mips1 -G 0	1.75	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O2 -mips1 -G 0	1.6	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O -mips1 -G 0	1.55	Software FP emulation
R3041	33/33	DRAM	2K	0.5K	-O2 -mips1 -G 0	1.33	DB-Refill = 4
R3041	33/33	DRAM	2K	0.5K	-O -mips1 -G 0	1.32	DB-Refill = 4

Stanford Integer

Part	Freq. (P/B)	Mem.	Icache	Dcache	Optimization Switches	Time	Comments
R5000	180/45/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000 -funroll-loops	13.92	512K L2 cache
R5000	180/45/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	19.19	512K L2 cache
R5000	180/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000 -funroll-loops	14.42	L2 cache off
R5000	180/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	19.69	L2 cache off
R4700	180/45	SRAM	16K	16K	-O2 -mips3 -G 0 -funroll-loops	14.52	64-bit everything
R4700	180/45	SRAM	16K	16K	-O -mips3 -G 0	21.74	64-bit everything
R4700	100/33	SRAM	16K	16K	-O2 -mips3 -G 0 -funroll-loops	25.65	64-bit everything
R4700	100/33	SRAM	16K	16K	-O -mips3 -G 0	38.63	64-bit everything
R4650	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-loops	19.67	SP FPA
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -G 0 -m4650	22.55	SP FPA
R4650	100/50	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-loops	25.41	SP FPA
R4650	100/50	SRAM	8K	8K	-O -mips3 -G 0 -m4650	29.30	SP FPA
R4640	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-loops	20.42	SP FPA, 32bit external
R4640	133/44.33	SRAM	8K	8K	-O -mips3 -G 0 -m4650	23.27	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-loops	23.27	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O -mips3 -G 0 -m4650	39.12	SP FPA, 32bit external
R3081	50/25	DRAM	8K	8K	-O2 -mips1 -G 0	95.2	DB-Refill = 4
R3081	50/25	DRAM	8K	8K	-O -mips1 -G 0	102.6	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O2 -mips1 -G 0	97.40	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O -mips1 -G 0	107.60	DB-Refill = 4
R3052	40/20	DRAM	8K	2K	-O2 -mips1 -G 0	92.27	Software FP emulation
R3052	40/20	DRAM	8K	2K	-O -mips1 -G 0	98.92	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O2 -mips1 -G 0	90.7	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O -mips1 -G 0	96.64	Software FP emulation
R3041	33/33	DRAM	2K	0.5K	-O2 -mips1 -G 0	137.10	DB-Refill = 4
R3041	33/33	DRAM	2K	0.5K	-O -mips1 -G 0	142.10	DB-Refill = 4

Stanford Floating Point

Part	Freq. (P/B)	Mem.	Icache	Dcache	Optimization Switches	Time	Comments
R5000	180/45/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000 -funroll-loops	19.19	512K L2 cache
R5000	180/45/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	23.29	512K L2 cache
R5000	180/45	DRAM	32K	32K	-O2 -mips4 -G 0 -m5000 -funroll-loops	19.69	L2 cache off
R5000	180/45	DRAM	32K	32K	-O -mips4 -G 0 -m5000	23.79	L2 cache off
R4700	180/45	SRAM	16K	16K	-O2 -mips3 -G 0 -funroll-loops	21.74	64-bit everything
R4700	180/45	SRAM	16K	16K	-O -mips3 -G 0	25.81	64-bit everything
R4700	100/33	SRAM	16K	16K	-O2 -mips3 -G 0 -funroll-loops	38.63	64-bit everything
R4700	100/33	SRAM	16K	16K	-O -mips3 -G 0	45.98	64-bit everything
R4650	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-loops	33.22	SP FPA
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -G 0 -m4650	38.35	SP FPA
R4650	100/50	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-loops	43.38	SP FPA
R4650	100/50	SRAM	8K	8K	-O -mips3 -G 0 -m4650	50.26	SP FPA
R4640	133/44.33	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-loops	34.00	SP FPA, 32bit external
R4640	133/44.33	SRAM	8K	8K	-O -mips3 -G 0 -m4650	39.12	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O2 -mips3 -G 0 -m4650 -funroll-loops	47.23	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O -mips3 -G 0 -m4650	54.31	SP FPA, 32bit external
R3081	50/25	DRAM	8K	8K	-O2 -mips1 -G 0	123.20	DB-Refill = 4
R3081	50/25	DRAM	8K	8K	-O -mips1 -G 0	135.90	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O2 -mips1 -G 0	131.20	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O -mips1 -G 0	150.50	DB-Refill = 4
R3052	40/20	DRAM	8K	2K	-O2 -mips1 -G 0	309.10	Software FP emulation
R3052	40/20	DRAM	8K	2K	-O -mips1 -G 0	322.26	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O2 -mips1 -G 0	342.00	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O -mips1 -G 0	352.00	Software FP emulation
R3041	33/33	DRAM	2K	0.5K	-O2 -mips1 -G 0	498.80	DB-Refill = 4
R3041	33/33	DRAM	2K	0.5K	-O -mips1 -G 0	511.10	DB-Refill = 4

Linpack Rolled Double Precision

Part	Freq. (P/B)	Mem.	Icache	Dcache	Optimization Switches	Kflops/S	Comments
R5000	180/45/45	DRAM	32K	32K	-O2 -mips4 -m5000	20,448	512K L2 cache
R5000	180/45/45	DRAM	32K	32K	-O -mips4 -m5000		512K L2 cache
R5000	180/45	DRAM	32K	32K	-O2 -mips4 -m5000	14,669	L2 cache off
R5000	180/45	DRAM	32K	32K	-O -mips4 -m5000		L2 cache off
R4700	180/45	SRAM	16K	16K	-O2 -mips3	17,445	64-bit everything
R4700	180/45	SRAM	16K	16K	-O -mips3	14,584	64-bit everything
R4700	100/33	SRAM	16K	16K	-O2 -mips3	10,520	64-bit everything
R4700	100/33	SRAM	16K	16K	-O -mips3	8,519	64-bit everything
R4650	133/44.33	SRAM	8K	8K	-O2 -mips3 -m4650	2,048	SP FPA
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -m4650	1,976	SP FPA
R4650	100/50	SRAM	8K	8K	-O2 -mips3 -m4650	1,554	SP FPA
R4650	100/50	SRAM	8K	8K	-O -mips3 -m4650	1,503	SP FPA
R4640	133/44.33	SRAM	8K	8K	-O2 -mips3 -m4650	2,029	SP FPA, 32bit external
R4640	133/44.33	SRAM	8K	8K	-O -mips3 -m4650	1,959	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O2 -mips3 -m4650	1,466	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O -mips3 -m4650	1,414	SP FPA, 32bit external
R3081	50/25	DRAM	8K	8K	-O2 -mips1 -G 2048 -fomit-frame-pointer	2,408	DB-Refill = 4
R3081	50/25	DRAM	8K	8K	-O -mips1	2,352	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O2 -mips1 -G 2048 -fomit-frame-pointer	2,744	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O -mips1	2,294	DB-Refill = 4
R3052	40/20	DRAM	8K	2K	-O2 -mips1 -G 2048 -fomit-frame-pointer	301	Software FP emulation
R3052	40/20	DRAM	8K	2K	-O -mips1	290	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O2 -mips1 -G 2048 -fomit-frame-pointer	298	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O -mips1	288	Software FP emulation
R3041	33/33	DRAM	2K	0.5K	-O2 -mips1 -G 2048	203	DB-Refill = 4
R3041	33/33	DRAM	2K	0.5K	-O -mips1	155	DB-Refill = 4

Linpack Unrolled Double Precision

Part	Freq. (P/B)	Mem.	Icache	Dcache	Optimization switches	Kflops/S	Comments
R5000	180/45/45	DRAM	32K	32K	-O2 -mips4 -m5000	22,220	512K L2 cache
R5000	180/45/45	DRAM	32K	32K	-O -mips4 -m5000		512K L2 cache
R5000	180/45	DRAM	32K	32K	-O2 -mips4 -m5000	15,539	L2 cache off
R5000	180/45	DRAM	32K	32K	-O -mips4 -m5000		L2 cache off
R4700	180/45	SRAM	16K	16K	-O2 -mips3	18,914	64-bit everything
R4700	180/45	SRAM	16K	16K	-O2 -mips3	17,809	64-bit everything
R4700	100/33	SRAM	16K	16K	-O -mips3	11,276	64-bit everything
R4700	100/33	SRAM	16K	16K	-O2 -mips3	10,276	64-bit everything
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -m4650	2,103	SP FPA
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -m4650	2,063	SP FPA
R4650	100/50	SRAM	8K	8K	-O2 -mips3 -m4650	1,598	SP FPA
R4650	100/50	SRAM	8K	8K	-O -mips3 -m4650	1,564	SP FPA
R4640	133/44.33	SRAM	8K	8K	-O2 -mips3 -m4650	2,082	SP FPA, 32bit external
R4640	133/44.33	SRAM	8K	8K	-O -mips3 -m4650	2,044	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O2 -mips3 -m4650	1,495	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O -mips3 -m4650	1,476	SP FPA, 32bit external
R3081	50/25	DRAM	8K	8K	-O2 -mips1 -G 2048 -fomit-frame-pointer	2,362	DB-Refill = 4
R3081	50/25	DRAM	8K	8K	-O -mips1	2,346	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O2 -mips1 -G 2048 -fomit-frame-pointer	2,744	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O -mips1	2,294	DB-Refill = 4
R3052	40/20	DRAM	8K	2K	-O2 -mips1 -G 2048 -fomit-frame-pointer	299	Software FP emulation
R3052	40/20	DRAM	8K	2K	-O -mips1	296	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O2 -mips1 -G 2048 -fomit-frame-pointer	297	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O -mips1	293	Software FP emulation
R3041	33/33	DRAM	2K	0.5K	-O2 -mips1 -G 2048	241	DB-Refill = 4
R3041	33/33	DRAM	2K	0.5K	-O -mips1	183	DB-Refill = 4

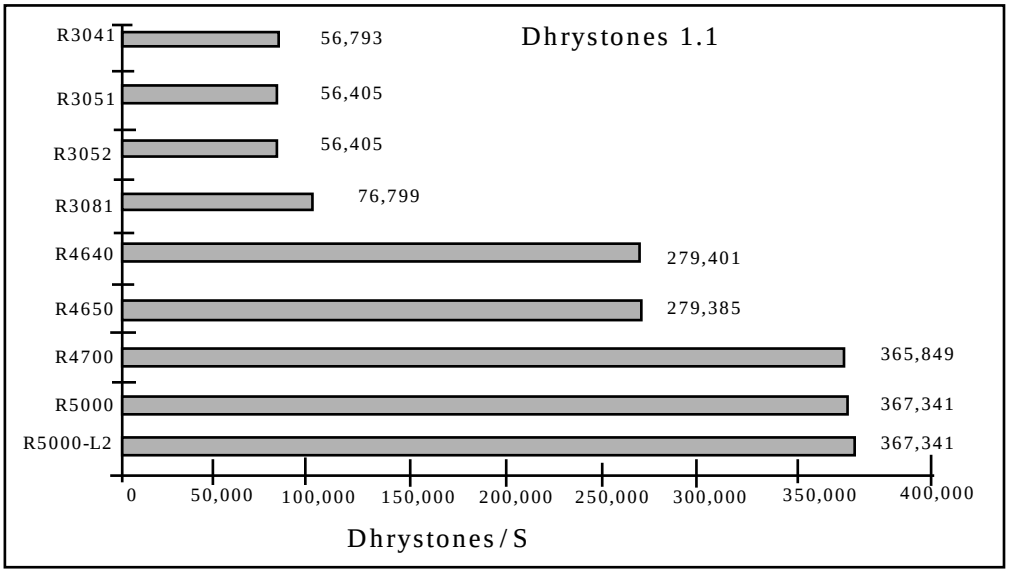
Linpack Rolled Single Precision

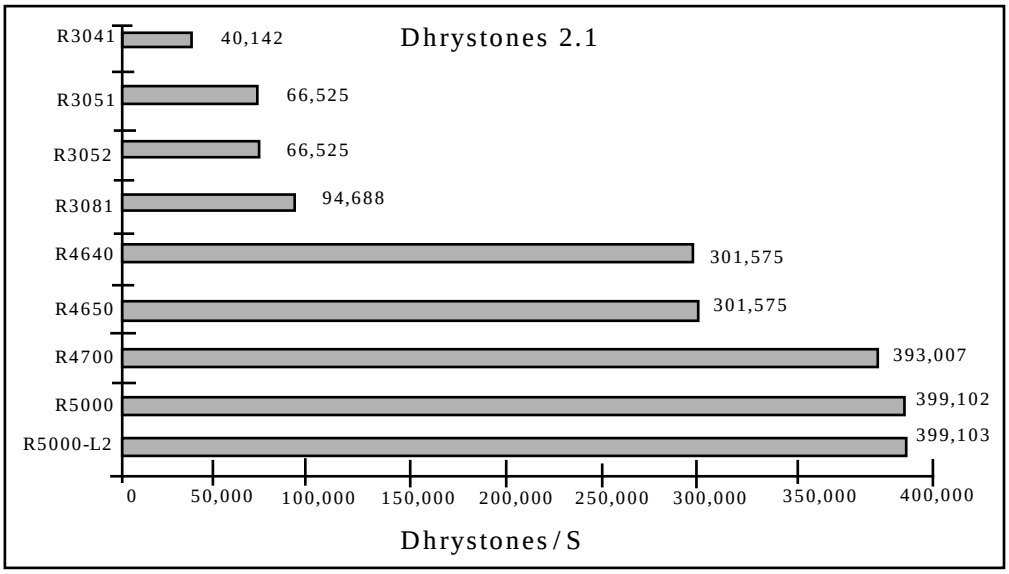
Part	Freq. (P/B)	Mem.	Icache	Dcache	Optimization switches	Kflops/S	Comments
R5000	180/45/45	DRAM	32K	32K	-O2 -mips4 -m5000	26,432	512K L2 cache
R5000	180/45/45	DRAM	32K	32K	-O -mips4 -m5000		512K L2 cache
R5000	180/45	DRAM	32K	32K	-O2 -mips4 -m5000	24,461	L2 cache off
R5000	180/45	DRAM	32K	32K	-O -mips4 -m5000		L2 cache off
R4700	180/45	SRAM	16K	16K	-O2 -mips3	22,029	64-bit everything
R4700	180/45	SRAM	16K	16K	-O -mips3	22,028	64-bit everything
R4700	100/33	SRAM	16K	16K	-O2 -mips3	12,633	64-bit everything
R4700	100/33	SRAM	16K	16K	-O -mips3	11,726	64-bit everything
R4650	133/44.33	SRAM	8K	8K	-O2 -mips3 -m4650	11,260	SP FPA
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -m4650	10,724	SP FPA
R4650	100/50	SRAM	8K	8K	-O2 -mips3 -m4650	8,753	SP FPA
R4650	100/50	SRAM	8K	8K	-O -mips3 -m4650	8,361	SP FPA
R4640	133/44.33	SRAM	8K	8K	-O2 -mips3 -m4650	10,895	SP FPA, 32bit external
R4640	133/44.33	SRAM	8K	8K	-O -mips3 -m4650	10,418	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O2 -mips3 -m4650	7,851	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O -mips3 -m4650	7,476	SP FPA, 32bit external
R3081	50/25	DRAM	8K	8K	-O2 -mips1 -G 2048 -fomit-frame-pointer	4,912	DB-Refill = 4
R3081	50/25	DRAM	8K	8K	-O -mips1	4,354	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O2 -mips1 -G 2048 -fomit-frame-pointer	4,340	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O -mips1	3,431	DB-Refill = 4
R3052	40/20	DRAM	8K	2K	-O2 -mips1 -G 2048 -fomit-frame-pointer	560	Software FP emulation
R3052	40/20	DRAM	8K	2K	-O -mips1	533	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O2 -mips1 -G 2048 -fomit-frame-pointer	557	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O -mips1	531	Software FP emulation
R3041	33/33	DRAM	2K	0.5K	-O2 -mips1 -G 2048	450	DB-Refill = 4
R3041	33/33	DRAM	2K	0.5K	-O -mips1	420	DB-Refill = 4

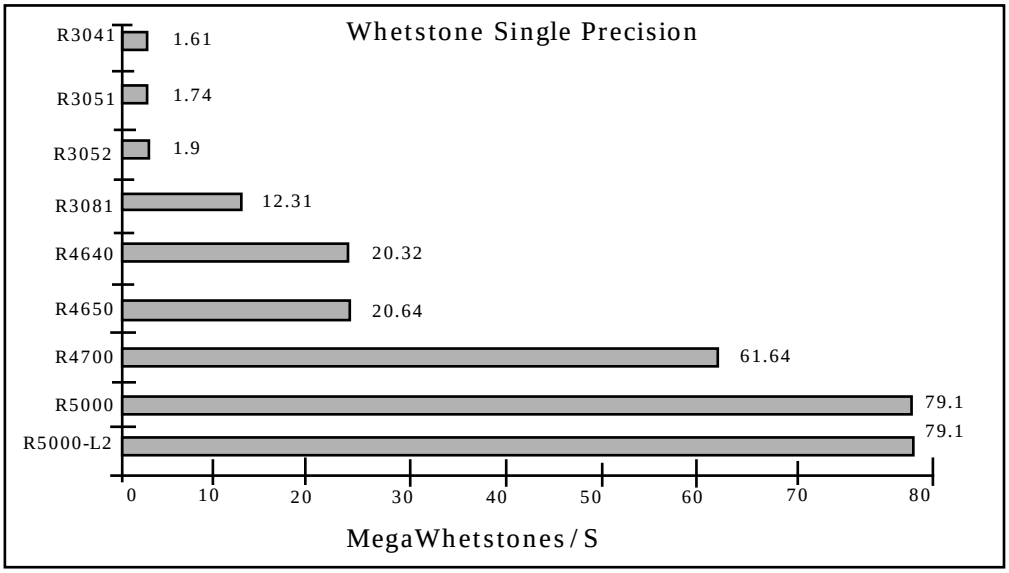
Linpack Unrolled Single Precision

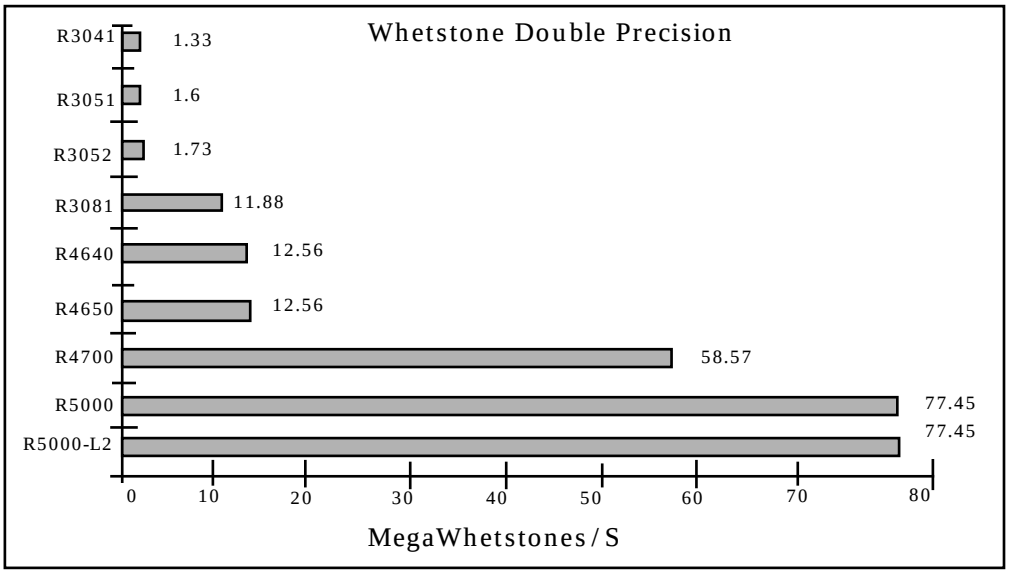
Part	Freq. (P/B)	Mem.	Icache	Dcache	Optimization Switches	Kflops/S	Comments
R5000	180/45/45	DRAM	32K	32K	-O2 -mips4 -m5000	34,674	512K L2 cache
R5000	180/45/45	DRAM	32K	32K	-O -mips4 -m5000		512K L2 cache
R5000	180/45	DRAM	32K	32K	-O2 -mips4 -m5000	31,278	L2 cache off
R5000	180/45	DRAM	32K	32K	-O -mips4 -m5000		L2 cache off
R4700	180/45	SRAM	16K	16K	-O2 -mips3	23,745	64-bit everything
R4700	180/45	SRAM	16K	16K	-O -mips3	23,227	64-bit everything
R4700	100/33	SRAM	16K	16K	-O2 -mips3	13,630	64-bit everything
R4700	100/33	SRAM	16K	16K	-O -mips3	13,309	64-bit everything
R4650	133/44.33	SRAM	8K	8K	-O2 -mips3 -m4650	11,884	SP FPA
R4650	133/44.33	SRAM	8K	8K	-O -mips3 -m4650	11,617	SP FPA
R4650	100/50	SRAM	8K	8K	-O2 -mips3 -m4650	9,281	SP FPA
R4650	100/50	SRAM	8K	8K	-O -mips3 -m4650	9,100	SP FPA
R4640	133/44.33	SRAM	8K	8K	-O2 -mips3 -m4650	11,478	SP FPA, 32bit external
R4640	133/44.33	SRAM	8K	8K	-O -mips3 -m4650	11,266	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O2 -mips3 -m4650	8,234	SP FPA, 32bit external
R4640	96/32	SRAM	8K	8K	-O -mips3 -m4650	8,051	SP FPA, 32bit external
R3081	50/25	DRAM	8K	8K	-O2 -mips1 -G 2048 -fomit-frame-pointer	4,898	DB-Refill = 4
R3081	50/25	DRAM	8K	8K	-O -mips1	4,763	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O2 -mips1 -G 2048 -fomit-frame-pointer	4,308	DB-Refill = 4
R3081	33/33	DRAM	8K	8K	-O -mips1	3,940	DB-Refill = 4
R3052	40/20	DRAM	8K	2K	-O2 -mips1 -G 2048 -fomit-frame-pointer	566	Software FP emulation
R3052	40/20	DRAM	8K	2K	-O -mips1	555	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O2 -mips1 -G 2048 -fomit-frame-pointer	560	Software FP emulation
R3051	40/20	DRAM	4K	2K	-O -mips1	544	Software FP emulation
R3041	33/33	DRAM	2K	0.5K	-O2 -mips1 -G 2048	459	DB-Refill = 4
R3041	33/33	DRAM	2K	0.5K	-O -mips1	443	DB-Refill = 4

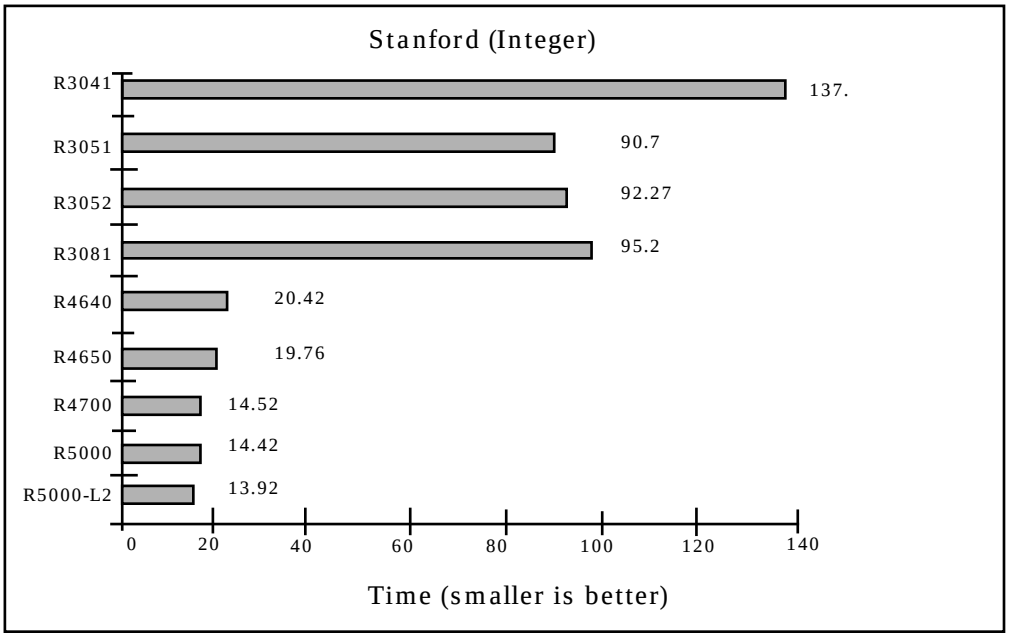
Result Graphs

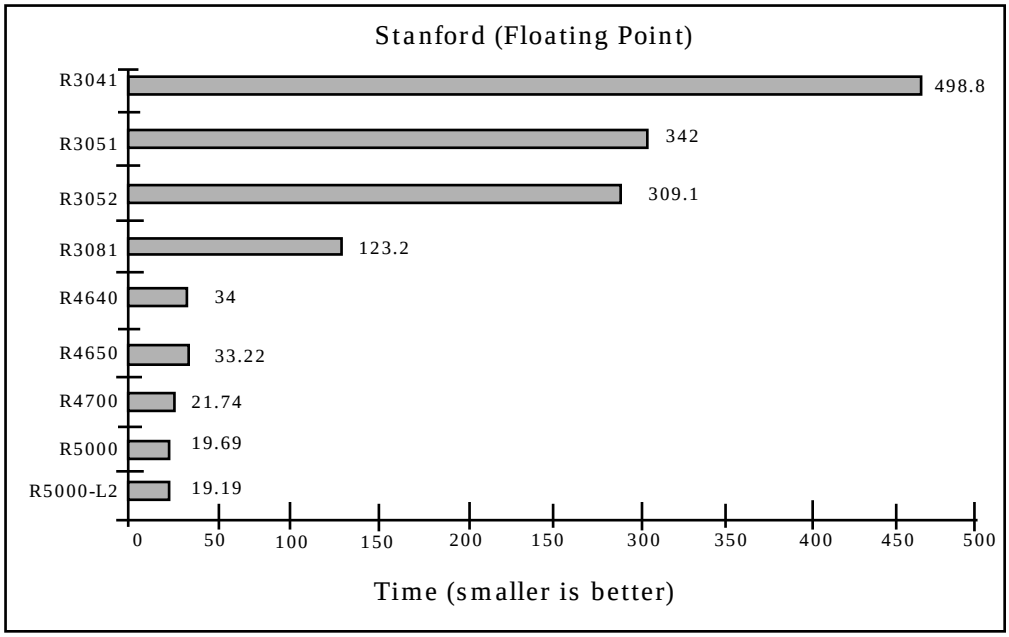


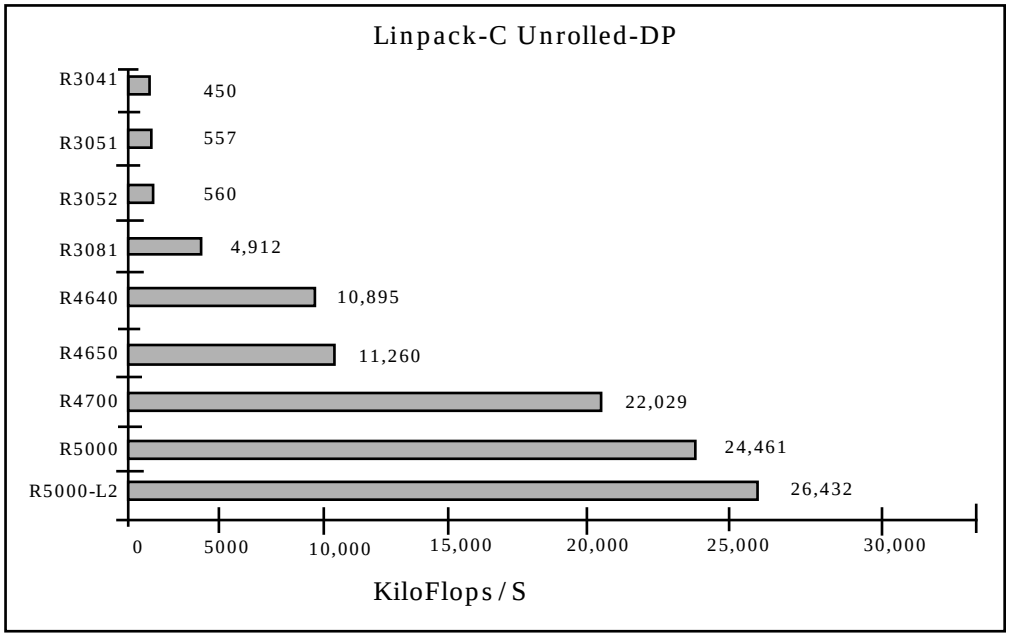


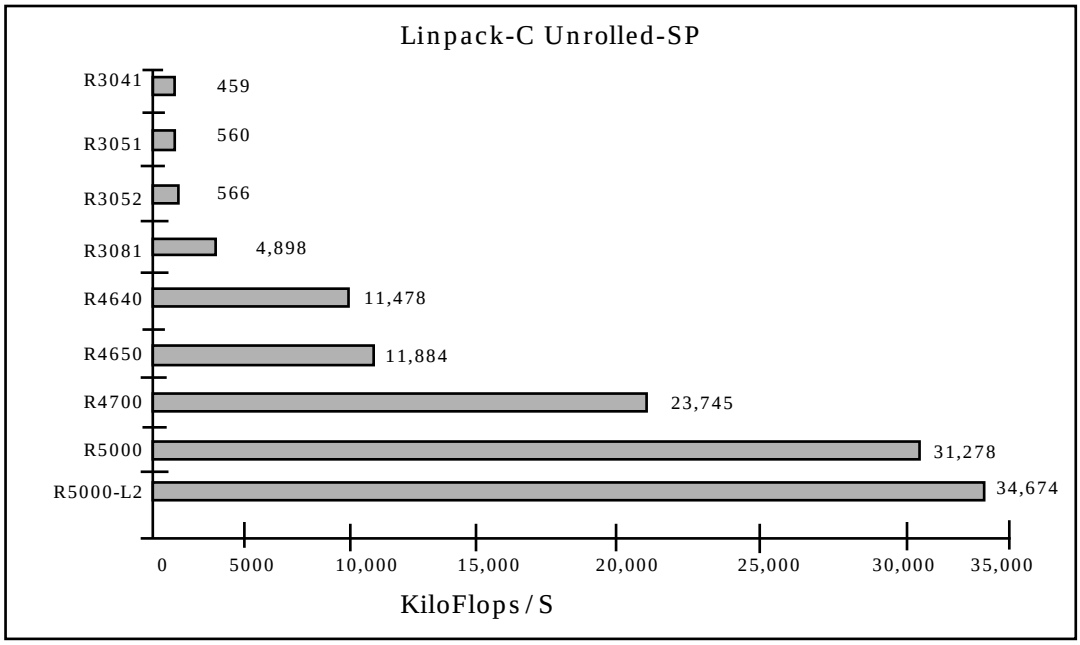

Whetstone Single Precision
R3041
1.61
R3051
1.74
R3052
1.9
R3081
12.31
R4640
20.32
R4650
20.64
R4700
61.64
R5000
79.1
R5000-L2
79.1
0
10
20
30
40
50
60
70
80
MegaWhetstones/S

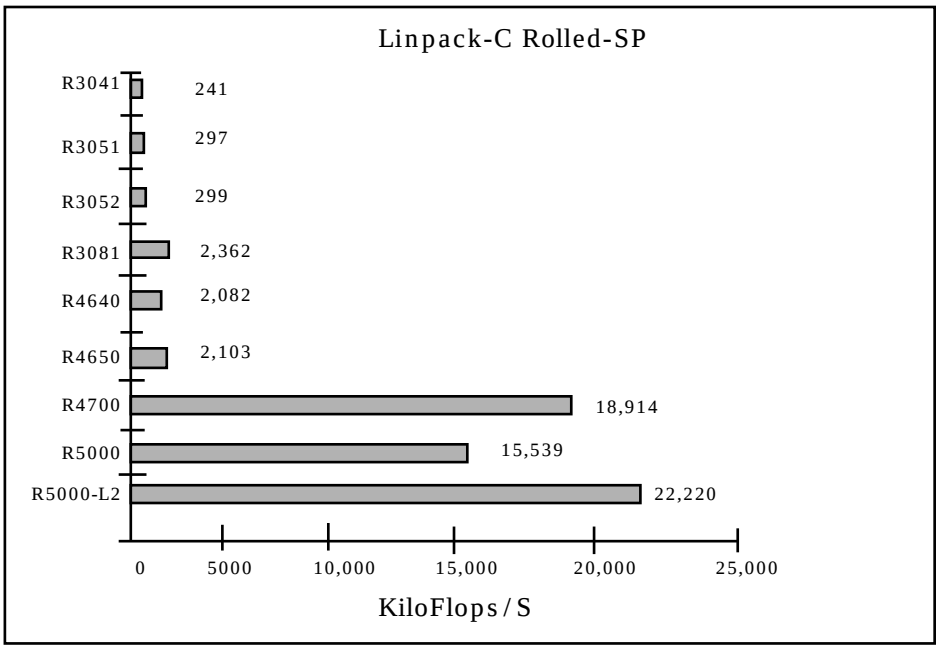

Whetstone Double Precision
R3041
1.33
R3051
1.6
R3052
1.73
R3081
11.88
R4640
12.56
R4650
12.56
R4700
58.57
R5000
77.45
R5000-L2
77.45
0
10
20
30
40
50
60
70
80
MegaWhetstones/S

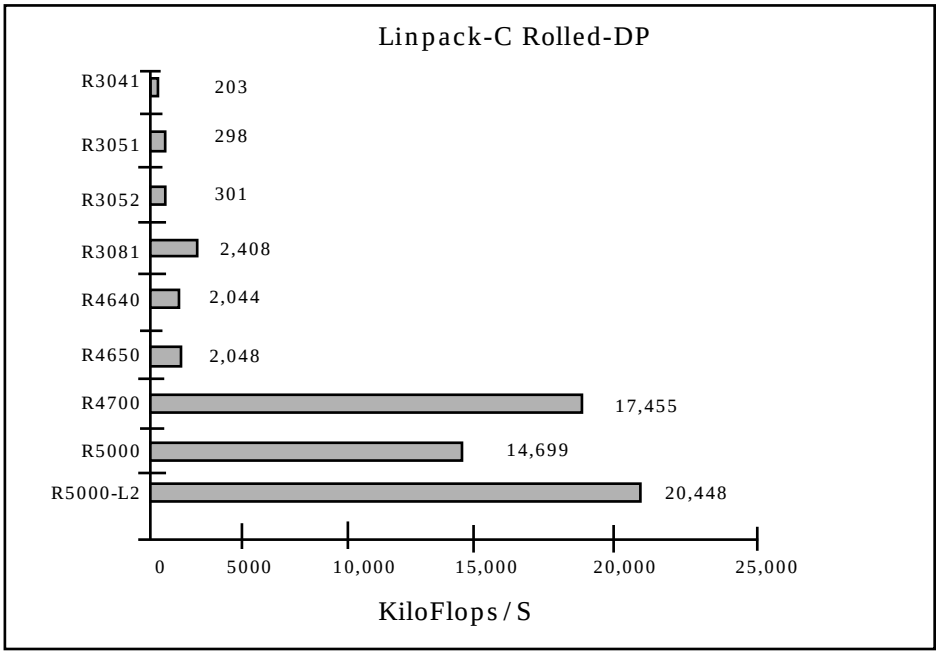

Stanford (Integer)
R3041
R3051
R3052
R3081
R4640
R4650
R4700
R5000
R5000-L2
137.
90.7
92.27
95.2
20.42
19.76
14.52
14.42
13.92
0
20
40
60
80
100
120
140
Time (smaller is better)


Stanford (Floating Point)
R3041
R3051
R3052
R3081
R4640
R4650
R4700
R5000
R5000-L2
498.8
342
309.1
123.2
34
33.22
21.74
19.69
19.19
0
50
100
150
200
150
300
350
400
450
500
Time (smaller is better)


Linpack-C Unrolled-DP
R3041
450
R3051
557
R3052
560
R3081
4,912
R4640
10,895
R4650
11,260
R4700
22,029
R5000
24,461
R5000-L2
26,432
0
5000
10,000
15,000
20,000
25,000
30,000
KiloFlops/S


Linpack-C Unrolled-SP
R3041
459
R3051
560
R3052
566
R3081
4,898
R4640
11,478
R4650
11,884
R4700
23,745
R5000
31,278
R5000-L2
34,674
0
5000
10,000
15,000
20,000
25,000
30,000
35,000
KiloFlops/S


Linpack-C Rolled-SP
R3041
241
R3051
297
R3052
299
R3081
2,362
R4640
2,082
R4650
2,103
R4700
18,914
R5000
15,539
R5000-L2
22,220
0
5000
10,000
15,000
20,000
25,000
KiloFlops/S


Linpack-C Rolled-DP
R3041
203
R3051
298
R3052
301
R3081
2,408
R4640
2,044
R4650
2,048
R4700
17,455
R5000
14,699
R5000-L2
20,448
0
5000
10,000
15,000
20,000
25,000
KiloFlops/S