EK-PC300-V1-001

Professional™ 300 Series

Technical Manual
Volume I
Kernel System

Digital Equipment Corporation

First Edition, June 1985

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INTRODUCTION

This manual documents system design concepts and hardware functions for the Professional 300 Series computer system. All hardware descriptions provide functional information on primary signal flow. This document does not include information on software programming.

Refer to the Related Documentation section for a listing of hardware and software documents that apply to the Professional 300 Series computer system.

Manual Organization
This hardware document set is divided into two volumes. Volume I contains all information regarding the kernel Professional 300 series system, including information on the Professional 325, Professional 350, and Professional 380. Volume II contains information on Professional 300 series option modules and accessories.

The following is a brief description of the Professional 300 Series Technical Manual, Volume I, Kernel System.

Chapter 1 – System Introduction describes the Professional 325, 350, and 380 systems. It also describes differences between the three systems and provides hardware specifications for each.

Chapter 2 – System Installation explains how to prepare the system site to install the Professional 300 Series system. It also provides information on cleaning the equipment and handling the diskettes.

Chapter 3 – Controls and Indicators describes all controls and indicators and their functions.

Chapter 4 – System Overview describes how the Professional 300 series system operates.

Chapter 5 – Professional 350 System Module describes the Professional 350 system module.

Chapter 6 – Professional 380 System Module describes the Professional 380 system module.

Chapter 7 – Bit Map Video Controller and Extended Bit Map Modules describes the bit map video controller module and extended bit map option module.

Chapter 8 – VR201 Monochrome Monitor describes the VR201 monitor.

Chapter 9 – LK201 Keyboard describes the LK201 keyboard and how it operates and interfaces with the Professional 300 system.

Chapter 10 – H7862 Power Supply describes the Professional 300 Series power supply and its operation.

Chapter 11 – System Memory and Memory Daughter Modules describes the RAM memory that is on-board the system module and the various memory daughter modules available as memory options to the Professional 300 series system.

The following describes the Professional 300 Series Technical Manual, Volume II, System Options.

Chapter 1 – Telephone Management System describes the telephone management system, including the voice unit.

Chapter 2 – CP/M 80 Option Module describes the CP/M 80 operating system module and how it interacts within the Professional 300 system.

Chapter 3 – DECNA Option Module describes the Digital Ethernet CTI Bus network adaptor; how it connects to other devices and how it operates within the host system.

Chapter 4 – Professional 380 Extended Bit Map Option Module describes the extended bit map option (EBO) module for the Professional 380. Connector pin assignments are also provided.

Chapter 5 – RD50 Hard Disk Drive Controller describes the RD50 hard drive controller module. A functional description of each circuit is provided.

Chapter 6 – RD50 Hard Disk Drive describes the RD50 hard disk drive operation. Removal/replacement procedures for the hard drive read/write module are also provided.

Chapter 7 – RX50 Controller Module provides functional and detailed descriptions of each circuit of the RX50 controller.

Chapter 8 – RX50 Dual-Diskette Drive describes the operation of the RX50 diskette drive.

Chapter 9 – RD52 Hard Disk Drive provides functional and detailed descriptions of the RD52 hard disk drive. Specifications for the RD52 are also included.

Related Documentation
The following is a list of documents related to the Professional 300 Series Technical Manual two-volume document set.

Professional 350 Pocket Service Guide	EK-PC350-PS
Professional 350 Illustrated Parts Breakdown	EK-PC350-IP
Professional 300 Series Owner Manual	AA-N587A-TH
Professional 300 Series Installation Guide	AZ-N626A-TH
Professional 350 User Guide For Hard Disk Systems	AA-N603A-TH
Professional 350 Field Maintenance Print Set	MP-01394-00
VR201 Field Maintenance Print Set	MP-01410-00
LK201 Field Maintenance Print Set	MP-01395-00
KEF11 Field Maintenance Print Set	MP-01473-00
Professional 380 Field Maintenance Print Set	~~MP-01957-01~~ MP-01922-01

CHAPTER 1
SYSTEM INTRODUCTION

1.1 PROFESSIONAL 300 SERIES SYSTEM DESCRIPTION

The following paragraphs provide a physical description of the Professional 300 Series computer. The kernel system consists of the following three hardware assemblies (Figure 1-1).

1. System unit
2. Video monitor
3. Keyboard

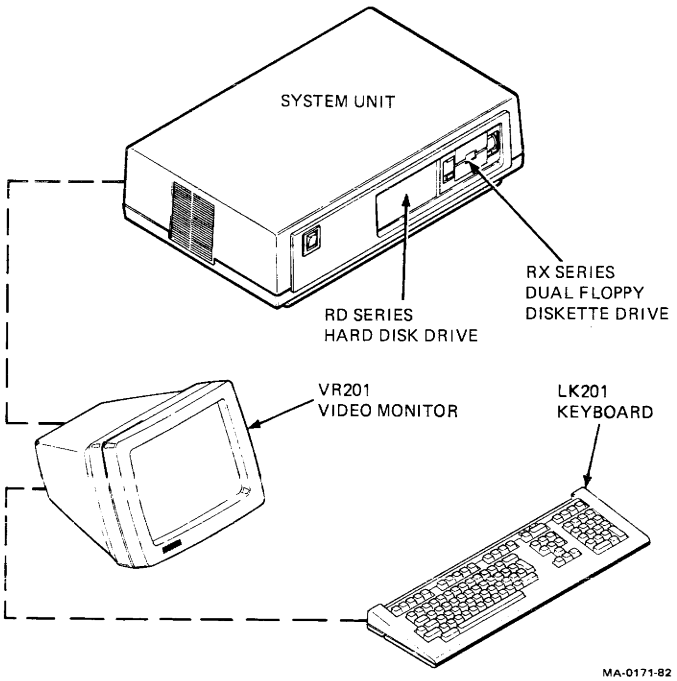


Figure 1-1 The Professional 300 Series Computer System

1.1.1 System Unit

The Professional 300 Series system unit contains the following components.

1. System Module – The system module is central to the entire computer system. It is a printed circuit board mounted on a metal plate that slides in and out of the bottom of the Professional enclosure. The system module contains all the control and interface electronics needed to support the microprocessor chip set mounted on the system module.

2. RD Hard Disk Drive – The system unit contains the RD series hard disk drive. It is a winchester-based hard disk drive that provides up to 32 megabytes of formatted storage. The RD drive is an option to both units.

3. RX50 Dual Diskette Drive – The system unit also contains the RX50 dual diskette drive. This is a dual diskette storage unit that provides 819 kilobytes of formatted storage on removable diskettes.

1.1.2 Video Monitor

The video monitor provides the system display. It is a 12 inch diagonal monochrome monitor that has an adjustable tilt for operator viewing comfort and two display controls on the rear panel to adjust brightness and contrast.

1.1.3 Keyboard

The operator uses the keyboard to enter data into the system. The keyboard contains three keypads (main, editing, and numeric) and a series of special function keys.

1.1.4 Professional 300 Series System Differences

Table 1-1 shows the differences between the Professional 325, 350, and 380 computer systems.

NOTE

Except for the differences that are described here, the Professional 325 and Professional 350 are identical in configuration and operation. All discussions pertaining to the Professional 350 computer system also apply to the Professional 325 computer system unless otherwise noted.

Table 1-1 Professional 300 Series System Differences

Category	System 325	350	380
RX Diskette Drive System	yes	yes	yes
CTI Bus user-available option slots (floppy-based monochrome system)	1	3	5
RD Hard Disk Drive System Option	no	yes	yes
Operating System downloading ability (LAN – Local Area Network)	no	yes	yes
Hard Disk-Based Operating System	no	yes	yes
Floppy Diskette Based Operating System	yes	yes	yes

1.2 SYSTEM SPECIFICATIONS

The general system specifications for the Professional 350 and 380 are listed below. Additional specifications for each component or option modules are supplied in the appropriate chapters.

SYSTEM UNIT

Functional

Professional 350 microprocessor	Digital F-11 chip set (CPU)
Professional 380 microprocessor	Digital J11 chip set (CPU)
Diagnostics	Built-in power-up self-test
Memory	Capable of addressing up to 3 megabytes
Video output	RS170-compatible, monochrome, bitmap graphics
Communications port	RS423 asynchronous/byte, up to 19.2 kilobaud with modem control
Printer port	Serial, RS423
Removable storage	Dual diskette drive. 5.25 in (13.3 cm) diskettes. 819 kilobytes total
Fixed storage (optional)	Up to 32 megabytes, 5.25 in (13.3 cm) hard disk drive, further capability as offered in RD series

Professional 350 system expansion, floppy-based system	3 option slots, user installable. Slots 1 and 2 are used for the RD and RX disk drive controllers.
Professional 380 system expansion, floppy-based	5 option slots, user installable.
Power	
Power supply type	Transistor, switch type ac to dc converter
Vac input	Switch selectable
115 V nominal	Single-phase, 3-wire 90 to 128 V rms, 47 to 63 Hz line frequency
230 V nominal	Single-phase, 3-wire, 174 to 256 V rms, 47 to 63 Hz line frequency
Line current	6 A @ 115 Vac 4 A @ 230 Vac
Power consumption	320 watts maximum
Circuit protection	Circuit breaker, externally accessible
Physical	
Height	16.5 cm (6.5 in)
Length	55.8 cm (22 in)
Width	34.3 cm (14.3 in)
Maximum Weight	15.9 kg (35 lb)

KEYBOARD

Functional	
Electronics	8-bit microprocessor, 4 kilobytes of ROM, 256 bytes of RAM, 4 indicators, transducer
Diagnostics	Power-up self-test
Keypads	
Main keypad	57 keys
Numeric keypad	18 keys
Special function keys	20 keys
Editing keypad	10 keys

Physical

Height	5 cm (2.0 in) at highest point
Length	53.3 cm (21 in)
Width	17.1 cm (6.75 in)
Weight	2 kg (4.5 lb)
Home row key height	30 mm above desktop

MONOCHROME MONITOR

Functional

Character format	24 lines × 80/132 characters per line software driven
Video format	Monochrome composite

Physical

Height	24.38 cm (9.75 in)
Width	29.33 cm (11.73 in)
Depth	30.57 cm (12.23 in)
Diagonal	305 cm (12 in) diagonally measured CRT
Weight	6.6 kg (14.5 lb)
Adjustable tilt	+5 to −25 degrees

RX50 DUAL DISKETTE DRIVE SUBSYSTEM

Performance

Formatted capacity	819 kilobytes
Diskettes per drive	2
Transfer rate	250 kilobits/s
Average access time	290 ms

Functional

Density	96 tracks/in

Physical

Height	8.4 cm (3.25 in)
Width	14.7 cm (5.75 in)
Depth	21.6 cm (8.5 in)
Weight	2.17 kg (4.8 lb)

RD50 HARD DISK DRIVE SUBSYSTEM

Performance	
Formatted capacity	5 megabytes
Transfer rate	5 megabits/s
Average access time	170 ms
Functional	
Density	255 tracks/in
Physical	
Height	8.25 cm (3.25 in)
Width	14.6 cm (5.75 in)
Depth	20.4 cm (8 in)
Weight	2.3 kg (5 lb)

RD51 HARD DISK DRIVE SUBSYSTEM

Performance	
Formatted capacity	10 megabytes
Transfer rate	5 megabits/s
Average access time	85 ms
Functional	
Density	345 tracks/in
Physical	
Height	8.25 cm (3.25 in)
Width	14.6 cm (5.75 in)
Depth	20.4 cm (8 in)
Weight	2.3 kg (5 lb)

RD52 HARD DISK DRIVE SUBSYSTEM

Performance	
Formatted capacity	32 megabytes
Transfer rate	5 megabits/s
Average access time	37.5 ms
Functional	
Density	695 tracks/in
Physical	
Height	8.25 cm (3.25 in)
Width	14.6 cm (5.75 in)
Depth	20.4 cm (8 in)
Weight	3.18 kg (7 lbs)

CHAPTER 2
SYSTEM INSTALLATION

2.1 INTRODUCTION
The Professional 300 Series computer system is customer-installable. Chapter 2 contains the following information.

1. Site preparation
2. Installation
3. System upkeep

2.2 SITE PREPARATION
Before installing the computer system, check the spacing, lighting, power, and environmental requirements.

2.2.1 Space
When positioning the Professional use these guidelines.

1. Allow six inches on all sides of the computer for adequate airflow.
2. Keep all ventilation ports clear.
3. Allow room for the placement of peripheral devices.
4. Place all cables away from traffic areas.

2.2.2 Lighting
Place the system unit and the video monitor away from direct sunlight to minimize heat and glare.

2.2.3 Power
The following are the power requirements.

1. Input voltage – 115 or 230 Vac
2. Line frequency – 47 to 63 Hz
3. Power consumption – 320 watts maximum

2.2.4 Environment
The following are environmental requirements.

1. Temperature – 10° to 40°C (50° to 104°F)
2. Humidity – 20% to 80% relative humidity
3. Maximum wet bulb of 25°C
   Minimum dew point of 2°C

2.3 PROFESSIONAL 300 SERIES SYSTEM INSTALLATION

This section describes how to install the Professional system and its options.

NOTE

The following procedures summarize the instructions in the Professional 300 Series Installation Guide (AZ-N626A-TH). Refer to this guide for complete installation procedures for the Professional 350. For the Professional 380, refer to the Professional Installation Instructions booklet (AV-C145A-TH).

2.3.1 Packaging

The Professional system is shipped in four containers. Each contains one of the following elements.

1. System unit
2. Software – including the Professional 300 Series Installation Guide
3. Video monitor – including a monitor cable
4. Keyboard – including a keyboard cable

2.3.2 Installing the Professional

Use the following steps to install the Professional computer system.

1. Unpack the system and place each component on the work area surface.

2. Connect the video monitor cable to the back of the system unit (Figure 2-1) and to the back of the video monitor (Figure 2-2).

3. Connect the keyboard to the back of the monitor (Figure 2-2).

4. Set the voltage select switch on the back of the system unit to the correct operating voltage (115 or 230/240 Vac).

5. Remove the shipping card from the diskette drive. To do so, open the door and slide the card out.

6. Make sure that the system unit power switch is set to the off position (0). Connect the power cord to the system unit and plug it into the nearest wall outlet.

2.3.3 Additional Equipment

The following are the options/modules for the Professional.

1. Printed circuit board (PCB) modules
2. Mass storage options

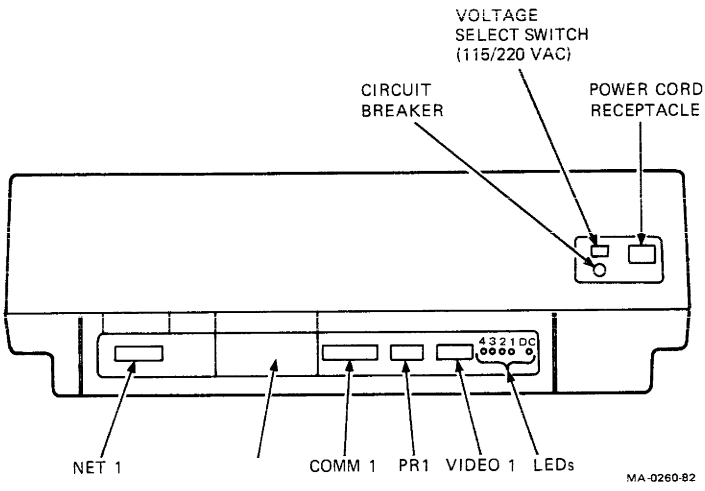


Figure 2-1 Professional 300 Series System Unit Rear Panel

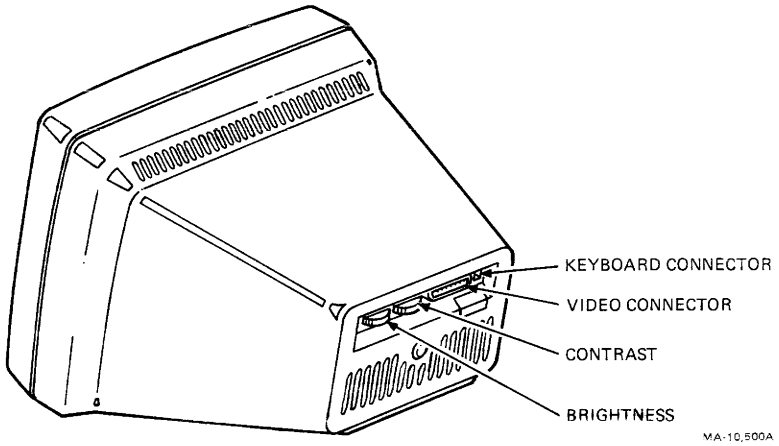


Figure 2-2 Professional 300 Series Monitor Rear Panel

2.3.3.1 Top Cover Removal – Use the following steps to remove the top cover.

1. Set the system unit power switch to off (0).
2. Unplug the power cord and disconnect all cables from the rear of the system unit.
3. Slide the top cover release tabs forward and out and lift the cover straight up (Figure 2-3).

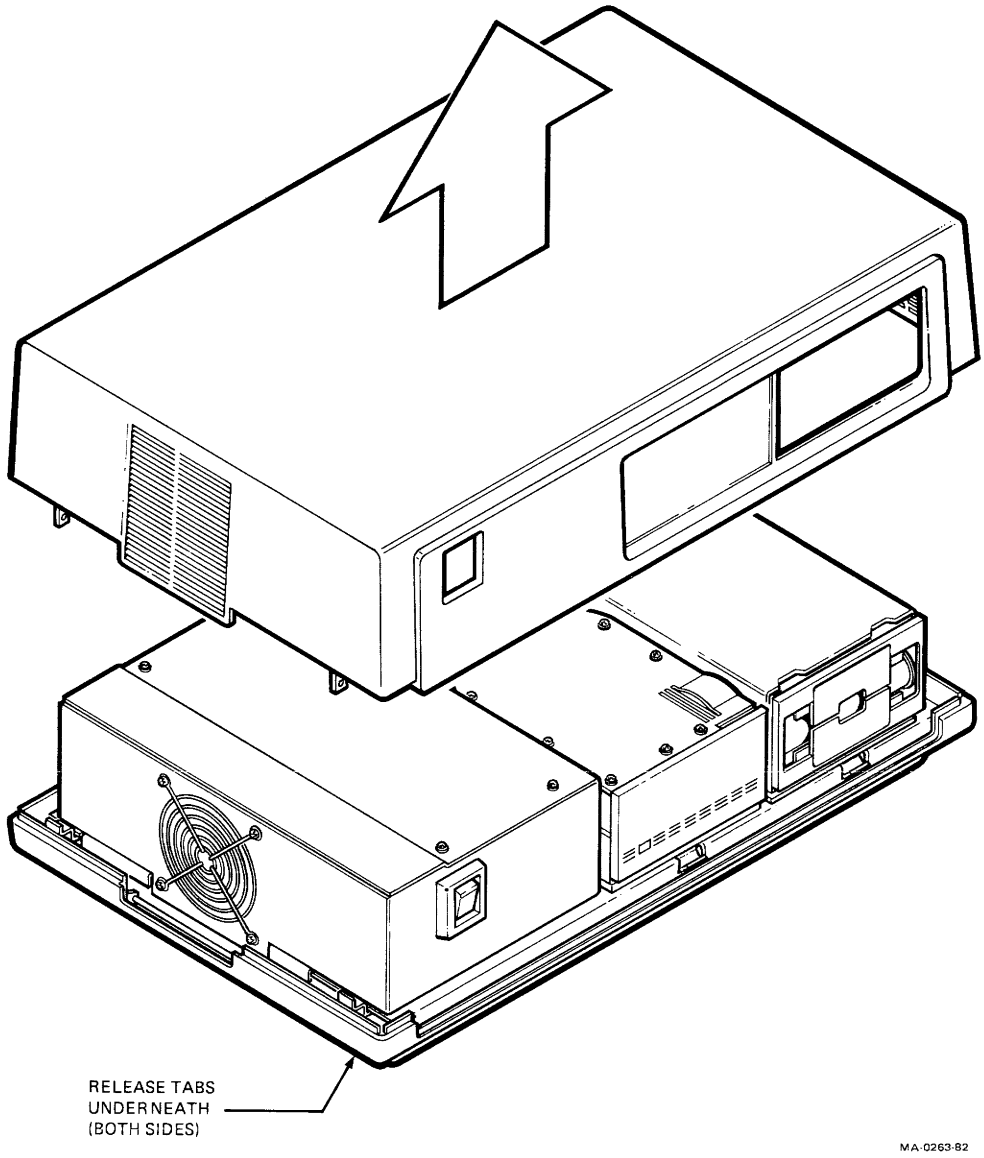


Figure 2-3 Top Cover Removal

2.3.3.2 Printed Circuit Board (PCB) Module Installation – Use the following steps to install PCB modules in the system unit card cage.

1. Remove the top cover (Section 2.3.3.1).

2. Remove the screw that secures the card cage door in place and open the card cage door (Figure 2-4).

3. Hold the module by the zero insertion force (ZIF) connector and pull the handle out by turning it 90° clockwise.

4. Slide the module into the slot in the card cage. Turn the handle straight up and push it in toward the module.

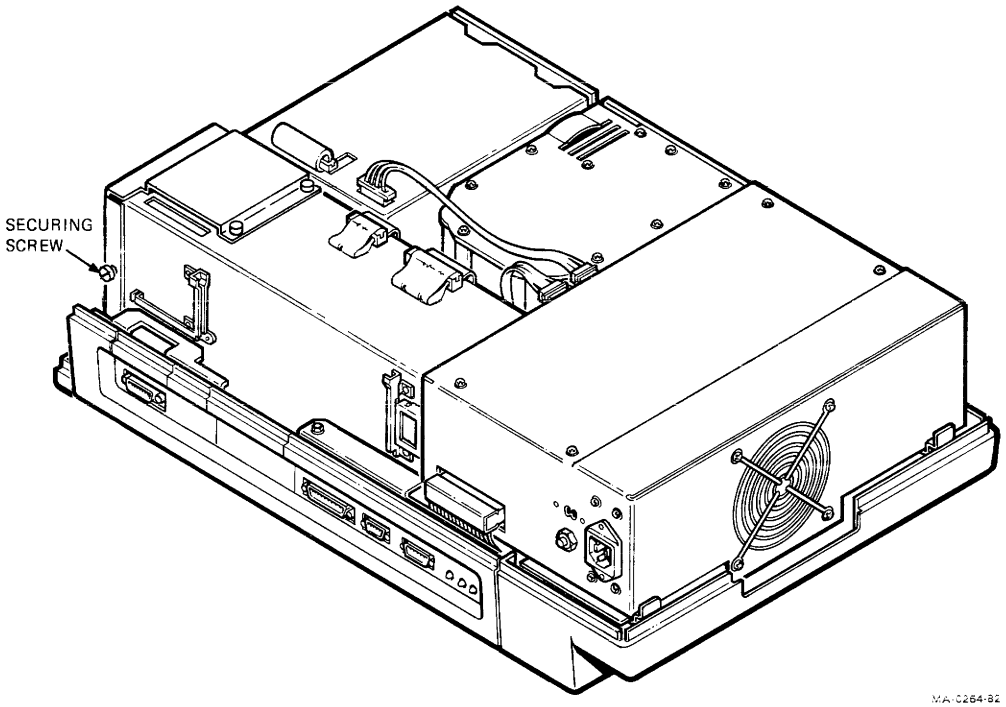


Figure 2-4 Card Cage Door Securing Screw

5. If there are any cables to be connected to the PCBs, remove the cable cover screws and then remove the cable cover.

NOTE

Install the Professional 350 extended bit map module into the slot next to the bit map video controller module. Connect the flat cable provided to the extended bit map module and the bit map video controller module as shown in Figure 2-5. Cable restrictions require that the hard disk drive controller be in slot 1.

6. Close the card cage door. Replace the cable cover if it was removed. Replace the top cover and reconnect all cables to the rear of the system unit.

7. Reconnect the system unit power cord to the nearest wall outlet after you install the last module.

2.3.3.3 RD-Series Mass Storage Device Installation – The RD-Series hard disk drive is the only mass storage device available as an option. Use the following steps to install the RD-Series mass storage device in the Professional.

1. Remove the top cover.

2. Remove the screw that secures the card cage door in place and open the card cage door (Figure 2-4).

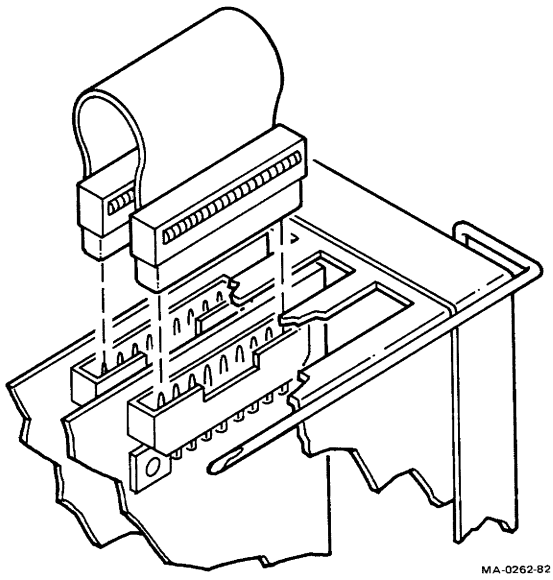


Figure 2-5 Bit Map Video Controller to Extended Bit Map Module Connector

3. Install the hard drive controller into the card cage.

NOTE
Cable restrictions require that the hard disk drive controller be in slot 1.

4. Connect the signal cables and the power cable to the RD50 hard disk drive (Figure 2-6).

5. Slide the hard drive into the system unit until it clicks into place (Figure 2-6).

CAUTION
Use extreme caution when installing the hard disk drive. Sudden physical shocks to the drive (such as dropping it onto a hard surface) will destroy it.

6. Connect the drive cables to the hard drive controller and the power supply (Figure 2-6).

7. Replace the top cover.

8. Reconnect all cables to the rear of the system unit and plug the power cord into the nearest wall outlet.

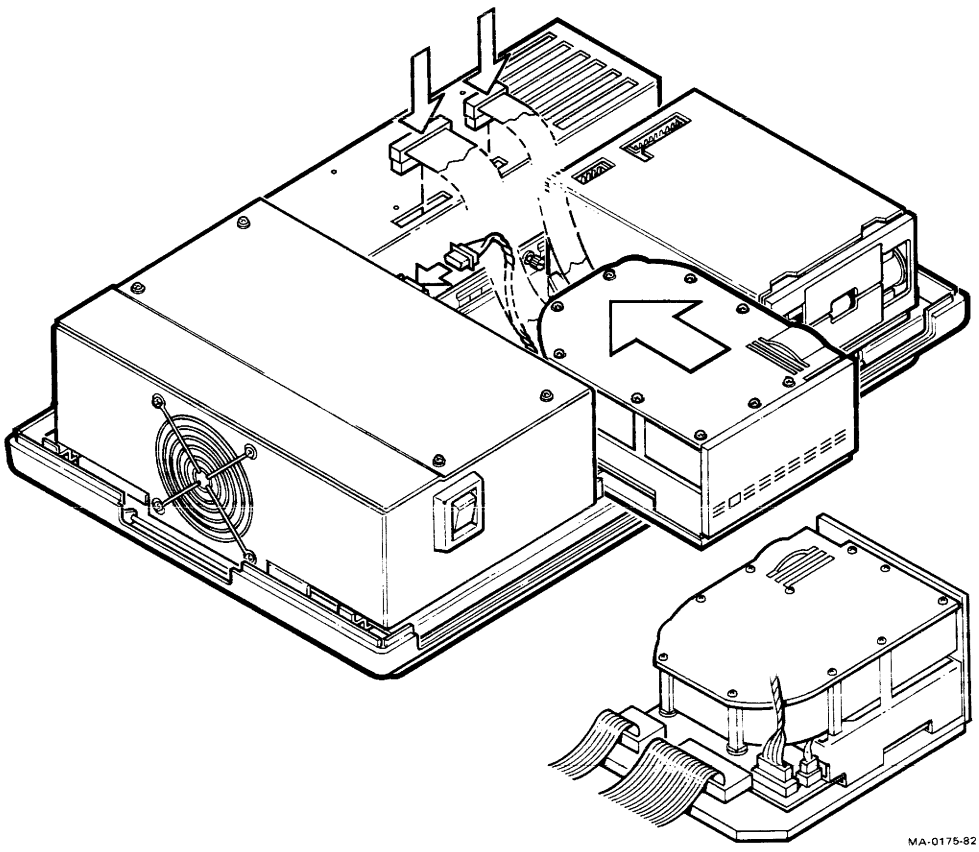


Figure 2-6 Hard Disk Drive Installation

2.4 PROFESSIONAL 300 SERIES SYSTEM UPKEEP

The following sections describe system cleaning and floppy diskette handling.

2.4.1 System Cleaning

To clean the system unit, video monitor, and keyboard covers, use a cloth dampened with a mild solution of soap and water.

To clean the monitor screen, use a cloth dampened with a mild solution of isopropyl alcohol and water.

2.4.2 Diskette Handling and Storage

Improper handling or storage of diskettes destroys recorded data and damages the read/write (R/W) heads in the RX50 dual diskette drive. Follow these instructions for diskette handling.

1. Return the diskette to its protective envelope when it is not being used.

2. Store diskettes vertically and loosely to avoid warping the jackets.

CAUTION

Never store or place the diskette near any strong magnetic fields (such as on top of a motor, on top of the system unit, or on top of the monitor). This could damage the data on the disk.

3. Use a felt tip pen to mark the diskette jacket. Do not use a pencil or ballpoint pen. They can crease the jacket and damage the media inside.

4. Insert the diskette into the drive carefully. Never force the door closed, you could crush the diskette.

5. Never remove or insert a diskette if either indicator on the RX50 drive is lit.

CAUTION

Do not open an access door if either drive is busy (drive indicator is lit). This damages the data stored on either diskette.

6. Never touch the recording surface where the jacket is cut away for the R/W heads. Fingerprints damage recorded data and the R/W heads.

7. Never store diskettes in direct sunlight or near heaters where temperatures go above 52°C (125°F). High temperatures warp the jackets.

8. Never bend or fold the diskette jacket.

CHAPTER 3
CONTROLS AND INDICATORS

3.1 INTRODUCTION
The Professional computer system has three major components: the system unit, the video monitor, and the keyboard. Each has controls and indicators that direct and monitor the system's operation.

3.2 SYSTEM UNIT CONTROLS AND INDICATORS
The following sections describe the controls and indicators for the Professional 300 system unit.

3.2.1 Controls
The system unit contains the following three controls.

1. System power switch
2. Voltage select switch
3. System circuit breaker

3.2.1.1 System Power Switch – The system power switch is on the front of the system unit (Figure 3-1). It controls the input power for the system and is labeled with the numbers 1 for on and 0 for off.

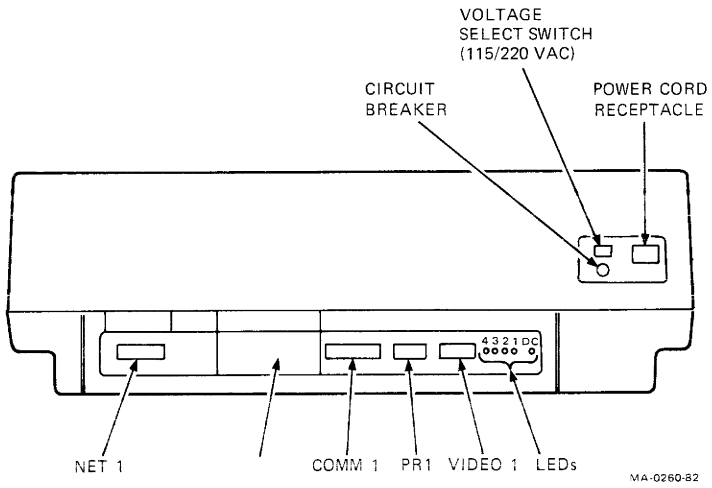


Figure 3-1 System Unit Front Panel

3.2.1.2 Voltage Selection Switch – The voltage selection switch is on the rear of the system unit (Figure 3-2). It selects either 110 Vac or 220 Vac and must be set before the system is turned on.

3.2.2 Indicators

The system unit contains two groups of indicators and one circuit breaker. The first group, on the front of the system unit (Figure 3-1), indicates whether the diskette drives are busy or inactive.

The second group, on the rear of the system unit (Figure 3-2), consists of 5 indicators, 4 red and 1 green, that indicate the status of the system unit's internal power and self-test.

3.2.2.1 Diskette Drive Busy Indicators – Two indicators on the front of the system unit indicate if the diskette drive is busy. The upper indicator lights if the upper drive is busy and the lower indicator lights if the lower drive is busy.

3.2.2.2 Indicators 1, 2, 3, and 4 – These indicators, on the rear of the system unit, monitor the system's self-test. The self-test runs whenever the system power switch is turned on. At the end of the test, all four indicators turn off and the Digital logo appears on the screen.

3.2.2.3 DC Indicator – The dc indicator monitors the power supplied to the system module. If this light is off when the power switch is on, then no dc is being applied to the system.

3.2.2.4 System Circuit Breaker – The system circuit breaker is located on the rear of the system unit (Figure 3-2). It pops out when an electrical fault occurs within the system.

3.3 VIDEO MONITOR CONTROLS

The following sections describe the controls for the VR201 video monitor.

The monitor has two controls (Figure 3-3).

1. Brightness
2. Contrast

3.3.1 Brightness – The brightness control, located on the rear of the monitor, determines the brightness of the display background.

3.3.2 Contrast – The contrast control, located on the rear of the monitor next to the brightness control, determines the brightness of the characters on the screen in comparison to the background of the screen.

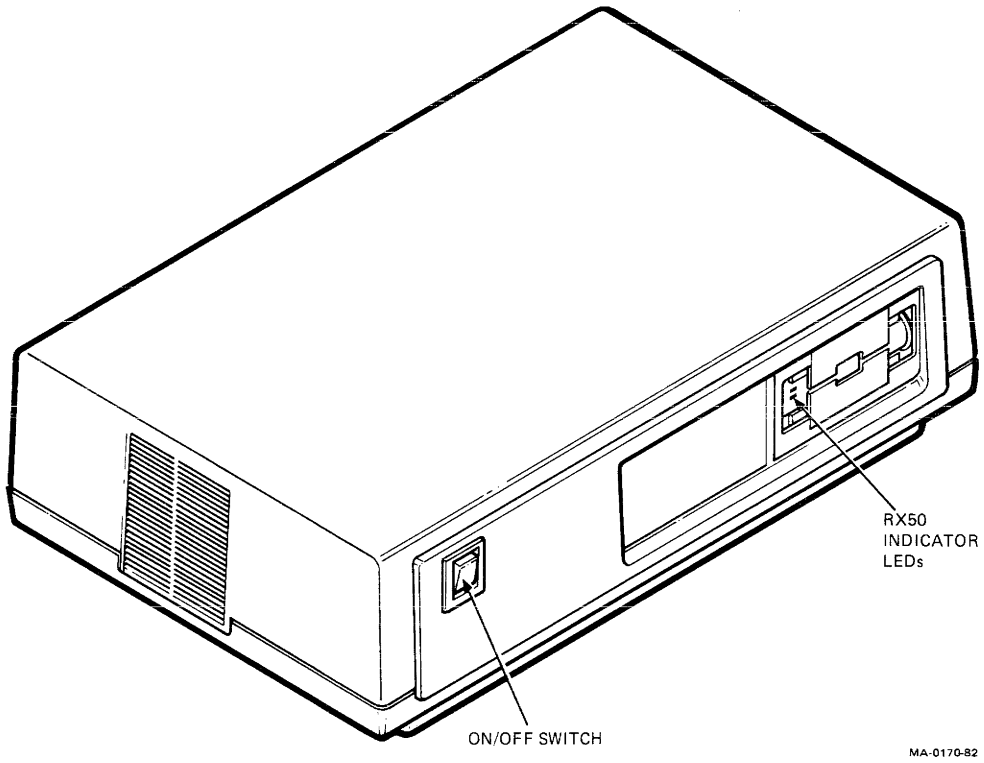


Figure 3-2 System Unit Rear Panel

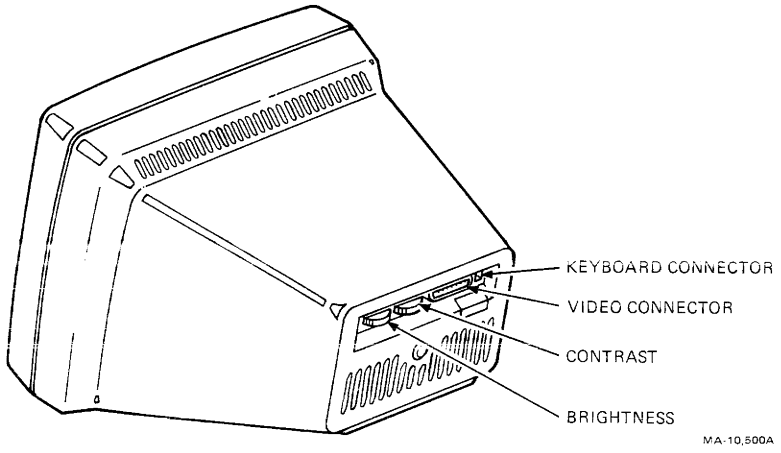


Figure 3-3 Monitor Rear Panel

3.4 KEYBOARD CONTROLS AND INDICATORS

The following sections describe the LK201 keyboard controls and indicators (Figure 3-4).

3.4.1 Controls

The LK201 keyboard contains a series of special function keys and three keypads: the main keypad, the editing keypad, and the numeric keypad. The special function keys generate electrical codes that are processed by the internal CPU and then sent to the system module.

3.4.1.1 Main Keypad – The main keypad operates like a standard typewriter keyboard.

3.4.1.2 Editing Keypad – The editing keypad is used to edit or change data that has already been entered into the system.

3.4.1.3 Numeric Keypad – The numeric keypad is used to enter numeric data. The number, minus sign, comma, and period keys generate the same characters as the corresponding keys on the main keypad.

3.4.1.4 Special Function Keys – The top row of the keyboard contains 20 keys. Two of these keys are marked **Help** and **Do.** The remaining keys are blank. These blank keys are called special function keys. The operation that each key performs changes depending on the software application.

3.4.2 Indicators

The keyboard has four indicators and two indicator sounds. The indicators are located just above the HELP and DO keys. The indicator sounds generate a signal sound when an action occurs.

3.4.2.1 HOLD SCREEN Indicator – The HOLD SCREEN indicator indicates when the system can display new data. If the indicator is off, the system can display new data. If the indicator is on, the data displayed on the screen is on hold and does not change.

3.4.2.2 LOCK Indicator – The LOCK indicator indicates when the LOCK key is pressed. If the LOCK indicator is off, all the alphabetic keys send lowercase characters. If the LOCK indicator is on, all the alphabetic keys send uppercase characters.

3.4.2.3 COMPOSE Indicator – The COMPOSE indicator indicates when the COMPOSE CHARACTER key is pressed. When it is on, the system combines the next two keys pressed and creates a special character.

3.4.2.4 WAIT Indicator – The WAIT indicator indicates when the system is performing a specific function or sequence of functions. When the WAIT indicator is on, the keyboard is inactive. The operator must wait before entering any more data or commands on the keyboard.

3.4.2.5 CLICK – The click is one of two indicator sounds. A circuit in the keyboard generates this sound when a key is pressed.

3.4.2.6 TONE – The tone is an indicator sound generated by the keyboard under software control. When the tone sounds, it indicates either something was performed wrong or a specific sequence of events is needed.

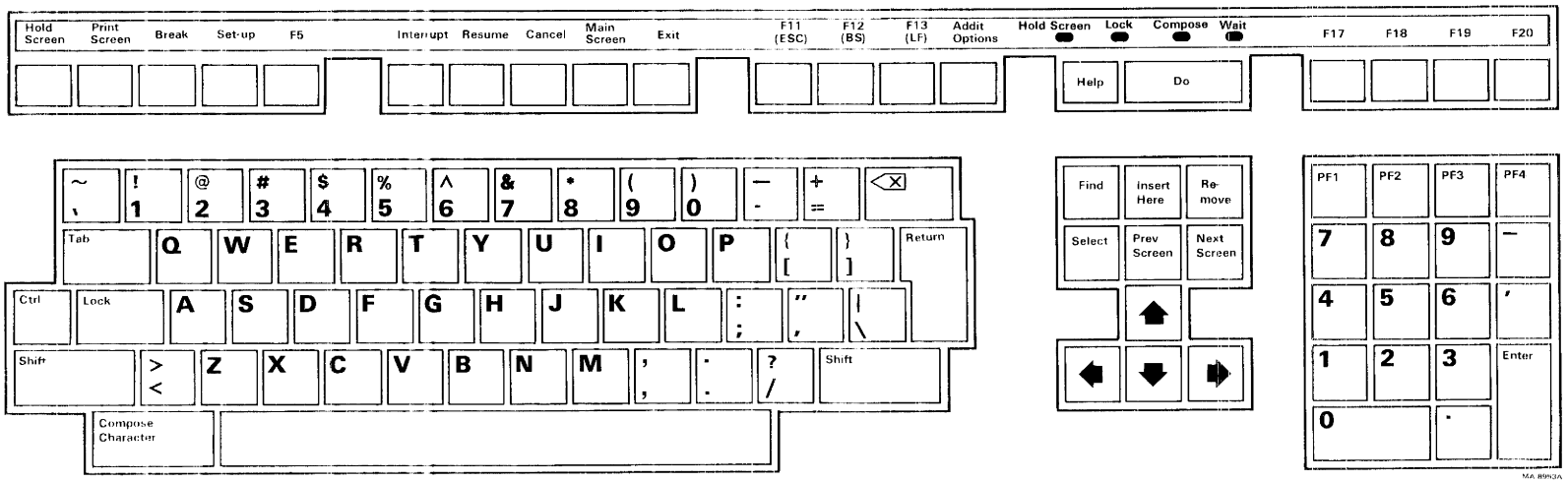


Figure 3-4 LK201 Keyboard Layout

CHAPTER 4
SYSTEM OVERVIEW

4.1 INTRODUCTION

This chapter describes the function of each component in the Professional 300 Series computer system and how they interact. Detailed descriptions for each component are provided in the following chapters.

Figures 4-1 and 4-2 are is a physical block diagrams that shows how each component fits together. Figure 4-1 shows the Professional 350. Figure 4-2 shows the Professional 380. Refer to these figures for the following discussion.

4.2 FUNCTIONAL DESCRIPTION

The following sections provide a functional description of the Professional 300 Series system components.

4.2.1 System Module

The system module is a 26.7 cm (10.5 in) × 40.6 cm (16 in) printed circuit board. It mounts on a metal plate that slides in and out of the bottom of the Professional enclosure.

The system module consists of the CPU chip set and support circuits. The F-11 is the central processing unit (CPU) for the Professional 350. The J11 is the CPU for the Professional 380. Refer to Chapter 5 for a detailed description of the F-11 chip set. Refer to Chapter 6 for a detailed description of the J11 chip set.

The following is a list of the system module electronics.

1. CPU – Professional 350 F-11 data/control chip, floating point processor and memory management unit chip set; Professional 380 J11 data/control, memory management unit and floating point unit chip set

2. 16 kilobytes of boot/diagnostic ROM

3. A video/keyboard port that supports RS170-compatible color, monochromatic signals and the keyboard interface. The keyboard interface electronics are located on the system module. The video interface electronics are located on the video controller. The Professional 350 uses a separate video module. The Professional 380 incorporates all video electronics in one gate array located on the system module.

4. A serial printer port that supports serial printers and acts as a terminal connector for maintenance purposes.

5. A modem communications port that supports asynchronous, byte-synchronous, and bit-synchronous communications.

6. A time-of-day clock with battery backup.

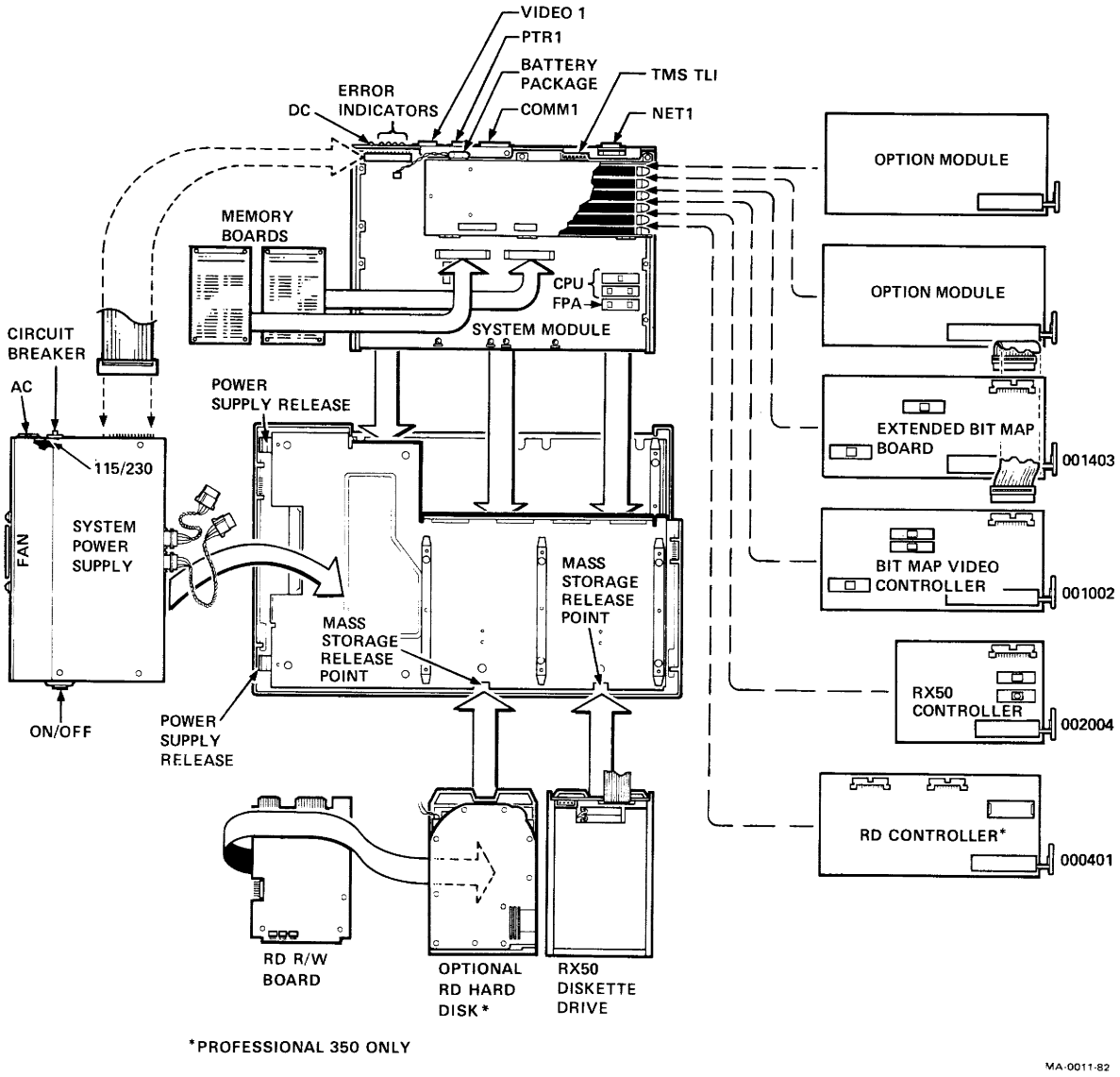


Figure 4-1 Professional 350 Physical Layout

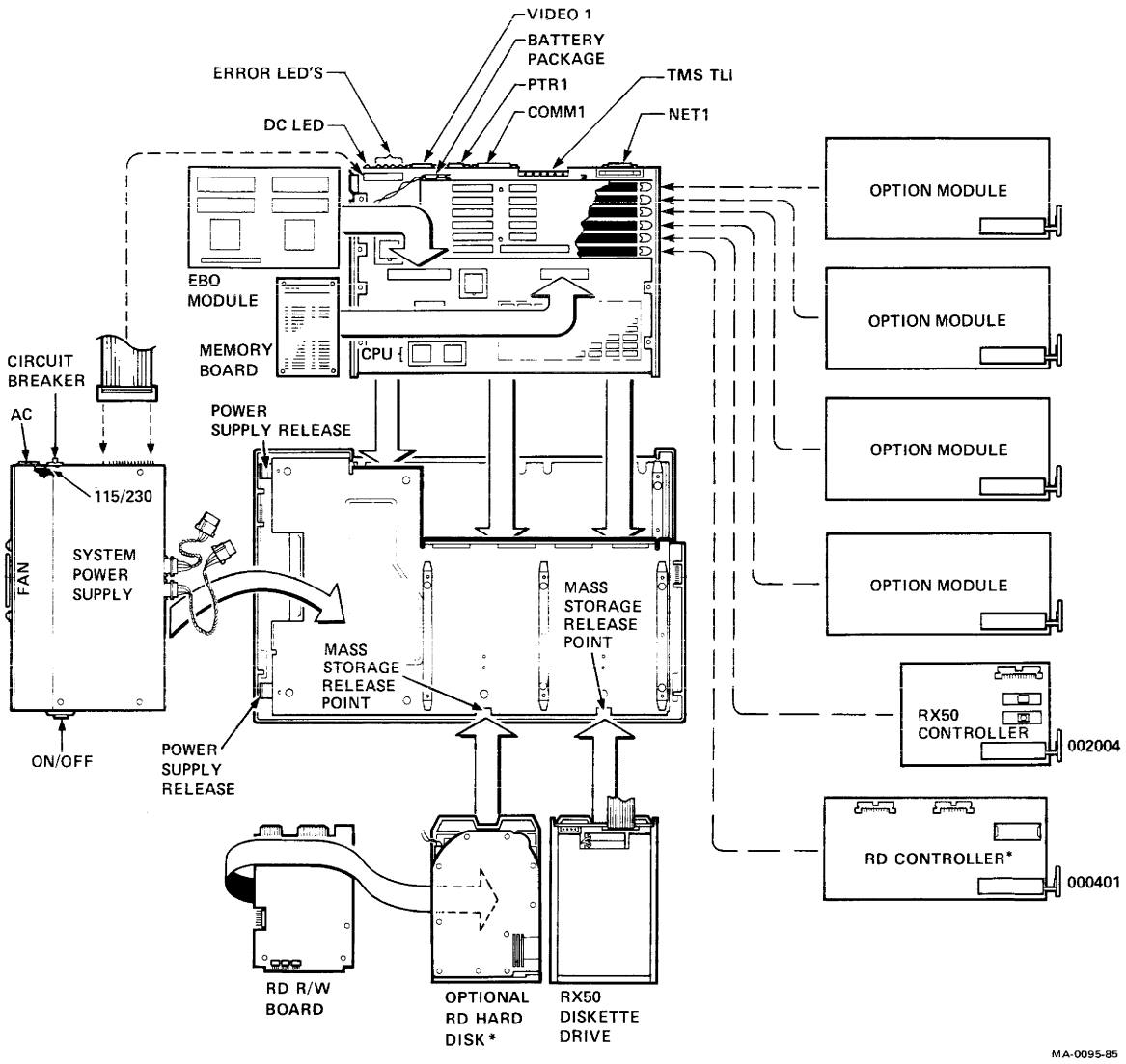


Figure 4-2 Professional 380 Physical Layout

7. The Professional 350 has two connectors that support two RAM daughter modules providing up to 1 megabyte of system memory. The Professional 380 provides up to one half a megabyte on the system module. The Professional 380 has one connector to support one RAM daughter module that provides up to a half meg of RAM for a total of 1 megabyte.

8. A six-slot card cage that supports the Computing Terminal Interconnect (CTI) Bus. These also allow access to a general purpose I/O connector and two dedicated I/O connectors.

9. A networking port.

4.2.1.1 Computing Terminal Interconnect (CTI) Bus – The CTI Bus is the interconnect path for the CPU and other option modules. It is a six-slot backplane that mounts on the system module.

Each slot in the card cage has a 90-pin "T" rail connector. All modules inserted into the card cage must use a 60- or 90-pin zero insertion force (ZIF) connector.

The first 60 pins of the bus are used for all CTI Bus signals. This portion of the CTI Bus is referred to as the general section. The last 30 pins route signals from the option modules to connectors on the rear of the system module. These pins are referred to as the private section of the CTI Bus.

4.2.1.2 System RAM Memory – The following paragraphs describe the random access memory (RAM) in the Professional 300 Series computer system.

Professional 350 – System memory consists of two memory daughter modules. Each RAM daughter module incorporates 16 64K × 1 dynamic MOS memory chips. Each daughter module provides 128 kilobytes of memory. The Professional 350 also comes standard with 256 kilobytes of RAM in an option slot in the backplane.

Professional 380 – The Professional 380 implements two groups of local RAM; module-resident RAM and a RAM daughter module that connects onto the Professional 380 system module.

- **System Module-Resident RAM** – The Professional 380 contains 512 kilobytes of system module-resident RAM. The on-board RAM consists of 64 64K × 1 dynamic RAM integrated circuit chips.

- **RAM Daughter Module Option** – The daughter module provides up to 512 kilobytes of RAM using 256K × 1 RAM integrated circuit chips. The RAM daughter module plugs into a 48-pin connector on the system module. The daughter module uses 40 pins on the connector. The remaining eight pins are for possible future memory expansion options for the Professional 380.

4.2.2 Keyboard Subsystem

The keyboard subsystem consists of the LK201 keyboard and the keyboard interface electronics. Refer to Chapter 9 for a detailed description of the LK201 keyboard.

The keyboard connects to the system module by a cable from the monitor. It is also detachable. The keyboard contains an 8051 microprocessor to process all data entered through the keyboard. The interface USART for the keyboard is on the system module.

4.2.3 Video Monitor Subsystem

The video monitor subsystem consists of the VR201 video monitor and the bit map video controller module. An extended bit map module is optional. Refer to Chapter 8 for a detailed description of the VR201 video monitor.

4.2.3.1 VR201 Video Monitor – The display screen is a 30.5 cm (12 in) diagonal monochrome monitor. The monitor housing contains the CRT, yoke assembly and the video monitor board. Two external controls adjust brightness and contrast. A cable in the rear of the system unit connects the monitor to the rest of the system. The monitor also contains a telephone-type connector for keyboard connection.

4.2.3.2 Professional 350 Bit Map Video Controller Module – The bit map video controller module is a 12.7 cm (5 in) × 30.5 cm (12 in) circuit board that plugs into one of the six slots in the CTI Bus card cage. The module contains bit map graphics with a single display memory plane of 1024 × 256 bits. The controller uses register-based control logic to help the system module access correct bit locations for screen display.

4.2.3.3 Professional 350 Extended Bit Map Option Module – The extended bit map option module (EBO) is a 12.7 cm (5 in) × 30.5 cm (12 in) circuit board that plugs into a slot next to the bit map video controller module in the CTI Bus card cage. This module adds two more bit map memory planes (1024 × 256/plane) to the monitor subsystem. When used with a monochrome system, it provides enhanced graphics and additional levels of gray scale. When used with a color system, the bit map video controller provides support for the blue scale. The red and green scales are supported by the extended bit map module.

NOTE

All video control logic for the Professional 380 is integrated onto the Professional 380 system module. Refer to Chapter 6 for a detailed description of the Professional 380 video control logic. Refer to Volume II, Chapter 4 for the Professional 380 Extended Bit Map Option Module.

4.2.4 RX50 Dual Diskette Drive Subsystem

The RX50 dual diskette drive subsystem consists of the drive controller and the drive unit. Refer to Chapter 7 of Volume II for a detailed description of the RX50 controller module and Chapter 8 for a detailed description of the RX50 dual diskette drive.

4.2.4.1 RX50 Controller Module – The RX50 controller module is a 12.7 cm (5 in) × 20.3 cm (8 in) circuit board that plugs into slot 2 of the CTI Bus card cage.

NOTE

The RX50 controller can only be inserted into slots 1 or 2 of the card cage. If the system has an RD hard disk drive subsystem, the RX50 controller can only be inserted into slot 2.

All subsystem activity is performed under program control. The RX50 controller module can perform implied seeking, reading, and writing to specified sectors and tracks on the diskette.

4.2.4.2 RX50 Dual Diskette Drive – The RX50 is a diskette drive that mounts in the system box. Each RX50 unit contains two physical drives.

NOTE

The RX50 unit is only capable of single-sided reading/writing per drive.

Each drive within a single drive unit provides 409,600 8-bit bytes (formatted) per diskette for a total of 819,200 bytes of storage. A signal cable connects the drive to the RX50 controller. A dc power cable connects the drive directly to the power supply.

4.2.5 RD Hard Disk Drive Subsystem

The RD hard disk drive subsystem consists of the controller and drive unit. In Volume II, refer to Chapter 5 for a detailed description of the RD hard disk controller and Chapter 6 for one of the RD hard disk drive.

4.2.5.1 RD Hard Disk Controller – The RD hard disk controller is a 12.7 cm (5 in) × 30.5 cm (12 in) circuit board that plugs into slot 1 of the CTI Bus card cage. The system module controls all drive activity. Data transfers to the storage media are performed in two steps.

1. The system module controls a data transfer from the main memory to the sector data buffer on the RD controller.

2. The RD controller then channels this data to the RD drive.

Two cables connect the controller to the drive: a disk data I/O cable and a control status cable. A power cable supplies power directly to the drive unit.

4.2.5.2 RD Hard Disk Drive – The RD is a 13.3 cm (5.25 in), nonremovable, sealed media, hard disk drive. Two nonremovable 5.25 inch hard disks are used as the storage media. Each disk surface uses one R/W head. The storage capacity (formatted) can be from 5 to 32 megabytes depending on which RD is in the system.

The RD hard disk drive consists of two subassemblies: the head/disk assembly (HDA) and a R/W module. The disk drive contains the storage media and supporting mechanical assemblies and cannot operate without the R/W module. The R/W module is assembled in the drive unit. Both slide into the system unit. Two connectors on the R/W module connect the drive to the RD hard disk controller. A third connector on the R/W module connects the drive to the power supply.

4.2.6 Power Supply

The power supply is a 210 watt, switch type, ac/dc voltage converter circuit. It operates at a constant frequency using pulse width modulation to regulate voltage to the system. Voltage to the supply is single-phase/three-wire and user-selectable at 115 or 230 Vac. Maximum input power required is 320 watts.

The supply mounts on the left side of the system unit. The power supply contains the system power switch, power supply circuit breaker, and voltage selection switch. It also contains circuits to protect the system against overvoltage, start-up undervoltage, and overcurrent conditions. Refer to Chapter 10 in Volume I for a detailed description of the power supply.

4.3 FUNCTIONAL DESCRIPTION OF OPERATION

The following is a functional operation description. Figure 4-3 is a functional block diagram that shows how the components interact in the Professional. Refer to this figure for the following discussion.

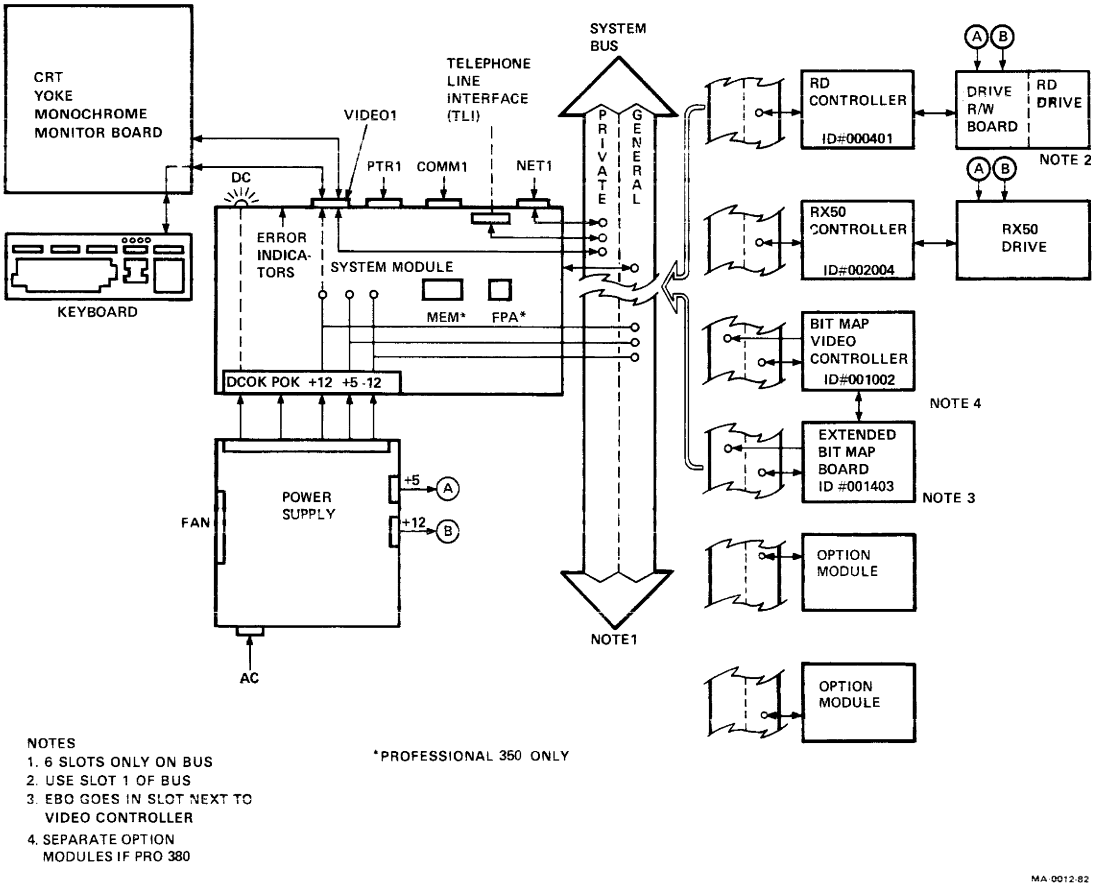


Figure 4-3 Professional 300 Series Functional Block Diagram

The operating system of the Professional can execute several simultaneous tasks. This is accomplished by using dedicated interrupts from microprocessor-based components to the CPU.

4.3.1 Initialization Sequence

At power up, the CPU accesses all available components to determine the system configuration. It then assembles an I/O map in the main memory. This corrolates each device with its appropriate handling routine.

4.3.2 Hardware Interaction Example

The following example shows how the Professional operates. Note that it may not follow the specific CPU execution cycles.

In this example, the Professional retrieves a file from the RX50, updates the video display, and prints a file to an attached printer. Each task is concurrently executed and supervised.

1. To retrieve a file, the host processor specifies the necessary address and executes a READ command to the RX50 controller. When the data is ready, the controller responds with a command completion interrupt to indicate the data is available.

2. To update the CRT display, the host processor calculates the data and address for the display. It then loads this information into the video bit map memory space.

3. To print a file, the host processor first addresses memory. It then addresses the printer USART. The USART assumes control and transfers the data, one character at a time, to the printer. As each transfer is completed, the USART interrupts the CPU and waits for the next character to be loaded.

Each task requires several host processor cycles. Dedicated interrupts received from each device inform the host processor of completed commands or device readiness. Most microprocessor-based devices for the Professional do not require sequential command and data accesses. This leaves the host processor free to select, according to its priority scheme, which device to service during each processor cycle.

CHAPTER 5
PROFESSIONAL 350
SYSTEM MODULE

5.1 INTRODUCTION

This chapter describes the Professional 350 system module, which is represented by the shaded part of Figure 5-1. The system module contains the central processor unit (CPU) and the circuits that support its operation. These circuits permit the CPU to communicate with devices mounted on the system module and on the CTI Bus or peripheral devices that are attached through the connectors on the rear panel of the system box. Figure 5-2 shows the system module.

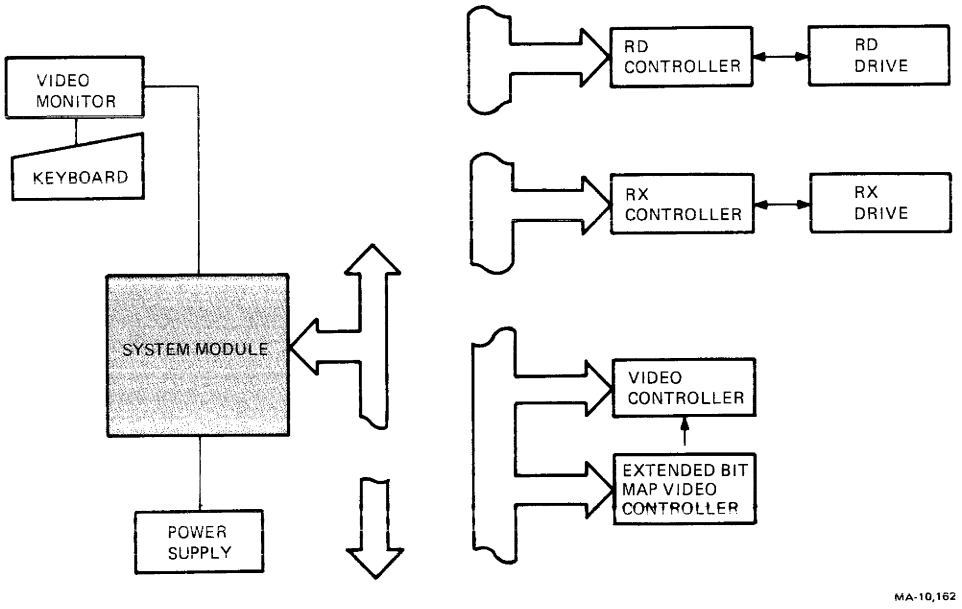


Figure 5-1 System Block Diagram

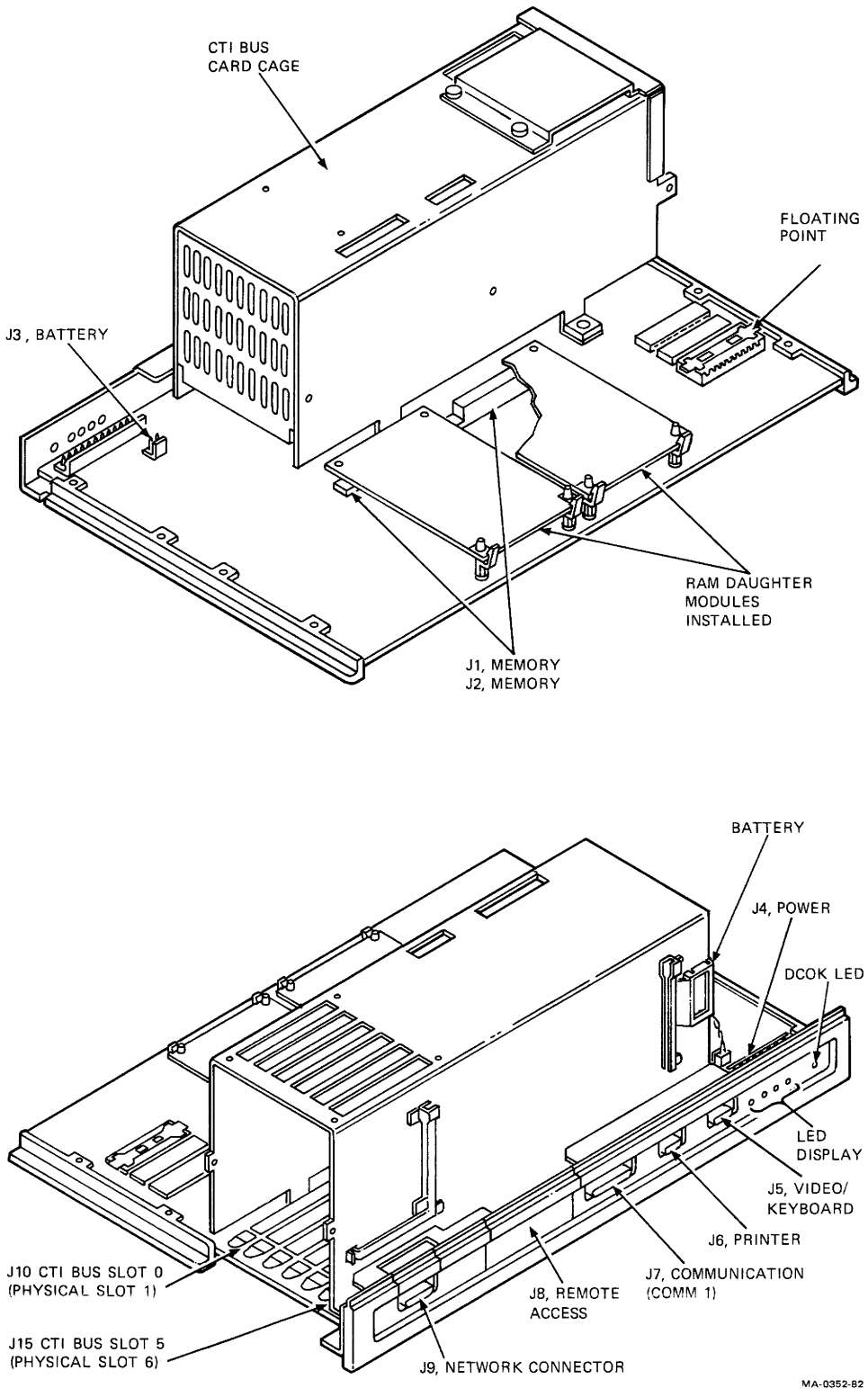


Figure 5-2 System Module

5.1.1 Chapter Organization

This chapter is divided into five sections.

1. Section 5.2 provides a general description of the functions performed by the system module.

2. Section 5.3 provides a detailed description of the circuits and components that perform the module's functions. It also provides the theory of operation.

3. Section 5.4 provides information about programming the devices that make up the system module. Programming information is given in machine language, not high level application language.

4. Section 5.5 provides the pin location for the connectors on the system module itself and the back panel of the system module box.

5. Section 5.6 provides the specifications for the unit.

Sections 5.2, 5.3, and 5.4 follow approximately the same format. The subsections follow the same sequence, so material presented in Section 5.2.6, for example, corresponds to material in Sections 5.3.6 and 5.4.6. This relationship also appears in Sections 5.2.6, 5.3.6, and 5.4.6.

5.1.2 Related Documentation

For related information, refer to the KEF11 Field Maintenance Print Set (MP-01473-00).

5.2 GENERAL DESCRIPTION

The following paragraphs describe the basic functions of the devices and circuits on the Professional 350 system module.

5.2.1 System Module General Description

The CPU/memory module provides the basic central processor unit (CPU) functions (F-11 CPU chip set, memory management unit and floating point) for the computer and also supplies the I/O module expansion backplane for up to six options. All input and output connectors (printer, keyboard, communications, network, and remote access lines) reside on this module. This module supports the Computer Terminal Interconnect (CTI) Bus structure.

The system module supports random access memory (RAM) on plug-in printed circuit modules (daughterboards). Each daughterboard is standard with 128 kilobytes of RAM and can be upgraded to 512 kilobytes. Up to two daughterboards can be used. These modules are not connected through the option area. A Professional 350 also has one memory board standard which is connected through the option area. It contains 256 kilobytes of RAM.

The system module has a 22-bit address space to access up to four megabytes, although this system's memory range has been limited to three megabytes. The top eight kilobytes are reserved as the I/O page.

All interrupts for devices on the system module and devices on option modules are handled by controllers on the system module. The system module supports DMA activity to the RAM memory and arbitrates all the DMA requests.

5.2.1.1 Subsystem Characteristics – The CPU/memory board provides the following functions.

PDP-11/23 instruction set
16-bit word or 8-bit byte addressing
Eight internal registers
Stack processing
Programmable vectored interrupts
Direct memory access (DMA)
16-bit ODT console emulator
Support for one megabyte of RAM (on system module daughterboards)
22-bit addressing (three megabyte addressing capability)
Kernel and user modes only (no supervisor mode)
Floating point instruction set
Power-up self-test and bootstrap (ROM based)
Indicator (LED) display
Battery backed-up time and date clock
Battery backed-up RAM (50 bytes)
Printer/console interface
Video/keyboard interface
Communications interface
Full modem controls
ID PROM
6-slot CTI backplane

5.2.2 Physical Description

The system module is 26.0 × 40.0 cm (10.4 × 16 inches) and has the CPU and support circuits on it. The CTI Bus is located in an aluminum card cage that has six bus slots inside. A hinged door covers the opening. Access slots for option modules are on top. The rear panel has most of the connectors on it and forms the rear of the system module.

5.2.3 System Module Features

The system module consists of a CPU which, under software control, can perform several tasks concurrently. This is called interlacing operations. Since a single operation may require more than one processor cycle, the CPU can perform another task while completing the first. When the first is done, an interrupt informs the CPU. The CPU can then find the status of that operation, begin its next step, and repeat the process for the second step.

The CPU directs, controls, and monitors operations on the system module. Interrupts, printer, keyboard, and communications interfaces are programmable. These devices perform their own functions and through interrupts, permit interlacing operations to take place in a foreground and background mode.

5.2.3.1 Central Processor – The central processor consists of a 2-die 40-pin hybrid integrated circuit. The data chip contains the PDP-11 general registers, the processor status word (PSW), working registers, the arithmetic logic unit (ALU) and conditional branching logic. It performs arithmetic and logical functions, handles all data and address (except relocation) transfers with the external bus, and operates most of the signals used for interchip communication and external system control.

The control chip contains microprogram (internally programmed sequences) logic and local microprogram storage in programmable logic array (PLA) and ROM arrays. This chip accesses the appropriate microinstruction in PLA or ROM, sends it along the microinstruction bus (MIB) to other control and MMU chips, and generates the next microinstruction (microprogram instruction) address. The control chip accesses only its local storage but additional control chips (NOT available from Digital) can be added externally to provide additional microprogram storage.

5.2.3.2 Memory Management – The memory management unit provides 22-bit memory addressing capability of up to four megabytes. It also allows memory protection in a multi-tasking operating system environment. The maximum allowable system memory is three megabytes.

The memory management function is implemented in one 40-pin package. The floating point registers are located in the MMU chip.

5.2.3.3 Floating Point Adapter (FPA) – The floating point instruction set (FP11) is included. Both single and double precision floating point capability are available. Other features available include floating-to-integer and integer-to-floating conversion.

The FP11 microprogram resides in two MOS/LSI chips contained in one 40-pin package the FPA. The FPA requires both the MMU chip and the base MOS/LSI chips because all the floating point accumulators and status registers reside in the MMU.

5.2.3.4 Power-Up Self-Tests – The power-up self-tests in ROM verify system configuration and available memory space. The self-test is executed at every system power up. Verification is the identification of devices and their conditions.

Self-tests include the following three parts.

1. System
2. Base options
3. Add-on options

After these three parts are finished, the system executes a bootstrap loading routine.

The system core self-test verifies the CPU, all available memory space, the self-test ROM, and the full addressing range of the MMU chip. The power-up self-test does not continue testing if the system core self-test is not successful.

The base option part of the self-test continues after successful completion of the system core self-test. This part tests all options available on the system module. The options include the communications port, system clock, FPA, the printer port, battery check, battery backed up RAM check, and video/keyboard port.

The final part of the self-test is the add-on options self-test. This test is performed on all options connected to the CTI Bus. The self-test is loaded from a ROM located on each option module. This does not include the RD hard disk drive subsystem, the RX50 dual diskette drive subsystem, and the video subsystem. The system's ROMs contain the diagnostics for these components. All other option modules contain their own self-test diagnostics. All option modules have an option identification number. This number allows the system self-test to determine which devices are installed in the system and to store this information in a configuration table for use by the operating system.

The primary indicator of an error during self-test is a picture of the system displayed on the monitor with the failing option highlighted. Also displayed are an error code and the identification number (ID) of the error type. The secondary error indicator is the four indicators (LED) display on the rear of the system box which can be used if the monitor display is either not attached or not working.

5.2.3.5 Boot Sequence – If the power-up self-tests are completed without error, the system enters a bootstrap routine and the Digital logo appears on the monitor. This causes a search to first determine the boot device and then to load the boot program.

The following is the three phase boot sequence.

1. Primary Boot Sequence – At the end of the power-up self-test, the diagnostic boot ROM determines if there are any removable media devices on the system. If there are, each device is read and tested for a bootable volume. If there are no removable media devices on the system or there is no bootable volume loaded, the secondary boot sequence is executed.

2. Secondary Boot Sequence – The second phase consists of reading the battery backed up RAM for customer-selected boot devices. The first selectable device boot routine in battery backed up RAM is loaded and executed. If this boot fails, the diagnostic boot ROM selects the next device. Once all devices in the battery backed up RAM have been tried without success, the tertiary boot sequence is started.

3. Tertiary Boot Sequence – The third step uses the boot priorities predetermined by the ID number of the devices. The diagnostic boot ROM starts with the highest priority, loads the appropriate boot program, and starts execution. If the boot fails, the next device in the priority chain is selected and an error is displayed on the monitor, indicating the boot process failed. The display is a picture of a diskette with a question mark.

NOTE

If the bootstrap error is displayed, the self-test ROM loops back to the primary boot sequence and stays in this loop until a valid boot is executed or power is reduced.

5.2.4 CTI Bus Option Connectors

The CTI Bus backplane is part of the system module. The backplane accepts option modules using a zero insertion force (ZIF) connector. There are six option module slots.

Each option slot has a 90-pin connector on the system module. The first 60 pins (referred to as the general section of the bus) are used for the CTI Bus signals. The last 30 pins, 61 through 90 (referred to as the private section of the bus), are used to route signals from the option modules to connectors on the rear of the system module. An option module that only requires the CTI Bus signals can use a 60-pin ZIF connector. An option module that requires using the rear connectors on the system module must use a 90-pin ZIF connector.

All signals, except six, are bused through all six slots. The six non-bussed signals provide slot dependent signals to the system module for handling address decoding, interrupts, and DMA.

5.2.5 System Registers

The system module contains registers that store information about the overall system status. The CPU reads these regularly and performs the appropriate service routine whenever a status change occurs.

5.2.5.1 Indicator (LED) Register and Display – This register is the only one visible to the user. It shows the system status after the power-up self-test (Section 5.2.3.4).

There are five LEDs on the rear of the system module, one green and four red. The green one turns on when the DCOK signal from the power supply is asserted. This indicates all dc power is within tolerance. The four red LEDs indicate errors found during the power-up self-test. At power up, all four red LEDs turn on then turn off if no errors are found. If the LEDs remain on, it indicates a system module error. The decoded indicator error codes are found in Table 5-6.

5.2.6 Interrupts

The system module uses three interrupt controller chips to handle all the system interrupts.

1. The first controller handles all the interrupts generated by devices on the system module.
2. The second controller handles all the A interrupts from the option modules.
3. The third controller handles all the B interrupts from the option modules.

The interrupt controllers do the following.

1. Latch the interrupt requests
2. Provide the interrupt enable for each
3. Prioritize the pending interrupts
4. Generate the proper vectors

The controllers interrupt the CPU at processor status level 4.

5.2.7 ROM Memory

The system module also contains 16 kilobytes of ROM. It contains the power-up self-test code, configuration and initialization code, and the boot code. Some of the ROM is in the I/O page and some is in the memory address space.

Address	Size	Location
17730000–17757776	12 KB	memory space
17760000–17767776	4 KB	I/O page

Any attempt to write to the ROM locations results in a nonexistent memory trap to location 4.

5.2.7.1 ID PROM – Each system module board contains a PROM with a unique 32-byte ID. The ID PROM contains information to verify the system module integrity.

5.2.8 RAM Memory

The system module contains support circuitry for two memory daughter modules. There are two 40-pin connector banks on the system module that accept the memory modules. The memory option modules provide up to 512 kilobytes of RAM per module with 16 256K × 1 dynamic RAM chips. The system module can address up to 512 kilobytes at each RAM daughter module bank.

The Professional 350 comes standard with 512 kilobytes of RAM. This is distributed as follows: two 128 kilobyte daughter modules and one 256 kilobyte option module (uses one slot). The daughter modules may each be upgraded to 512 kilobytes of RAM.

5.2.9 Video/Keyboard Port

The system module provides a serial keyboard port as part of the video/keyboard port. Video signals for black and white and color CRT monitors use other pins in the same port.

The video controller, mounted on the CTI Bus, generates the video signals. Refer to Chapter 7 for information about the bit map video controller module.

The keyboard uses a 2661 USART and performs asynchronous serial communications at programmable baud rates up to 19.2 kilobaud. The port uses EIA RS-423 signal levels. Connection is made on the rear of the unit via a 15-pin male D-subminiature connector, J5. Section 5.5 shows the pinning and position of J5 on the system module.

The keyboard part of the port communicates with the computer's keyboard. However, it is a general serial port that can be used to communicate with any serial device. The mode of operation is programmable (Section 5.4). When using the port with the computer's keyboard, the mode must be set to the following conditions.

1. 8-bit character length
2. No parity
3. One stop bit
4. 4800 baud clock rate

5.2.10 Printer Port

The system module provides a serial printer port. It can perform asynchronous serial communications at programmable baud rates up to 19.2 kilobaud. The port uses EIA RS-423 signal levels. Connection is made on the rear of the unit via a 9-pin male D-subminiature connector, J6.

5.2.10.1 Console Serial Line Port – The console DL is included as a maintenance feature. Physically, it is the same port as the printer port. The printer port can be made to simulate a standard console interface. When a terminal is connected to the port instead of a printer, the address decoder recognizes the console addresses 17777560–17777566. In this mode, the port programs like a DL serial device with a receiver CSR, a receiver data buffer, a transmitter CSR, and a transmitter data buffer. Accesses to these registers when a terminal is not connected to the port result in reads of all 0s and writes with no effect. All the printer port registers, 17773400–17773406, are always accessible.

Interrupts are not handled like a standard console DL. There are no interrupt enable bits in the CSR registers at locations 17777560 and 17777564. Interrupts must be enabled/disabled and handled through interrupt controller 0 like the printer port interrupts. The vectors can be changed from the printer port vectors of 220 and 224 to the console vectors of 60 and 64 by reprogramming the response memory in interrupt controller 0 (refer to Sections 5.2.6, 5.3.6, and 5.4.6 for details).

Hardware break detection can be enabled when a terminal is connected to the port. This allows the processor to halt into micro-ODT (Octal Debugging Technique) when the break key is depressed on the terminal. The hardware break detection has no effect if a printer is connected to the port.

When pins 8 and 9 of the printer port connector J6 are connected together, the hardware determines that a terminal is connected to the port. When using the port for a printer, a printer port cable (PN BCC05) should be used (the cable does not short pins 8 and 9). When using the port as a console, a terminal port cable (PN BCC08) should be used (the cable shorts pins 8 and 9).

5.2.11 Communication Port

The system module has a communication port that can operate in asynchronous and bit or byte synchronous protocols. In asynchronous mode, it runs at split programmable baud rates up to 19.2 kilobaud. In synchronous mode, it runs up to 740 kilobaud. The transmitter is double buffered and the receiver is quad buffered. A full set of modem controls is also present. All the port signals are EIA RS-423 levels. Connection is made on the rear of the unit via a 25-pin male D-subminiature connector, J7.

There are two interrupts associated with the communications port. The first interrupts the CPU if the 7201 USART chip requires service, receiver or transmitter. The second interrupt can indicate that a state change has occurred on one of four modem control signals. These four modem control signals are Ring Indicator, Data Set Ready, Clear To Send, and Carrier Detect.

5.2.12 Battery Backed-Up System Clock and RAM

The battery backed-up system clock and RAM keeps track of time and date. It stores 50 bytes of data even when the system is turned off. The clock is an MC146818 CMOS chip. Backup is achieved by using a rechargeable nickel cadmium (NiCD) battery. The battery power is supplied to the system module via connector J3.

The clock accuracy is better than one minute per month.

The battery continuously charges when the system is powered on. When the power is shut off, the battery supplies power to the clock which continues to update the time and date. A completely charged battery maintains clock operation for a minimum of 10 days while the system is turned off. The battery is completely charged after 48 hours of continuous system power on time.

The system clock and RAM contain a bit which indicates if the clock power goes too low and that the time and date may be invalid. The bit, called a valid RAM and time (VRT) bit, is located in the CSR3 register. See Section 5.4.13.1 for details of the VRT bit.

The chip can also be programmed to interrupt the CPU at a specified alarm time or at a periodic rate. The periodic rate can be programmed to one of 13 frequencies ranging from 2 Hz to 8.192 kHz. There is no line time clock.

5.3 DETAILED DESCRIPTION

This section provides functional and detailed descriptions of the functions performed by the microprocessor and support circuits of the KDF11-CA system module. It describes the system logic used for making decisions. It only describes computer operations, electronic processes, or complicated timing sequences when necessary.

To understand the central processor's functions refer to the following books.

Microcomputers and Memories (EB-20912-20)
Microcomputer Processor Handbook (EB-15836-18/79)
KDF11 Field Maintenance Print Set (MP-01473-00)

All illustrations in this section are functional block diagrams. Logic symbols indicate function and may not represent actual circuitry. Figure 5-3 shows this section's map and module block diagram. For quick reference, each block on the diagram has a number or numbers by it. These numbers refer to the subsection(s) in this section that describe the block.

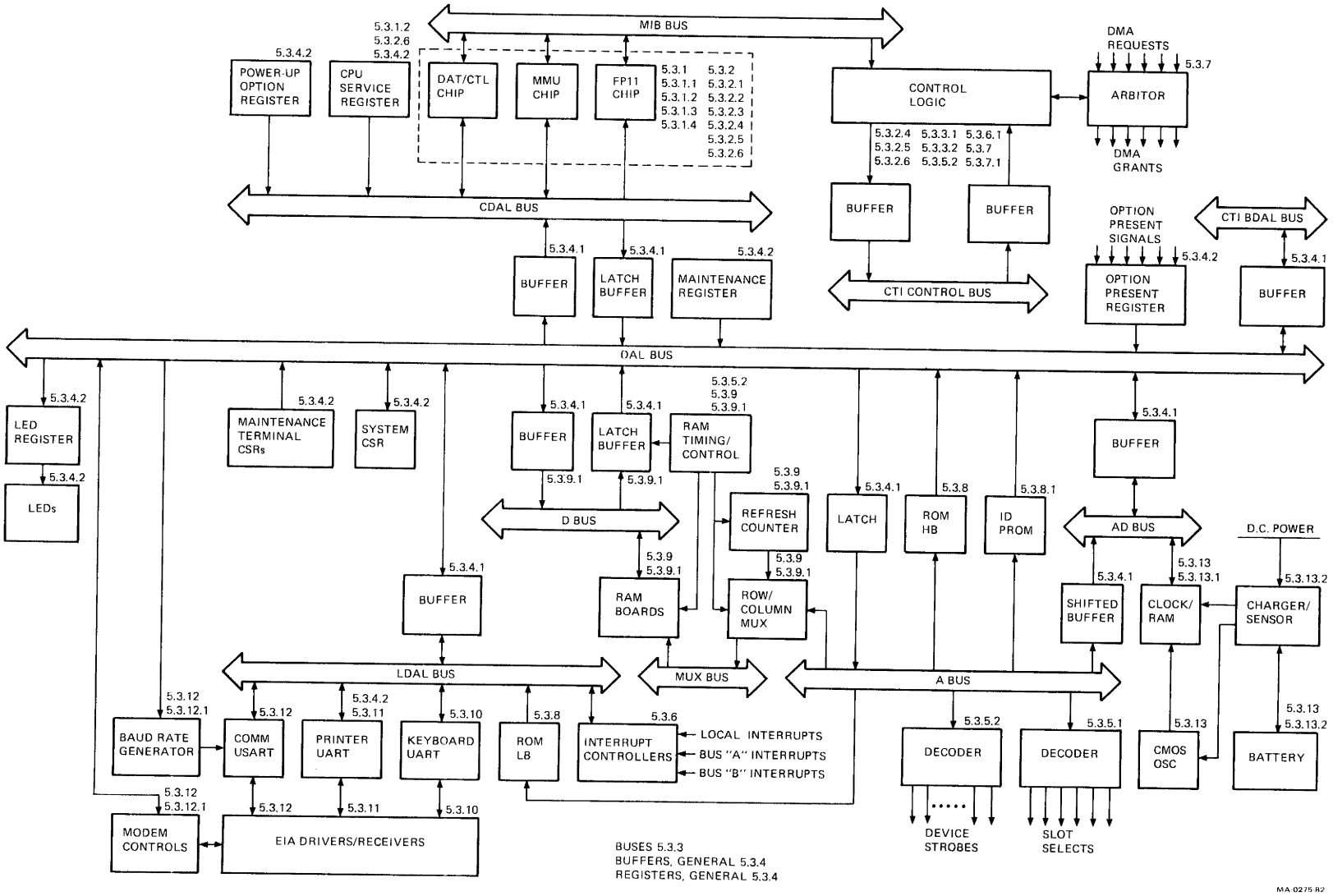


Figure 5-3 Section 5.3 Map

5.3.1 Microprocessor Overview

The Professional 350 CPU chip set has five integrated circuit chips: the data chip, the control chip, the memory management unit (MMU) chip and two floating point (FP) chips. The chip set is a 16-bit LSI microprocessor with PDP-11/23 capabilities. It also implements a subset of PDP-11/70 memory management. The chip set also executes floating point arithmetic instructions.

The chips are installed on 40-pin ceramic dual in-line packages (DIP). The basic configuration is a hybrid combination of a data chip and a base control chip on a single DIP, the central processor chip. The memory management unit (MMU) is mounted by itself on a DIP. The floating point chips are mounted on another DIP.

The data chip contains PDP-11 registers, scratchpad registers, and the arithmetic logic unit (ALU). The control chip contains (in internal memory) instructions to supervise CPU operations. These instructions, called microinstructions, emulate the instructions performed in full size PDP-11 processors. The CPU's logic that tells it how to use microinstructions is called the microprogram. The PDP-11 instructions are called here macroinstructions. The Professional's CPU performs microinstructions which emulate PDP-11 macroinstructions. Several microcycles (periods to perform microinstructions) may be required for each macrocycle (period to complete a macroinstruction).

The memory management chip contains the necessary registers and relocation logic to implement 18- and 22-bit addressing. It also contains the floating point register file.

1. Data chip
   The data chip contains PDP-11 registers, scratchpad registers, the processor status word (PS), the arithmetic logic unit (ALU), and the conditional branching logic (i.e., microinstructions). This chip performs all arithmetic and logic functions, handles data and address transfers with the rest of the system (except relocated addresses), and coordinates most interchip communication.

2. Control chip
   The control chip contains the microprogram logic and the required storage areas to supervise CPU operations. The control chip implements microinstruction sets, emulating the basic PDP-11 instruction set. These instruction sets include the extended instruction set (EIS) and provides console debugging capabilities.

3. Memory management unit (MMU) chip
   The memory management unit (MMU) performs two activities. It provides the memory management and contains the necessary registers for floating point execution.

   As a memory management unit, the chip provides dual mode capability (user instruction space – normal operation) and kernel (CPU instruction space – internal operation) for relocation of a 16-bit virtual address to an 18-or-22 bit physical address. The MMU chip contains the error detection logic to provide memory protection features such as R/W access control and page length limits. In addition, all necessary memory management data registers are in this chip.

   As an aid to floating precision, the MMU chip provides the 36 16-bit registers needed for operand storage, status information storage, and scratchpad areas during floating point operations.

4. Floating Point Adapter (FPA)
   The floating point adapter (FP11) provides 46 additional instructions to the integer arithmetic instructions in the basic instruction set. This executes floating point operations 5 to 10 times faster than equivalent software routines and provides for both single precision (32-bit) and double precision (64-bit) operands. This is equivalent to 7 and 17 decimal digit accuracy, respectively. This also conserves memory space since the FP11's internal logic executes floating point routines instead of programmed routines. FP11 operation requires the MMU for operation because the MMU contains eight 64-bit floating point registers.

5.3.1.1 Chip System Architecture – These are three categories of signals used for communicating between the chips and with external logic: Microinstruction Bus (MIB), Data Address Lines Bus (DAL), and discrete signals (Figure 5-4).

The MIB is time-multiplexed. During clock-low time, a new microinstruction travels along the MIB from the active control chip to the data chip and all other control chips. During the next clock-high time, the data chip generates control information based on this microinstruction and transmits control information on the MIB.

The CDAL bus is a bidirectional connection between the logic circuits. It is time-multiplexed and has two independent definitions during the clock cycle. During the first half of a cycle, clock-high time, the chips use the CDALs to transfer data in or out. This data is a PDP-11 macroinstruction, a 16-bit physical or virtual address, or some form of numerical data. During the last half of a cycle, clock-low time, a relocated address or service information can be transferred on the CDALs. The relocated address is the 18 or 22-bit translation of the 16-bit virtual address driven by the data chip during the preceding clock-high time. The MMU chip must be installed (normal operation in the Professional 350) for 22-bit addressing. Synchronous and asynchronous status information, service, also use the CDAL bus. Service information consists of interrupt requests, error conditions, power conditions and the halt line. This information is latched in the control chip where it directs microprogram flow.

The discrete signals are dedicated lines each with specific meanings; they are not time-multiplexed. These signals are discussed later.

Table 5-1 summarizes the buses just presented.

5.3.1.2 Data/Base Control Chip Interaction – The data chip/base control chip combination is a multichip PDP-11 microprocessor with expandable internal storage for microprogram processing. The data chip/control chip relationship is that of arithmetic logic unit (ALU) and sequencer; the data chip is an ALU and controller, the control chip directs the microprogram sequence and storage. The following sequence provides an overview of their operation. This sequence considers just the base control chip. However, all control chips interact with the data chip in the same manner. They differ only in what macro-level information they can decode.

1. Fetch macroinstruction: both the data and control chips receive and latch a macroinstruction.

2. Execute macroinstruction: the control chip transmits a specific sequence of microinstructions to emulate the latched macroinstruction. Simultaneously, the data chip receives the microinstructions and performs the appropriate arithmetic, logic, and control functions.

3. Load service information: the control chip latches service information. If service is pending (Section 5.3.2.6), the chip set goes to step 4. If no service is pending, the chip set goes to step 1.

4. Execute service routine: the control chip transmits a specific sequence of microinstructions to execute the required service routine. Simultaneously, the data chip receives the microinstructions and performs the appropriate arithmetic, logic, and control functions.

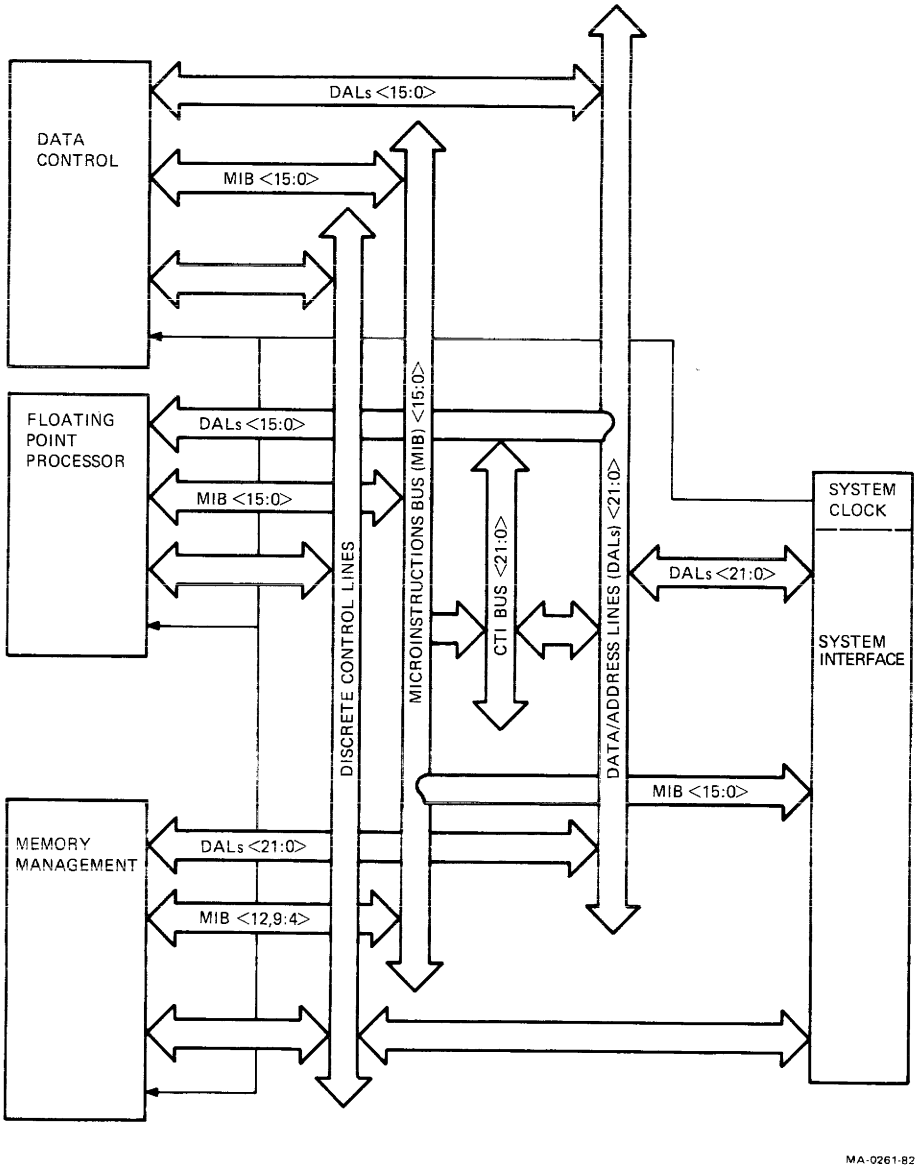


Figure 5-4 CPU Chip Set Communication

Table 5-1 Functional Summary of CPU Communication Buses

	Clock High Time	Clock Low Time
CDALs:	a macroinstruction, a 16-bit physical or virtual address, or numerical data	A relocated address, or service data
MIB:	control information	A microinstruction

To help clarify the preceding process, the following provides a detailed emulation of the CLR R0 macroinstruction.

Clk*	Data Chip	Control Chip
	PART I: MACROINSTRUCTION FETCH	
Low		Transmit ADR2 PC microinstruction on the MIB, (this instruction causes the value in the PC to address memory and increments the PC by 2.
↑	Latch ADR2 PC microinstruction from the MIB	
High	Execute address ADR2; put PC on the DALs, increment PC by 2, output discrete control signals	
↓		Latch control information from the MIB
Low		Transmit instruction input microinstruction on the MIB
↑	Latch instruction input microinstruction from the MIB	
High	Execute the microinstruction just brought in; input the CLR R0 macroinstruction from the DALs and output discrete control signals	
↓	Latch macroinstruction from the DALs	Latch macroinstruction from the DALs and control information from the MIB

* The terms in this column define the state of the clock line: low = clock voltage at a low, high = clock voltage at a high, ↑ = a rising edge, ↓ = a falling edge.

Low		Transmit CLR microinstruction on the MIB
↑	Latch CLR microinstruction from the MIB	
High	Execute CLR microinstructions; clear the register which is specified in the latched macroinstruction and transmit discrete control signals	
↓		Latch the control information from the MIB

The chip set now goes to service. On the next rising edge, the macro-level service data is clocked into the control chip from the CDALs. If no service is requested, the machine falls through to the macroinstruction fetch sequence. If service is requested, the appropriate service routine begins.

If the CPU cycle is not an address relocation, CDAL address bits 16–21 are pulled low.

5.3.1.3 Memory Management Interaction – When the MMU is used for memory management, it supplies the resources for 18 and 22-bit addressing. When added to the data chip/control chip system, it creates an additional communication situation. This occurs when an address needs to be relocated. The following sequence shows the address relocation.

Relocation Address Interchip Communication

Clk	**Data Chip**	**MMU Chip**
High (during execution of an address micro-instruction)	Outputs the address on the CDALs and BSIO (a discrete control signal), outputs the the proper AIO codes (specific combinations of MIB lines) on the MIB.	Detects an address cycle by looking at the AIO codes, asserts a specific MIB line to indicate a relocated address cycle and inputs the address from the CDALs and BSIO.
↓	Latches the MIB line data for MMU chip; this tells the data chip that the MMU is relocating an address.	

Relocation Address Interchip Communication (Cont)

Clk	Data Chip	MMU Chip
low		Generates the relocated address and transmits it on the CDALs and BSIO.
↑	Latches the relocated address from the CDALs and BSIO to check for reference to the PSW.	Latches the internally relocated address to check for reference to any of the processor's registers.

If memory management is disabled, address cycles (a macrocycle) proceed as all other microcycles. If enabled, it adds three changes to the address cycles of the basic chip interaction. First, it changes when the address on the CDALs is valid. Instead of being valid towards the end of clock high time, the address must be examined towards the end of clock low time. Second, clock low time must be lengthened from the minimum specified value for nonrelocated cycles. This allows the MMU time to operate. Third, to prevent a bus conflict, service cannot be on the DALs at the same time as a relocated address. The microprogramming prevents the chip set from loading service data during an address relocation. In addition, the system interface will not drive the DALs with service data at this time.

5.3.1.4 Floating Point Interaction – Floating point instruction is standard in the Professional 350 computer. The FP11 requires the MMU chip's floating point registers. These registers are indirectly addressed by the control field of the I/O microinstructions. The timing of the data transfers to and from these registers is the same as for any other I/O microinstruction. These transfers are transparent to the system user.

The microprogram handles control chip selection. A control chip deselects itself by executing an unconditional jump to another control chip. The target control chip decodes the jump microinstruction and selects itself. This executes the microprogram in a different part of the internal instruction set.

5.3.2 Instruction Cycles and Timing

The following paragraphs describe concepts of instruction and timing cycles used in the Professional 350. It does not explain the PDP-11 instruction set.

1. Section 5.3.2.1 explains micro- and macroinstruction cycles.
2. Section 5.3.2.2 explains the base system timing logic.
3. Section 5.3.2.3 explains how the system creates the needed timing signals.
4. Section 5.3.2.4 explains how the MIB lines are decoded to start a cycle.
5. Section 5.3.2.5 explains the CPU reset function.
6. Section 5.3.2.6 explains the service register's timing between cycles.

5.3.2.1 Instruction Cycles – The chip set emulates PDP-11 macroinstructions with microprograms. This may require several microinstructions to do a single macroinstruction. Microinstructions use the system clock for synchronization. Macroinstructions require longer periods to execute that depend on the instruction performed. Macroinstructions use another internal clock, based on the first, for timing. The chip set tells its support circuits how much time is required and sets up the circuits to synchronize properly.

1. Microinstruction Cycles
   The basic microinstruction cycle (Figure 5-5) shows common operations which occur every microcycle. The conditional latching of service data during a microinstruction cycle is controlled by the Next Address Field of the microinstruction being executed. As far as the system interface is concerned, it should place service data on the CDALs every clock-low time, except during address relocation cycles.

   During certain microinstructions, internal data is placed on the CDALs. This happens because the CDAL drivers are enabled every clock high time unless an input microinstruction is being executed. During certain microinstructions, this data is meaningful; for others the data is not used. As one microinstruction executed the next is accessed. This results in a faster execution of instructions.

   Microinstructions are not included in this manual because they are proprietary and confidential to Digital Equipment Corporation.

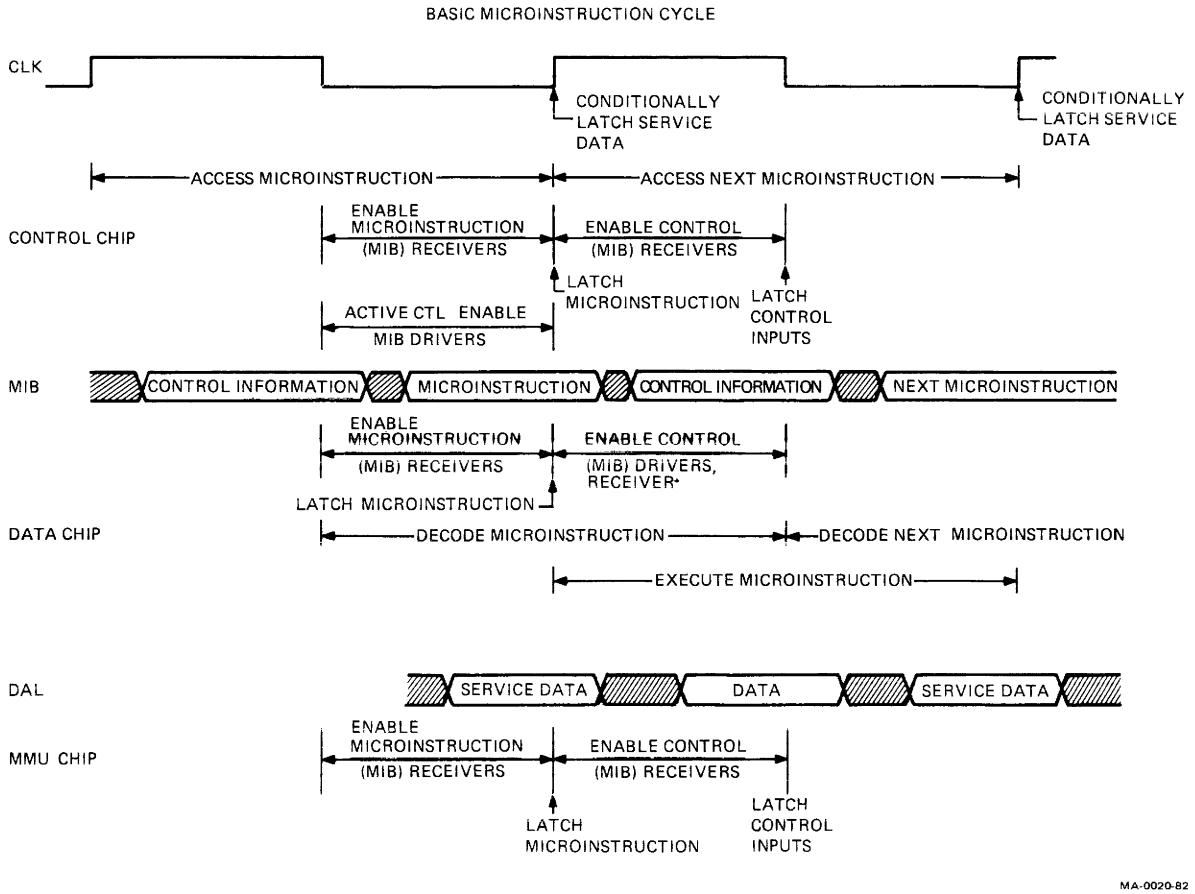


Figure 5-5 Basic Microinstruction Cycle

2. Macroinstruction Cycles
   If service is pending, the appropriate service sequence is initiated. If no service is pending, a macroinstruction is fetched.

   Once a macroinstruction is fetched, the appropriate emulation microprogram is selected. After the completion of the emulation microprogram, the cycle begins again by first determining if service is pending.

5.3.2.2 Basic Timing Logic – The microprocessor operates on microprogram data and instructions during the high and low periods of its clock. This section describes the system clock. The clock uses two signals, oscillator output (OSC H) and PHASE H, to synchronize the CPU and supporting logic. OSC is the system clock. PHASE is the CPU chip set clock.

The oscillator output (OSC H) is the system clock. It regularly sets certain circuits to allow data transfer. During CPU clock high time (PHASE H asserted), the data chip generates control information based on the current microinstruction and transmits this on the MIB. The microinstructions travel along the MIB during CPU clock low time (PHASE H not asserted). The control information on the MIB sets other circuits and determines the duration of PHASE. Depending on the macrocycle, PHASE H and PHASE L remain high or low for specific multiples of OSC. These two clocks, along with other control information, direct the path and timing for data flow.

Three MIB line states indicate the present type of CPU cycle. See Table 5-2. The control circuitry reads the MIB lines and sets timing circuits for PHASE. PHASE's duration, then, varies depending on the status of the MIB lines.

Each microcycle may be an address cycle, a data write, or other operation shown in the table. A read-modify-write cycle to memory requires several different PHASE periods. PHASE stays high depending on which devices are communicating. It may be kept high for two, three, five, or more clock cycles depending on the kind of microcycle. PHASE may be kept high while waiting for a reply from any addressed device and may be kept high indefinitely waiting for DMA. PHASE can be low for two, five, or six clock cycles, again depending on the type of microcycle. If PHASE is kept low longer than six clock cycles, the CPU chips may lose data from lack of refresh. Table 5-3 describes the three basic microcycles.

Table 5-2 System Set Up for Instruction Cycle

MIB AIO 12 2	9 1	8 0	Name	Microinstruction Invoked by	Meaning
0	0	0	AWO	Address	During this cycle, the data chip transmits an address. It is a data write only operation.
0	0	1	ARW	Address	During this cycle, the data chip transmits an address. It is a data read modify write operation.

Table 5-2 System Set Up for Instruction Cycle (Cont)

MIB AIO	12 2	9 1	8 0	Name	Microinstruction Invoked by	Meaning
	0	1	0	–	Unused	
	0	1	1	ARO	Address	During this cycle, the data chip transmits an address. It is a data read only operation.
	1	0	0	WRITE BYTE	Output	The data chip performs a byte output operation. During this cycle, the data chip transmits a data byte. If the address is even, the data is be on the low byte of the DALs. If the address is odd, the data is on the high byte. In both cases the non-data byte is unpredictable.
	1	0	1	WRITE	Output	The data chip performs a word output operation. During this cycle, the data chip transmits a word of data.
	1	1	0	READ	Input	The data chip performs an input operation. During this cycle, the data chip reads a word of data.
	1	1	1	NOP*	All except Address, Input, or Output	Data chip is not performing an I/O operation (neither data in nor data out operation).

* These control signals are forced to NOP (AIO = 7_8) if an input or output microinstruction is executed when the explicit PS address mode is active (for example, if the PS is referenced by its I/O address, the input and output AIO codes are overridden to the NOP AIO code). This information is needed by the control and MMU chips.

Table 5-3 Microcycles

Cycle Description	Cycle Steps
Read Only	ARO, READ
Write	AWO, NOP, WRITE* or WRITE BYTE*
Read-Modify-Write	ARW, READ, NOP, WRITE* or WRITE BYTE*

* The AIO code determines if this is a byte or word operation. Address A00 determines the high or low byte if it is a byte operation.

By coordinating PHASE with OSC, the latches and buffer chips are ready to load address or data information. It is necessary to synchronize times for set-up, hold, and release because of buffer chip parameters and bus specifications.

Example – MIB control information and OSC H produce a sequence of timing signals (including PHASE). The number of signals depends on the type of cycle to be run. Figure 5-6 shows a timing diagram for an address relocation cycle. This operation requires three high clock periods and five low. Note the system clock, OSC, is a periodic signal.

1. PHASE goes high at OSC H rising edge. As PHASE H goes high, its complementary output, PHASE L, goes low. This starts the following timing signal sequence and clears a second timing sequence.

2. At the next OSC H rising edge, Phase Time 2 (PT 2) goes high.

3. At the next OSC H, PT 3 goes high.

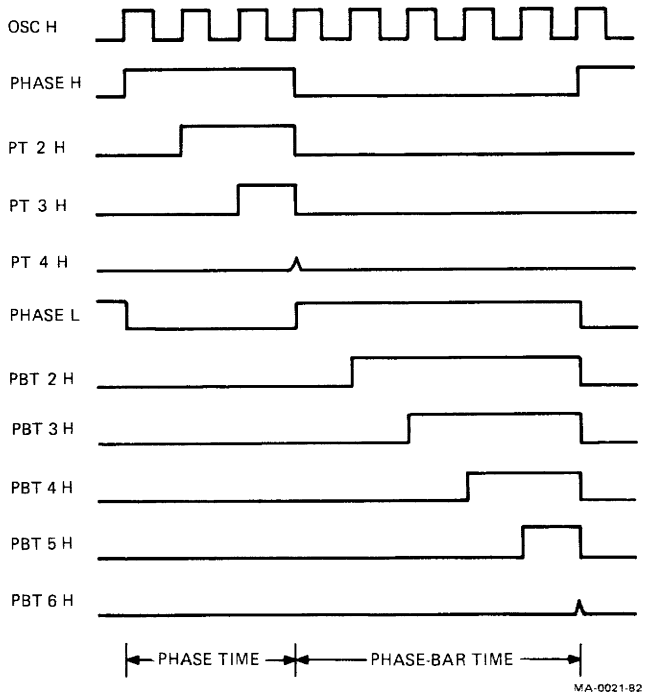


Figure 5-6 Address Relocator Cycle

4. At the next OSC H, PHASE goes low and PHASE-BAR goes high. PT 2 and PT 3 go low. However, PT 4 was clocked in just as the input signals went low so that PT 4 H appears as a spike impulse.

5. As PHASE L goes high, it starts a similar sequence of timing signals during PHASE-BAR.

6. At the next OSC H, PHASE-BAR TIME 2 (PBT 2 H) goes high.

7. At each of the next three OSC H signals, PBT 3 H, PBT 4 H, and PBT 5 H go high respectively.

8. At the sixth OSC H, PHASE-BAR goes low as PBT 6 H appears as a spike impulse.

9. The signals now are PHASE H and PHASE-BAR L.

10. PT 4, PT 5, PT 6, and PBT 6 are not generated during this cycle.

The next section describes how these signals are generated.

5.3.2.3 Detailed Timing Logic – A 26.666 MHz crystal oscillator output is divided by two and buffered to drive the timing logic for the CPU, the CTI Bus control logic, and the DAL Bus control logic. This signal, OSC H, has a period of 75 ns. Figure 5-7 shows the signals used for system timing.

The clock driver uses the PHASE H flip-flop output to produce the +12 V CPU chip set clock signals (CHIP CLKA H and CHIP CLKB H). Each chip set clock cycle consists of a PHASE time (PHASE H set) and a PHASE-BAR time (PHASE H clear). The CPU chip set is semi-static and loses information if it remains in PHASE-BAR time longer than 500 ns. However, it can remain in PHASE time indefinitely. PHASE and PHASE-BAR are complementary.

Two shift registers (PT 2 H through PT 5 H and PBT 2 H through PBT 6 H) operate as clock signal timers during PHASE time (PT) and PHASE-BAR time (PBT), respectively. PT means PHASE TIME and PBT means PHASE-BAR-TIME. If PHASE H is set, but PT 2 through PT 5 are clear, the logic is in phase time one. If PHASE H and PT 2 are set, but PT 3 H through PT 5 H are clear, then the logic is in phase time two. Similarly, if PHASE H is clear and PBT 2 H through PBT 5 H are clear, the logic is in phase-bar time one. If PBT 2 H through PBT 4 H are set, but PHASE H and PBT 5 are clear, then the logic is in phase-bar time four.

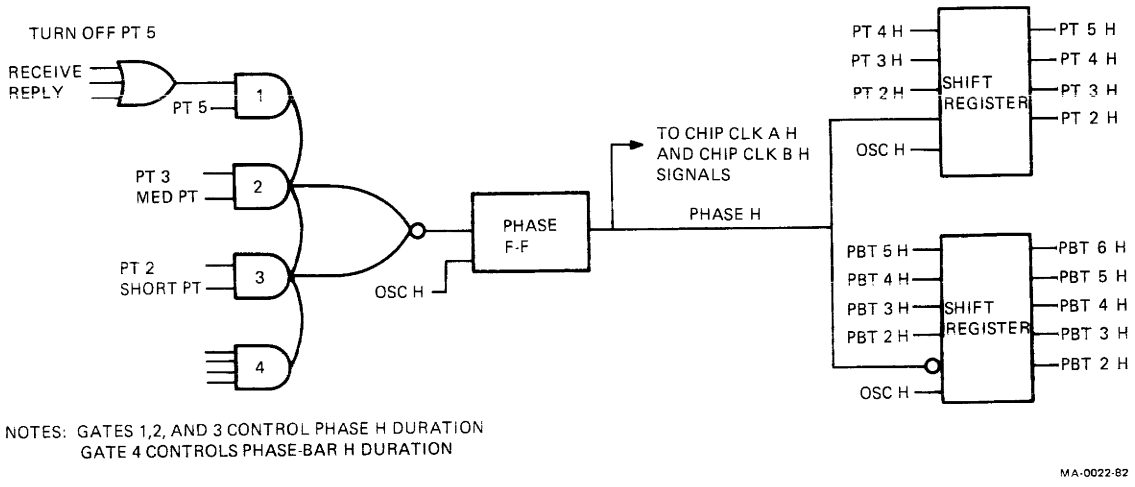


Figure 5-7 Phase Signal Duration Functional Diagram

The PHASE H flip-flop and the two shift registers are clocked on the leading edge of OSC H. When PHASE H is set, the logic advances from one phase time to the next in sequence. However, there is one exception: the logic pauses in phase time one if DMA is in process.

When PHASE H is clear, the logic advances from one phase-bar time to the next. Usually it advances from PBT 2 to PT 1. However, there are two exceptions:

1. During address relocation cycles, the logic enters PHASE after PBT 5.

2. During a reset of the CPU chip cycle, the logic enters PHASE after PBT 6.

A clearing signal clears the flip-flops, which gate data onto the CDAL lines during PHASE time. That data must remain there for one-half OSC period into PHASE-BAR time. The phase time clearing signal clears the flip-flops, which gate data onto the CDAL lines during PHASE-BAR time. That data must remain there for one-half OSC period into PHASE time.

5.3.2.4 MIB Decode Logic – During PHASE-BAR time, the MIB lines contain the current microinstruction provided by one of the CPU control chips (Table 5-2). During PHASE H time, the MIB lines contain control information provided by the CPU data chip. The system logic monitors some MIB lines during PHASE time and some at the end of PHASE time.

During PHASE Time, the MIB lines 12, 9, and 8 contain the address input/output signals (AIO 2, 1, and 0). The AIO codes are decoded to determine whether the current cycle is an address cycle, a bus type data in cycle, or a bus type data out cycle. The AIO lines are signals which determine whether the logic enters PHASE-BAR time after PT 2 (SHORT PT H), after PT 3 (MED PT H), or after PT 5 (SHORT PT H and MED PT H both clear).

At the end of PHASE time, PHASE H clocks the following MIB lines into flip-flops.

1. MIB 15 H to REL CYC H if a memory relocation cycle is indicated.

2. MIB 12 H inverted to LAD CYC L for an address cycle.

3. MIB 07 H inverted (SYNCF H) to LSYNCF L to synchronize the address on the bus.

4. MIB 14 H to INIT H to initialize the system whenever a reset instruction occurs or at power up.

5.3.2.5 CPU Chip Reset – The CPU can remain in PHASE H time indefinitely; PHASE L can remain no longer than 6 clock cycles before data may be lost. Table 5-4 shows error conditions which could cause the CPU to be reset. If one of these errors occur, the system logic generates a reset signal which extends PHASE-BAR time to six clock cycles. Reset enables the CPU service register so the CPU can determine which error condition caused the reset.

5.3.2.6 Service Register – Service information is system status information. The CPU uses this to monitor the conditions shown in Table 5-5. The service information is enabled on the CDAL lines when not doing address relocation when PHASE H is low or during a chip reset. Logic circuits turn on the drivers that place the service data on the CDAL bus for the CPU to read directly.

Table 5-4 Reset Conditions

Signal	Meaning
DCOKC 3 L	DC voltage is OK and present for at least 3 clock cycles. This is a normal condition that causes reset on power up.
BUS ERROR H	The processor put out an address on the bus but there is no response from the device.
NO CSEL H	Neither control chip (CPU nor FPP) is active.
MER H	There is a bus memory error.
ABORT L	MMU chip tried to address an invalid address.

Table 5-5 Service Register

Signal	Meaning
DCOKC 3 L	DC voltage is OK and present for at least 3 clock cycles. This is a normal condition that causes reset on power up.
TIME OUT H	No response was received after putting an address on the bus.
MER L	There is a bus memory error.
ABORT L	MMU chip tried to address an invalid address.
CTL ERR L	Neither control chip (CPU nor FPP) is active.
HALT H	Octal debugging technique signal to start or stop single step operation
PWRFL H	Power failing
IRQ 4 H	Interrupt request

5.3.3 Buses

Both 16-bit addresses and 8-bit data bytes or 16-bit data words are multiplexed over bus data/address lines. During a programmed data transfer, the processor asserts an address on the bus for a fixed time. After the address time is completed, the processor initiates the programmed input or output data transfer. The actual data transfer is asynchronous and requires a reply from the addressed device. The bus synchronization and control signals provide this function.

The bidirectional and asynchronous communications on the buses allow the devices to send, receive, and exchange data at their own rates. The bidirectional nature of the bus allows use of the common bus interfaces for different devices.

Communication between two devices on the bus is a master-slave relationship. At any point in time, there is one device that controls the bus. This device is the bus master. The master device controls the bus when communicating with another device on the bus, the slave. An example of this relationship is the processor which, as master, fetches an instruction from memory (which is always a slave). Another example is a DMA device interface which, as master, transfers data to memory, a slave. Bus master control is dynamic. The bus arbitrator is the processor module.

Since the CTI Bus is used by the processor and all I/O devices, a hardware priority structure determines which device becomes bus master when more than one device requests control of the bus. Every device on the CTI Bus which is capable of becoming bus master is assigned a priority according to its function or type. If two devices of the same priority level each request the bus at the same time, the device in the lower slot number becomes the bus master.

Data transfers on the CTI Bus are asynchronous; communication is independent of the physical bus length and the response time of the slave device. The asynchronous operation between bus master and slave devices depends on synchronizing the bus transactions with clock signals. This allows each device to operate at the maximum possible speed.

Full 16-bit words or 8-bit bytes of information can be transferred on the bus between a master and a slave. The information can be instructions, addresses, or data. For example, this type of information transfer occurs when the processor, as master, fetches instructions and operands and transfers data to and from memory.

Refer to Figure 5-4 for a simplified diagram of the buses and Figure 5-8 for a complete system block diagram showing interfaces. Figure 5-9 shows the buses without other functions. The following paragraphs describe each major bus.

Microinstruction Bus (MIB)

The 16-bit MIB is common to all data and control chips. The MMU receives a subset of the MIB because it does not need access to all MIB control signals. A different subset of the MIB controls the processor support logic.

The MIB is time multiplexed and is used for different functions during clock high and low times. During clock high time, the MIB transfers control information from the data chip to all control chips, the MMU, and the board logic. During clock low time, the MIB transfers microinstructions from the active control chip to other control chips and the data chip.

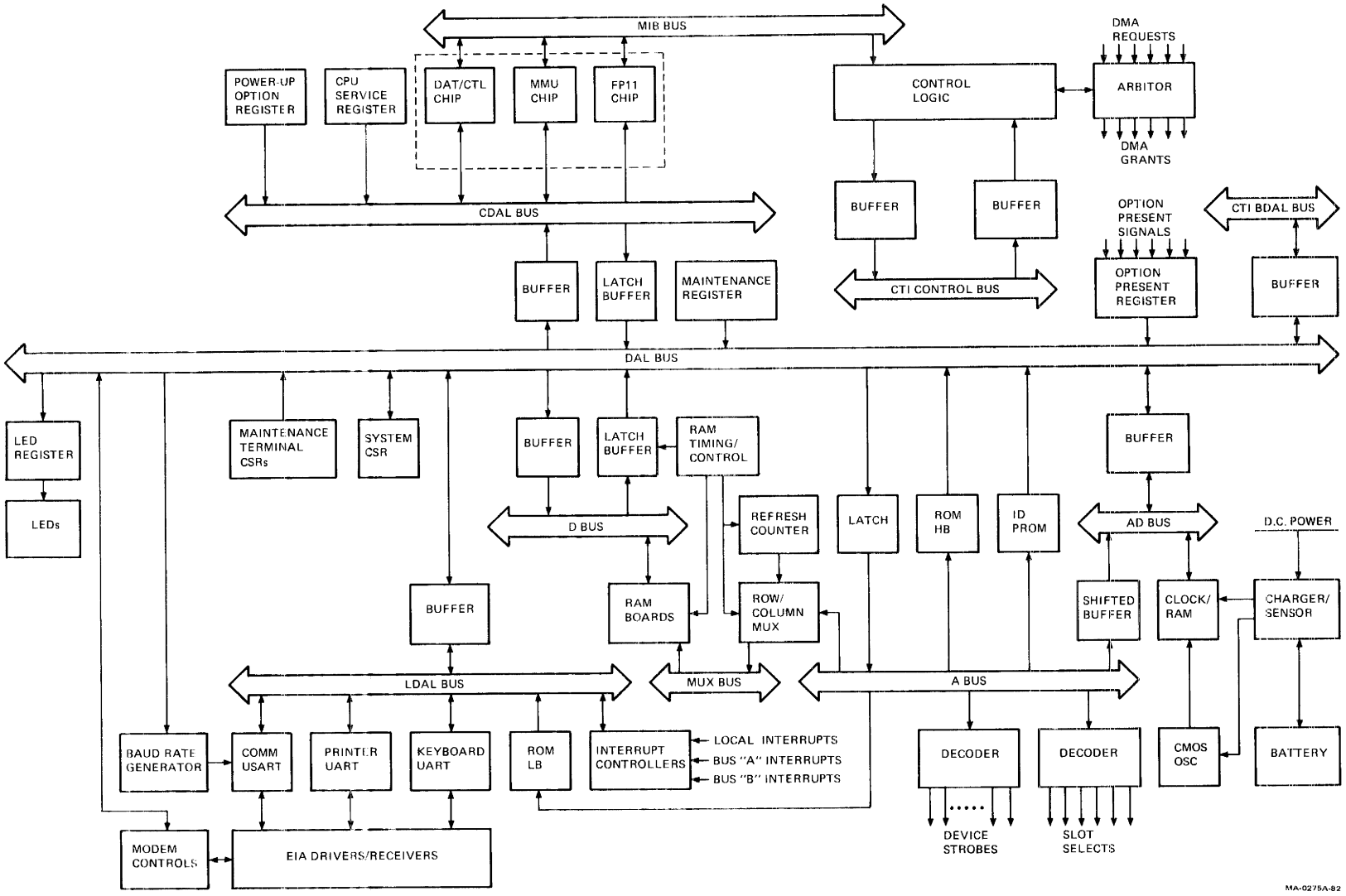


Figure 5-8 System Module Block Diagram

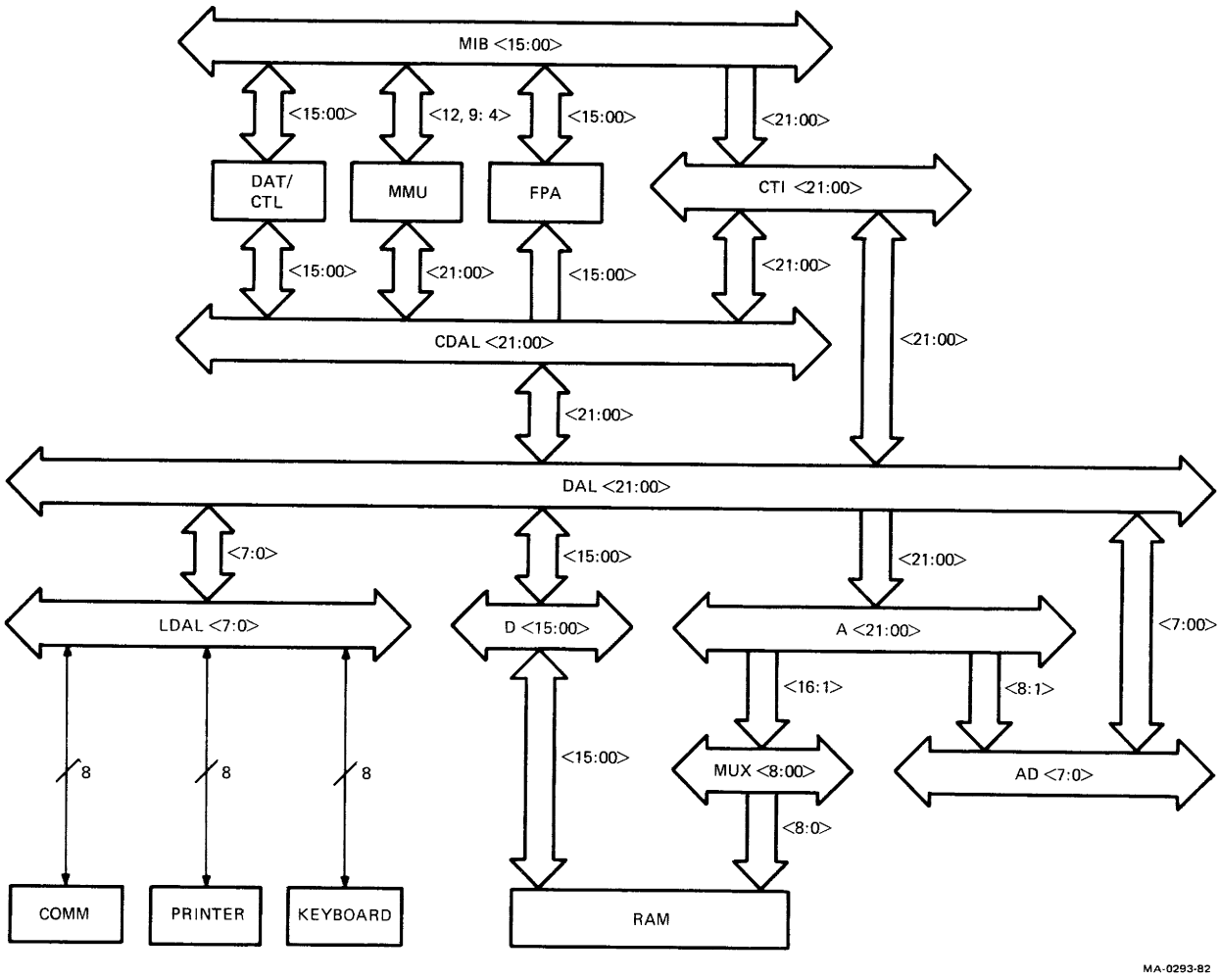


Figure 5-9 Professional 350 System Module Bus Scheme

Data/Address Line Bus (DAL)

The DAL interconnects all the MOS chips and buffers on the processor board. The 22-bit DAL bus is time multiplexed. Of the 22, the CPU uses six lines for addressing only. During clock high time, the data chip transfers information to or receives information from the other chips along the DAL. During clock low time, the board transfers service data (such as interrupt requests) along the CDAL bus to the control chip. The control chip receives service information and determines whether to trap or fetch the next instruction. During clock low time or during address relocation, the relocated address from the MMU transfers to the DAL bus.

Computer Terminal Interconnect Bus (CTI)
The CTI Bus is the control path for the CPU and all options modules. It is also the Professional 350 backplane. The six option slots mounted on the system module connect to the 90-signal bus. All signals are bused to all six slots with the exception of six signals. These six slot dependent signals are on the system module for address decoding, interrupts, and DMA. These signals are as follows.

1. Option present indicator
2. Slot select from the I/O page address decoder
3. Two interrupt request lines (A, B) from each option
4. DMA request from the option
5. DMA grant from DMA arbitration circuits

Each option slot has a 90-pin connector on the system module. The first 60 pins are used for the CTI Bus signals. These are referred to as the general section of the bus. This section of the bus is control lines and bused data/address lines (CTI/BDAL). The last 30 pins, 61 through 90, route signals from the option modules to connectors on the rear of the system module. These are referred to as the private section of the bus. An option module that only needs the CTI Bus signals can use a 60-pin Zero Insertion Force (ZIF) connector. An option module that uses the rear connectors on the system module must use a 90-pin ZIF connector. Section 5.3.5.2 describes the bus timing relationships. Refer to Section 5.5 and Table 5-30 for the CTI Bus signal definitions.

D Bus
The D bus is the data path to and from the externally mounted RAM daughterboards. Data from the DAL bus can be written to RAM via the D bus when the WRITE signal is asserted and then written directly to the daughterboards. A RAM read causes data to be latched from the D Bus into three-state latches for release to the DAL bus. The RAM modules are addressed via the A Bus.

A Bus
The CPU and DMA devices use the A Bus to address all I/O devices and memory. Addresses are latched from the DAL bus and held until the bus cycle is completed. Logic uses the A Bus to activate device strobes, slot selects, ROM, registers, and RAM addressing.

AD Bus
This bus accesses the battery backed up clock chip. It also permits battery backed up RAM addressing and data transfer. This is a low byte only bus. Refer to Section 5.3.4.1 for further information.

LDAL Bus
This bus is the low driver data/address bus. It is the system's interface to devices with low drive outputs: the keyboard, printer, and communications ports. It also carries interrupt vectors to the CPU from the interrupt controller chips. It carries low drive signals to a TTL buffer which drives the DAL bus. It is a low byte-only bus.

CDAL Bus
The CDAL bus is an interface bus between the CPU chips and the DAL bus. The CPU chips have low output drive and would be loaded down by the DAL bus and its interface logic.

MUX Bus
The MUX bus carries address data from the A Bus to the RAM daughterboards. Quad 2:1 multiplexers transmit first the low, then the high bytes of address data to the RAMs. Refresh address for the RAM also uses the MUX bus. The system module can support up to 512 kilobytes per daughterboard using a ninth address line.

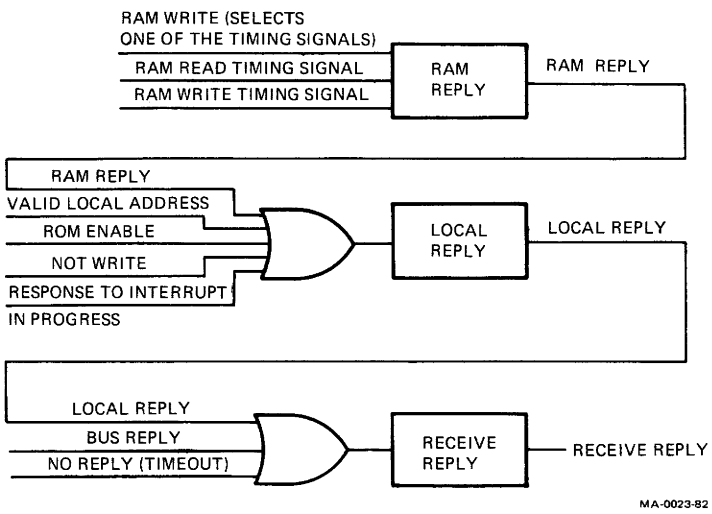


Figure 5-10 Reply

5.3.3.1 Bus Reply – All bus cycles require the enabled device to reply, whether it is a local (system module) or CTI Bus device. The CPU stops in PHASE time and waits for a reply. The reply ends PHASE time. Figure 5-10 shows the reply signals and the signals that enable them. Each device needs a different time to reply which depends on its speed. Therefore, the device determines when PHASE ends via its reply time.

If PT 4 H is asserted, the CPU is on the bus and a DMA device cannot use the bus. If PT 4 H is sent, there are 6.5 μs for a device to reply. If no reply comes, a timer times out and asserts the reply signal. The reply ends PHASE time but indicates a timeout error to the CPU.

5.3.3.2 Other Bus Control Signals – Other signals which control data flow on the CTI Bus and internal buses are as follows.

1. ADDRESS STROBE – Occurs on OSC L. Refer to Figure 5-11.

2. DATA STROBE – Occurs on OSC H. Refer to Figure 5-11.

3. MDEN – Master Drive Enable indicates that the master is placing an address or data on the bus. Refer to Figure 5-12.

4. SDEN – Slave Drive Enable indicates that a slave should drive data on the bus. Refer to Figure 5-12.

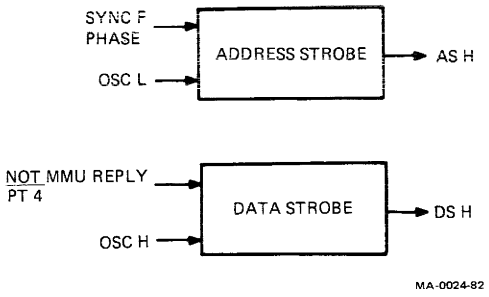


Figure 5-11 Address and Data Strobe

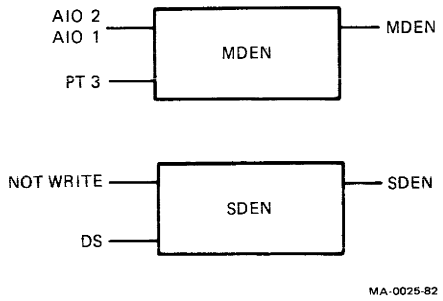


Figure 5-12 Master and Slave Drive Enable

5.3.4 Bus Interfaces

Bus interfaces in the Professional 350 fall into two categories, buffers and registers. Buffers isolate electrical circuits from each other. For example, a buffer permits passage of data on one bus to another to meet device drive or timing requirements (Section 5.3.4.1).

Registers hold status information for the CPU to read. They transfer their data directly to the appropriate bus when addressed and enabled (Section 5.3.4.2).

5.3.4.1 Buffers – There is an interfacing buffer between each pair of buses. These buffers switch a data path to and from different circuits according to CPU instructions and the timing requirements of different circuits.

Although buffers switch signals, they can also change drive level requirements depending on the requirements of the devices they serve.

Figure 5-13 shows the system block diagram with only buses and buffers. Each buffer on the figure has a number which corresponds to the following numbered paragraphs. These paragraphs describe buffer's function. Figure 5-13 also shows the enabling signals and the transceivers that change the buffers' direction.

1. CDAL – DAL Buffers – Signals from the CPU on the CDAL bus are always passed as 16 bits. They are clocked into latch buffers at the first OSC L rising edge during PT 3 H or at the rising edge of PBT 4. The CPU enables output to the DAL bus when it becomes bus master. This places either an address or data on the bus.

2. DAL – CDAL Buffers – This buffer permits data from the DAL bus to be gated onto the CDAL bus and to the CPU chip set. The signals are clocked in on the falling edge of the PHASE H signal.

3. DAL – CTI/BDAL Buffer – This buffer consists of three octal bus transceivers between the DAL and CTI/BDAL buses. The CTI/BDAL bus connects the DAL bus to all slots on the CTI Bus. The CPU transmits address to the DAL bus in 22-bit words. Data to or from the CTI/BDAL bus is transferred in 16-bit words (BDAL 15:00).

4. DAL – A Bus Address Latches – Latch buffers transfer addresses on the DAL bus to the A Bus. All DAL lines and BSIO in DMA devices must assert 22-bit addresses and BSIO. The master also uses 22-bits at address strobe time. The chips in this circuit require set up time for the addresses to stabilize on the bus before latching them.

5. DAL – LDAL Buffer – This buffer uses an octal transceiver to transmit eight bits of data. The LDAL, a low drive bus, connects to devices that provide low drive. The buffer amplifies these devices and puts the signals directly on the DAL bus.

6. DAL – D Buffer – Data for RAM on the DAL bus is written to the D Bus during write operations. The data is then transmitted directly to the RAM chips.

7. D – DAL Buffer – Data in RAM is available after addressing. The data is latched in tri-state latch buffers when a valid RAM request is made. A RAM read signal enables the output. This places the data on the DAL bus.

8. A – AD Buffer – This shifted buffer passes address data (A08–01) to access RAM and registers in the battery backed-up clock/RAM circuit. A08–01 are used because the address bit A00 normally selects high or low byte data. Since this circuit is a low byte device, A00 is not used by the chip. Therefore the address is shifted one bit to A08–01, instead of A07–00. The address is valid at the address strobe signal.

9. DAL – AD Buffer – This octal bus transceiver permits data transfer to and from the battery backed-up clock/RAM circuit. It is enabled by the address decoder and data strobe signals.

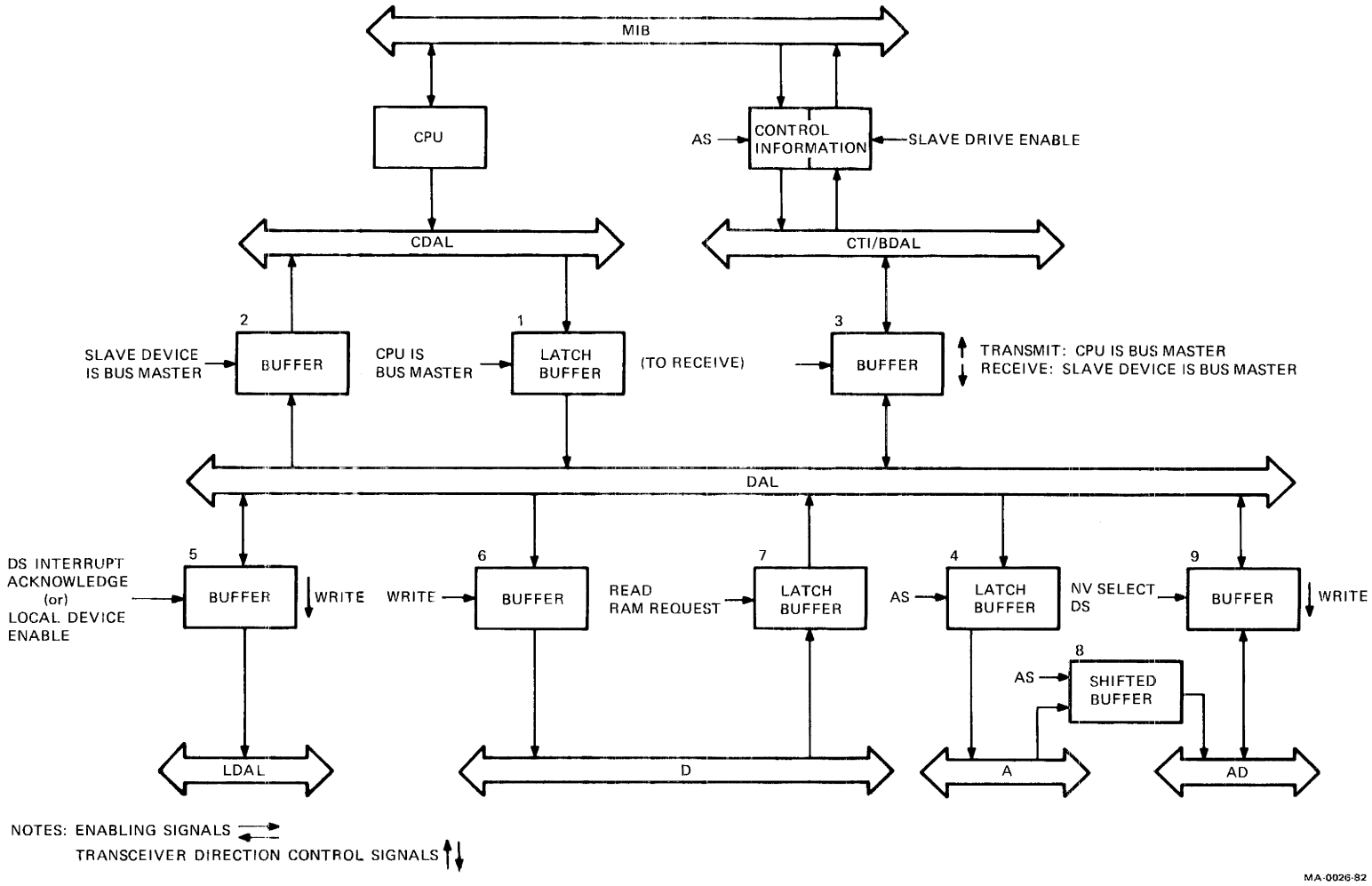


Figure 5-13 System Block Diagram with Bus Interfaces

5.3.4.2 Registers – Registers hold status information or other information needed for data processing. Certain interrupt data, power level data, and system configuration data are examples of the kinds of data stored in registers.

Figure 5-14 shows the system block diagram. Each register on the figure has a number that corresponds to the following numbered paragraphs. These paragraphs describe each register's function.

1. Power Up Option Register
   This register, on the CDAL lines, is an octal tri-state buffer. It is read at power up to make the CPU go to an address in the system ROM (17760000) and begin executing the code there to start the power-up self-test.

2. CPU Service Register
   This register stores information about power, errors, and interrupts. Refer to Section 5.3.2.6 for a list of service register functions.

3. Maintenance Register (Address 17777750)
   This register tells the system software the type of CPU and hardware configuration. The software can then configure itself to the hardware configuration.

   When the computer is booted, the operating software asserts address 17777750. The address decoder asserts the signal LREPLY H and the CPU waits for a response. Since 17777750 is an invalid address, there is no response. This means that no device is driving the bus. The software then reads the bus (which is all low) and interprets this to mean a Professional 350 computer.

4. Option Present Register (Address 17773702)
   A hardwire in each option module pulls a line low when it is inserted in its slot. These assert the signals OPRES 0 through 5 L.

   When the CPU needs to determine which slots are used (to determine address ranges), it puts this register's address on the A lines. When decoded, it asserts RD OPRES L. RD OPRES L enables the register and puts the data on the DAL lines. The buffer control signal SDEN L permits the buffers to transfer the data to the CDAL lines which connect directly to the CPU data chips.

5. Indicator (LED) Register (Address 17773704)
   This LED register is a system status indicator. There are five LEDs on the back of the system module (one green and four red LEDs). The green LED lights when the power supply asserts the DCOK signal. The four red are error indicators used by the power-up self-test. Table 5-6 indicates the error condition for each LED code.

   The LED display register uses only the first four bits of the low byte. It controls the state of the four red LEDs on the rear of the unit. The register is reset at power up. (At power up, all four red LEDs are on.) The first error is latched and held and the LED display indicates the error found. Otherwise the register is always read as all 0s. All writes to the high byte have no effect.

   Figure 5-15 shows the positions of the LEDs if viewed from the back of the unit.

6. Maintenance Terminal Control and Status Register (Address 17777560–17777566)
   A console terminal can be connected to the system through the printer port for maintenance debugging and testing. The console terminal interface is made of four registers at addresses 17777560–177777566. The microcode Octal Debugging Technique (Micro-ODT) accepts 16-bit addresses which permits addressing 56 kilobytes of memory plus the 8 kilobytes I/O page.

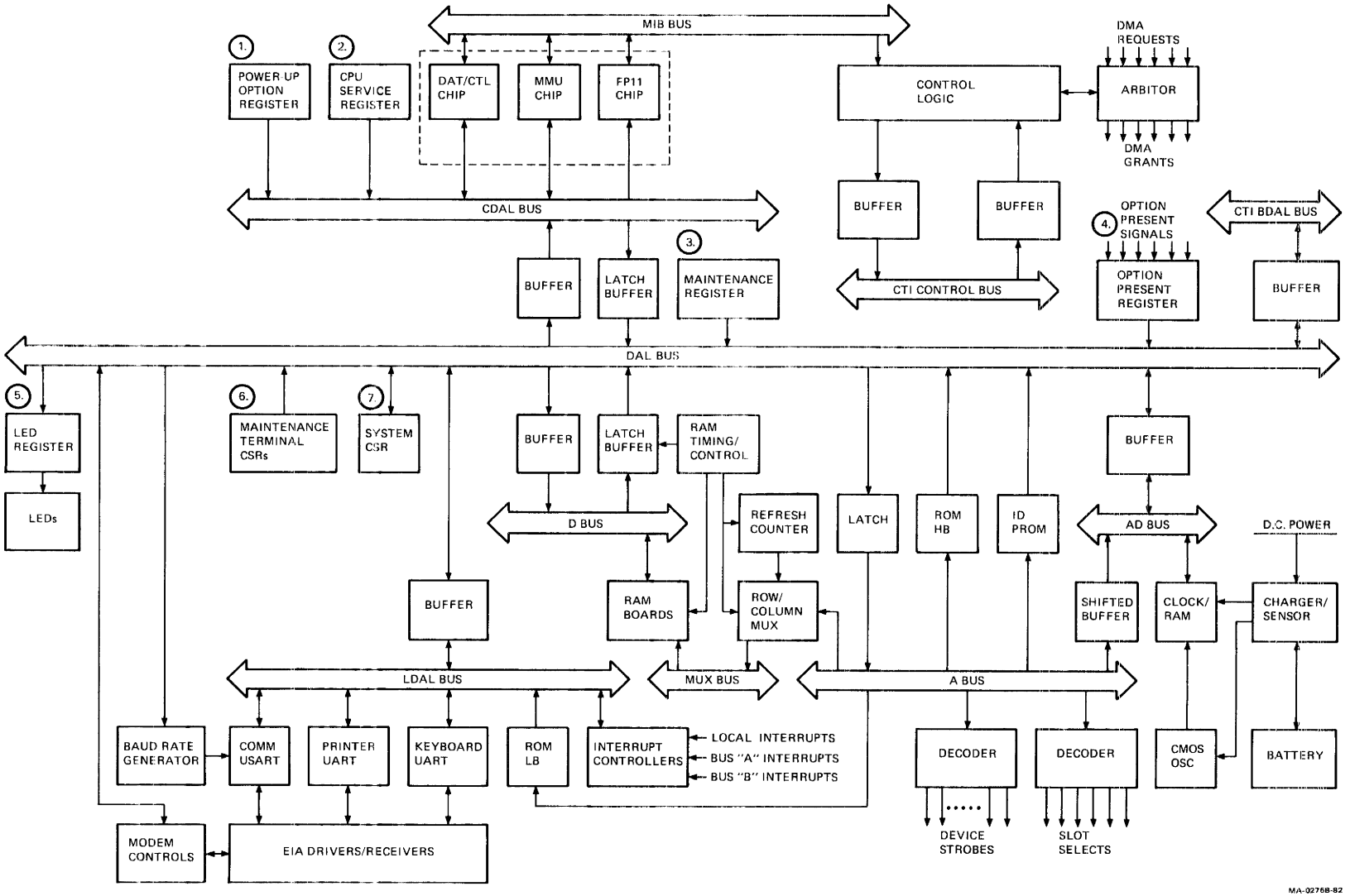


Figure 5-14 System Block Diagram with Register

Table 5-6 Indicator (LED) Error Codes

LED 3	LED 2	LED 1	LED 0	Error Condition
off	off	off	off	None – self-test found no errors
off	off	off	on	Bus slot 0 error detected (physical slot 1)
off	off	on	off	Bus slot 1 error detected (physical slot 2)
off	off	on	on	Bus slot 2 error detected (physical slot 3)
off	on	off	off	Bus slot 3 error detected (physical slot 4)
off	on	off	on	Bus slot 4 error detected (physical slot 5)
off	on	on	off	Bus slot 5 error detected (physical slot 6)
off	on	on	on	Invalid – reserved
on	off	off	off	Invalid – reserved
on	off	off	on	Keyboard failed
on	off	on	off	No boot found
on	off	on	on	Monitor cable not present
on	on	off	off	Memory in slots 0 and 1 both failed
on	on	off	on	Memory in slot 1 failed (low bank)
on	on	on	off	Memory in slot 0 failed (low bank)
on	on	on	on	System module failed*

* All the LEDs are lit at power up (lamp test). If they all remain lit, a system module error is indicated.

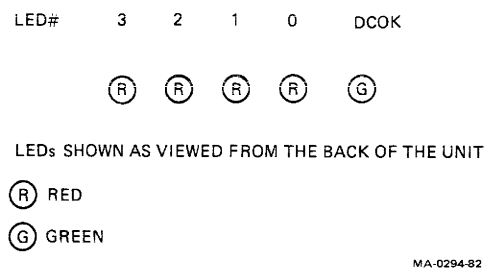


Figure 5-15 Indicator (LED) Display

7. System Control and Status Register (CSR) (Address 17773700)
This register tells the CPU which memory module(s) is (are) present (0 and/or 1) and the size (128 or 512 kilobytes). It also tells if a monitor cable is connected to the system. In addition, the register enables or disables the break detect from the printer interface.

   The CPU puts this register's address on the A lines, which, when decoded, assert RD STATUS L. RD STATUS L enables the register and puts the data on the DAL lines. The buffer control signal, SDEN L, allows the buffers to transfer the data to the CDAL lines which connect directly to the CPU data chips.

5.3.5 Other Control Logic

This section describes the control logic used to select or enable devices on the system module or on the CTI Bus.

5.3.5.1 Slot Select Decoder – The slot select decoder uses addresses and selection signals to enable different slots on the CTI Bus. It asserts a slot select signal (SS n L).

During clock high time of a memory management address relocation cycle, the MMU chip determines if the address the CPU control chip puts out is in the I/O page range (17760000–17777776). During clock low time, if it is in the range, the MMU chip puts out a relocated address on the CDAL bus and enables BSIO H. BSIO H is asserted as BIOSEL L on the CTI Bus and is latched with BSIO and the A Bus address. Latched BSIO H is LBSIO H which, along with A bus signals A 12:10, enables the slot select decoder. The decoder uses address lines A 9:7 to assert the slot number selection. Table 5-7 provides each slot's address assignments. Address assignments depend on slot number, not device type.

Table 5-7 Slot Select and Address Ranges

Slot	Address Range
0	17774000–17774177
1	17774200–17774377
2	17774400–17774577
3	17774600–17774777
4	17775000–17775177
5	17775200–17775377

5.3.5.2 I/O Page Address Decoder – The I/O Page Address Decoder is a local device address decoder. It is a programmable logic array (PLA) that recognizes device addresses and enables the corresponding circuit. For example, if an address for battery backed up RAM is on the bus, the decoder asserts a battery backed up RAM enable.

When an address is on the bus, all devices read the address but only the enabled devices can react to it. The decoder decodes addresses and enables devices for data transfer. System logic coordinates the data flow on the buses. It opens the appropriate buffers at the right times to permit reading addresses and data and holds buffers and latches for specified times. System logic uses the system clock and timing signals generated by PHASE time.

The following are examples of data flow. Refer to Figure 5-13 for each of the examples. This figure shows the system block diagram with bus interfaces only. In addition, each example refers to an illustration that shows the system block diagram and the address and data flow. Table 5-8 shows the system memory map with addresses.

Example 1 – CPU Writing to I/O Device (Refer to Figure 5-16).

1. The CPU indicates it is to be bus master and latches the address into the CDAL-DAL latch buffer. This puts the address on the DAL bus. Address strobe also transfers the address to the A bus. System control logic decodes microinstructions on the MIB bus to generate necessary control signals.

Table 5-8 System Module Memory Map

00000000–????????*	RAM – main memory
17730000–17767776	16Kb ROM – diagnostic/boot
17772300–17772316	MMU – kernel PDRs
17772340–17772356	MMU – kernel PARs
–17772516	MMU – SR3
17773000–17773032	Clock registers
17773034–17773176	Battery Backed-up RAM – 50 bytes
17773200–17773212	Interrupt controller registers
17773300–17773314	Communication port registers
17773400–17773406	Printer port registers
17773500–17773506	Keyboard registers
17773600–17773676	ID PROM
–17773700	System CSR
–17773702	Option module present register
–17773704	Indicator (LED) display register
17774000–17774176	Option module slot 0
17774200–17774376	Option module slot 1
17774400–17774576	Option module slot 2
17774600–17774776	Option module slot 3
17775000–17775176	Option module slot 4
17775200–17775376	Option module slot 5
17777560–17777566	Maintenance terminal registers
17777572–17777576	MMU – SR0, SR1, SR2
17777600–17777616	MMU – user PDRs
17777640–17777656	MMU – user PARs
–17777750	Processor maintenance register
–17777776	Processor PSW

* Upper address limit depends upon the amount of RAM the system is configured with. All addresses are 22-bit octal format. The system module supports addressing on the daughter modules up to 1 megabyte; the system supports up to 3 megabytes.

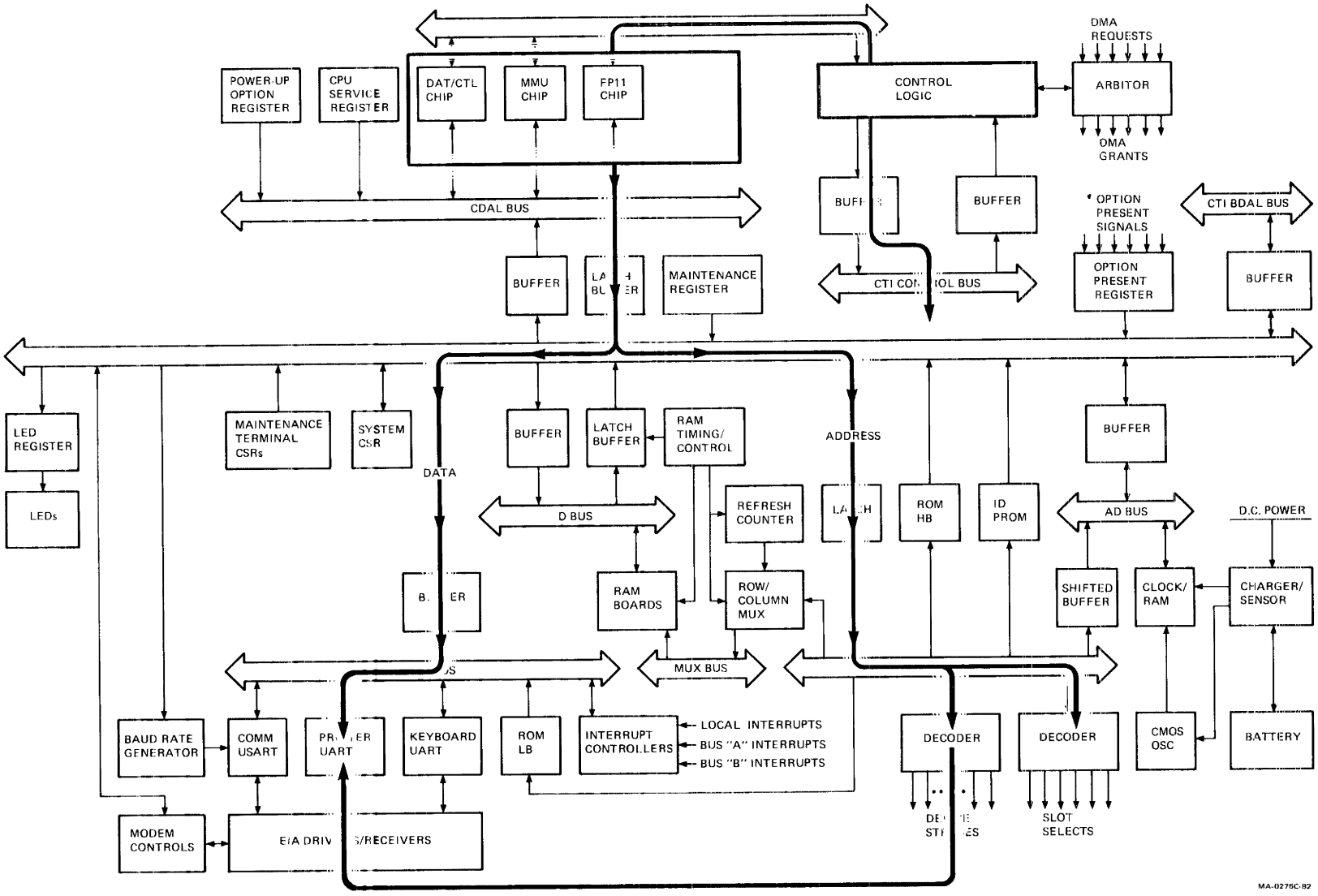


Figure 5-16 CPU Writing to I/O Device

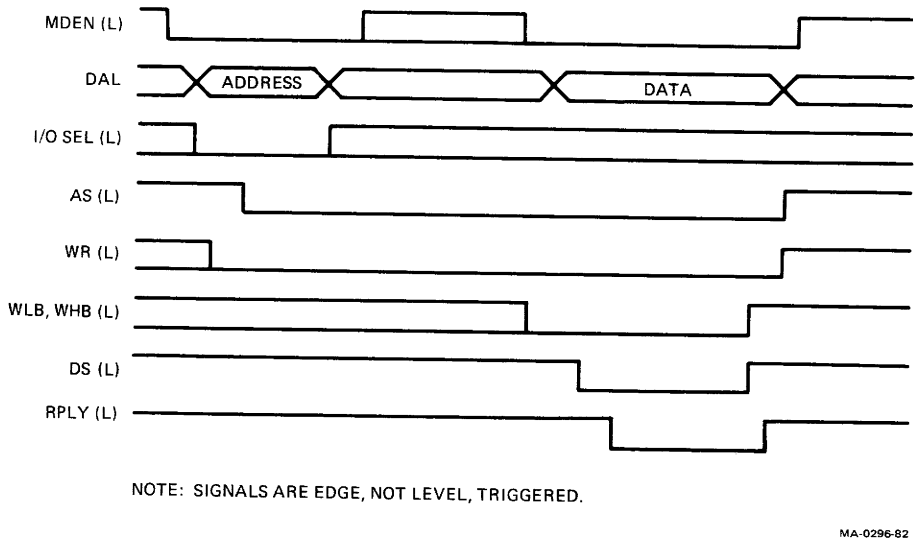


Figure 5-17 Simplified CTI Bus Timing Relationships During Write Cycle

2. The address decoder decodes the address and, if valid, enables the device (here the printer USART). The ROM, RAM, and slot address decoders also read the address but do not enable because the address is invalid for their devices.

3. On data strobe, the DAL-LDAL buffer transfers data to the LDAL bus and to the printer USART.

   Although this example shows writing to an I/O device, the signals are also asserted on the CTI Bus. Since no device on the bus was addressed (slot select), the bus devices do not respond. The address decoder responded to the address, enabling the printer USART. Figure 5-17 shows a simplified bus timing relationship for signals on the CTI Bus.

Example 2 – CPU Read from RAM on a daughter module (Refer to Figure 5-18.)

1. The CPU indicates it needs to read from RAM. It signals it is to be bus master and latches the address into the CDAL-DAL latch buffer. This puts the address on the DAL bus. Address Strobe also transfers the address to the A Bus.

2. The RAM address decoder decodes the address, recognizes that it is a valid RAM address, and asserts a RAM enable. This decoder is a 256 × 4 PROM decoder which enables the appropriate RAM daughterboard module. (There are two possible).

3. The address is now on the A Bus. A delayed address strobe signal and the system RAM enable assert signals that transfer the address to a multiplexer driver which, in turn, puts the address on the RAM chips. Note that the address is also on the CTI Bus but external RAM does not respond because the address is not decoded in their ranges.

4. Once addressed, the data in RAM is available for reading. Additional system timing signals open the latch buffers, putting the RAM data on the DAL bus. The CPU has finished addressing and enables the slave drive enable signal. This allows a slave device to drive the bus. This signal enables the DAL-CDAL latch buffer and gates the data to the CDAL bus which connects directly to the CPU chip set.

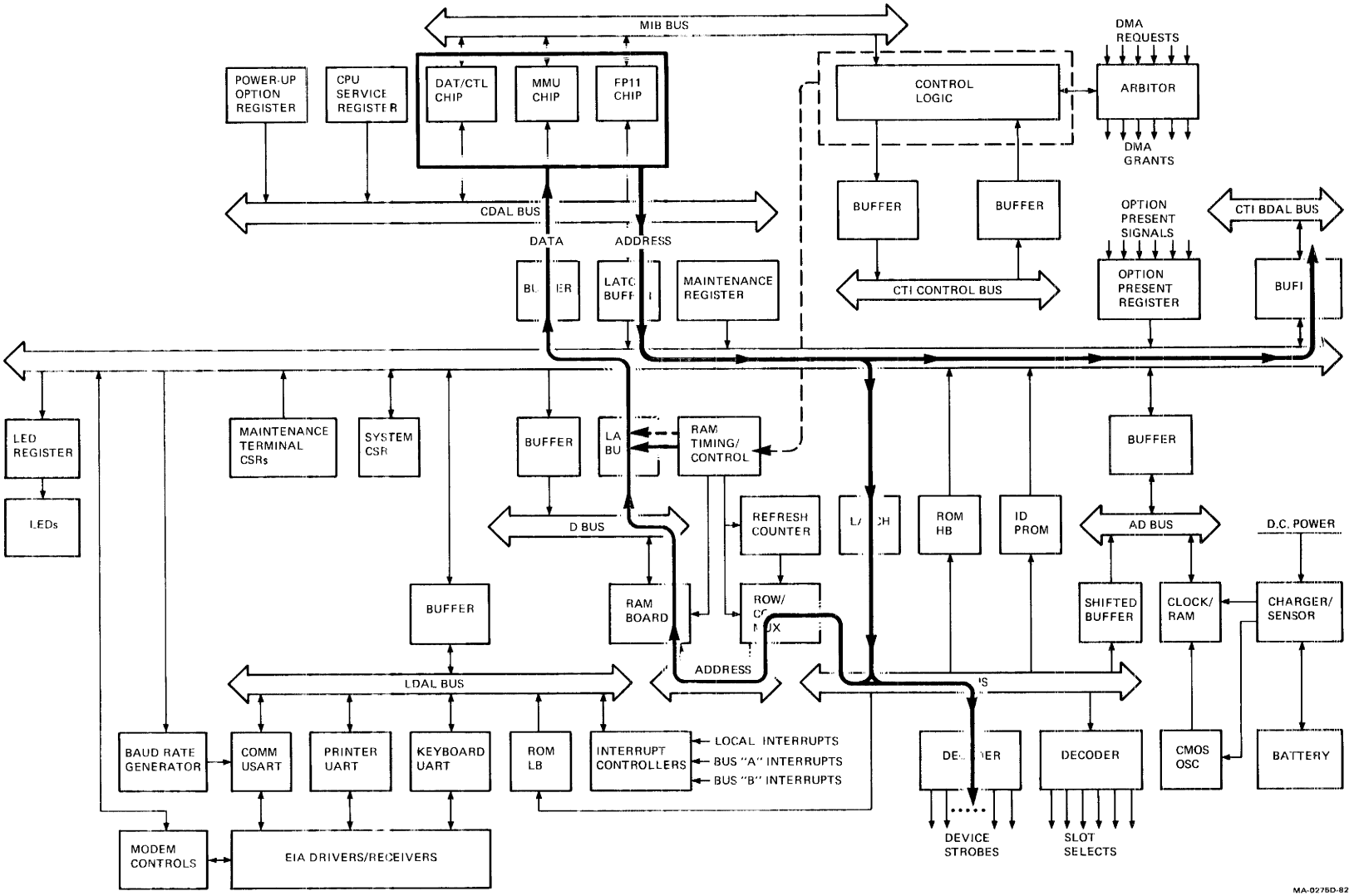


Figure 5-18 CPU Read from RAM

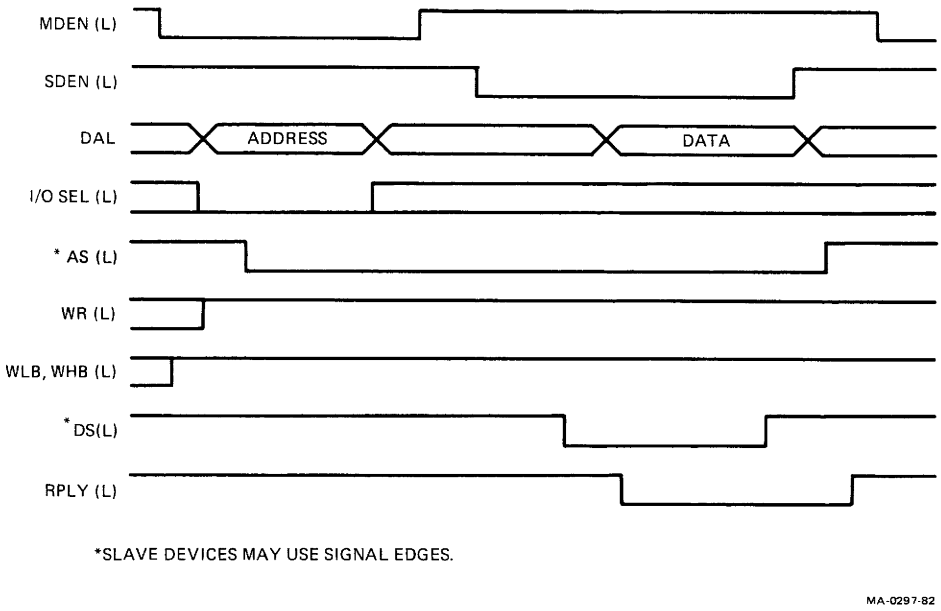


Figure 5-19 Simplified CTI Bus Timing Relationship During a Read Cycle

5. If the CPU requires backplane RAM, the system board RAM enable is not generated and the appropriate device on the CTI Bus decodes the address and would reply from the bus.

   Although this example shows reading from RAM, the signals are also asserted on the CTI Bus. Since no device on the bus was addressed (slot select), the bus devices do not respond. The address decoder responded to the address, enabling RAM. Figure 5-19 shows a simplified CTI Bus timing relationship during a read cycle.

Example 3 – DMA Request and Grant (Refer to Figure 5-20. Also refer to Section 5.3.7 for a description of DMA).

1. A device on the CTI Bus signals a request for DMA. A hardwire circuit chooses which DMA request is first.

2. The DMA selection circuit gives a DMA grant to the first device requesting DMA.

3. The device asserts it is bus master and puts an address on the DAL bus and then address strobe.

4. Address strobe latches the address to the A Bus and then it is decoded. The appropriate memory (either RAM daughterboard or RAM in the backplane) is enabled. If the required operation is a write to memory, the DMA device asserts the write signal.

5. On data strobe, data transfers to or from the bus master (the device). The direction depends upon the state of the WRITE signal. If the bus master writes to the RAM daughterboards, the DAL-D buffer transfers the data.

   Figure 5-21 shows a simplified CTI Bus timing relationship for a DMA request and grant cycle.

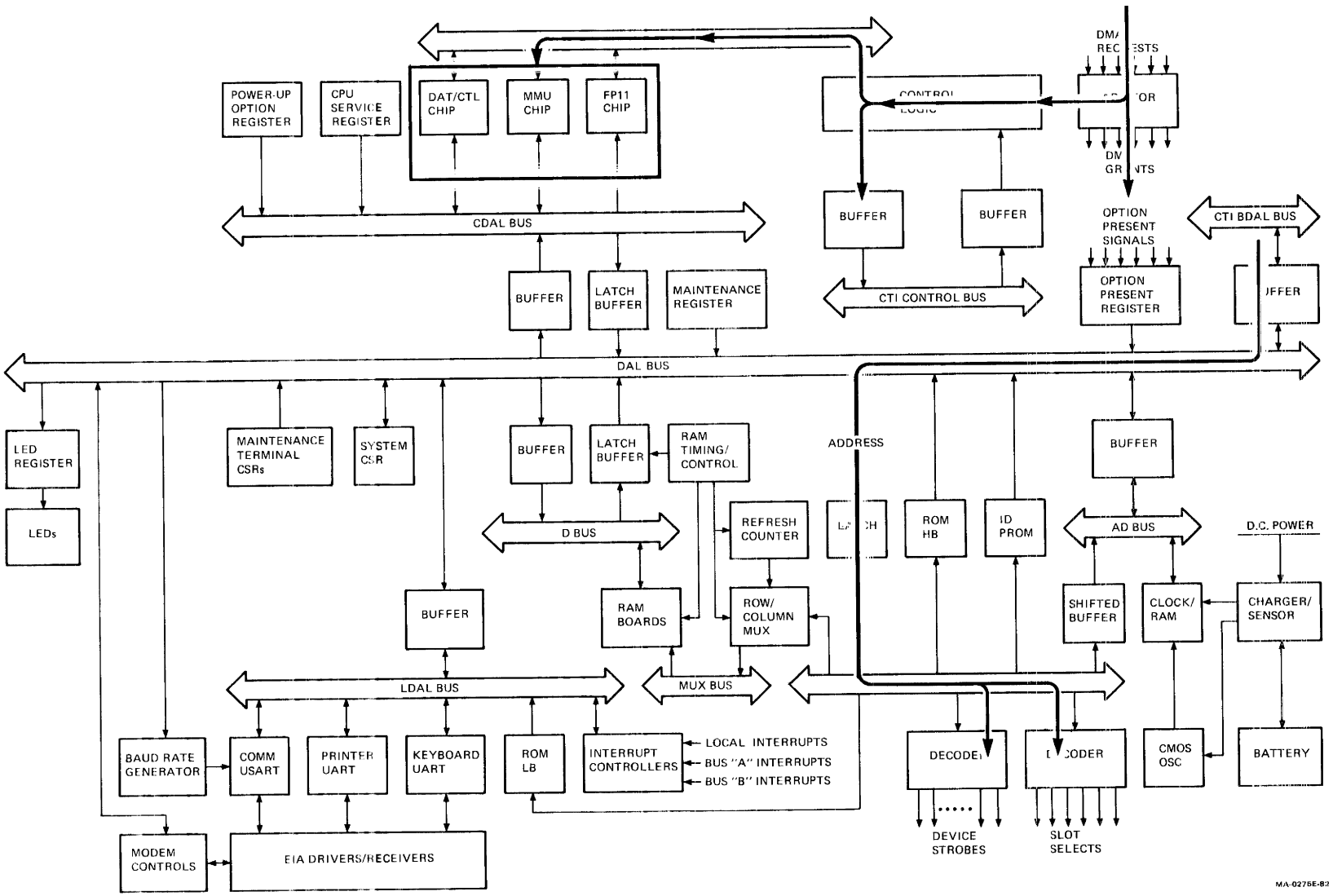


Figure 5-20 DMA Request and Grant

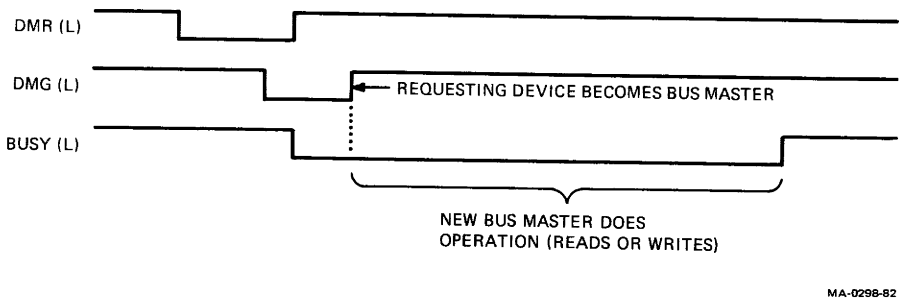


Figure 5-21 Simplified CTI Bus Timing Relationship During a DMA Request/Grant Cycle

Example 4 – CPU Writing Out to RAM on a daughter module (Refer to Figure 5-22).

1. The system mounted RAM modules are addressed as in example 1.

2. A clock signal enables the data transfer from CPU to DAL bus, then to the DAL-D buffer. The CPU asserts a write signal. The WRITE signal enables the buffer, putting the data on the D Bus. The WRITE signal also enables RAM to write.

3. Since the RAM chips were enabled once addressed, data strobe clocks the data into RAM.

4. If the CPU required backplane RAM, the system RAM enable is not generated and the appropriate device on the CTI Bus decodes the address and would reply from the bus.

5.3.6 Interrupt Vector Circuit

The system module uses three interrupt controller chips (9519A) to handle all the system interrupts. The first controller handles all the interrupts generated by devices on the system module. The second controller handles all the A interrupts from the option modules and the third controller handles all the B interrupts from the option modules. The interrupt controllers latch the interrupt requests, provide the interrupt enable for each, prioritize the pending interrupts, and generate the proper vectors (Figure 5-23). Firmware programs the controller chips to prioritize pending interrupts and generate their vectors. The controllers interrupt the CPU at processor status level 4.

After acknowledgement, the device interrupt request line must be unasserted and then reasserted to generate a new CPU interrupt request.

Refer to Table 5-9 for the interrupt controller assignments.

Each of the interrupt controllers has a set of registers which control the specific features of operation. These registers are accessed via the CSR and data registers. Refer to Section 5.4 for details on these registers.

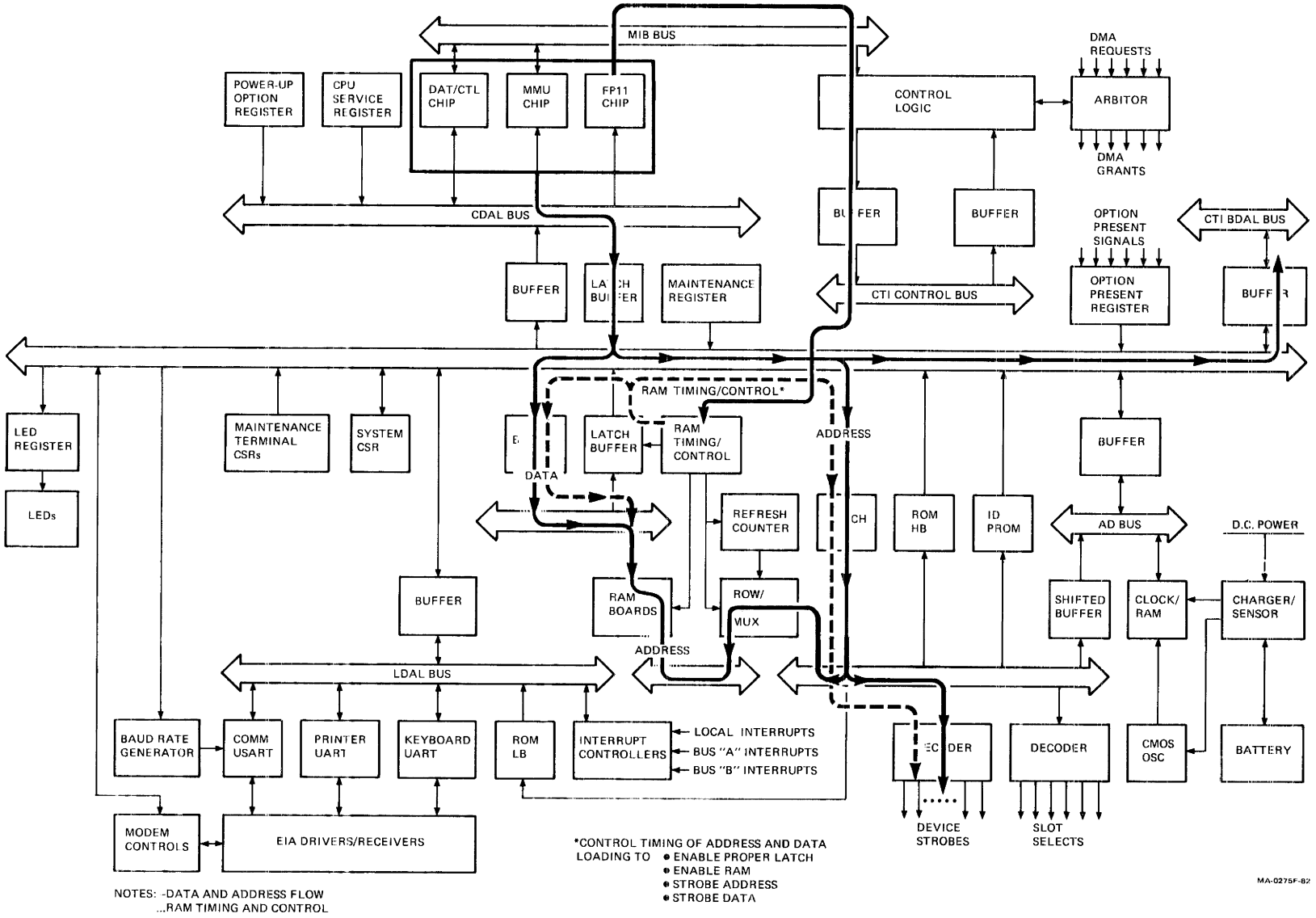


Figure 5-22 CPU Writing Out to RAM

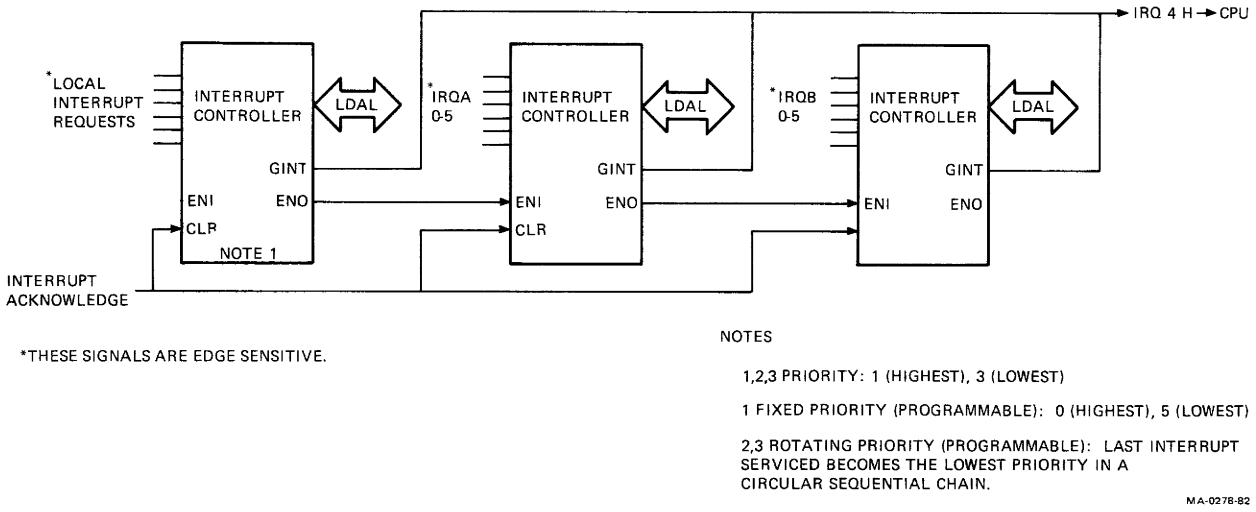


Figure 5-23 Functional Interrupt Control Circuit

Table 5-9 Interrupt Controller Assignment

Controller	Request Level	Vector*	Interrupt Description
0	0	—	Not used
	1	200	Keyboard receiver interrupts
	2	204	Keyboard transmitter interrupt
	3	210	Communication port interrupt
	4	214	Modem controls change interrupt
	5	220	Printer receiver interrupt
	6	224	Printer transmitter interrupt
	7	230	Clock interrupt
1	0	300	Option module 0 interrupt request A
	1	310	Option module 1 interrupt request A
	2	320	Option module 2 interrupt request A
	3	330	Option module 3 interrupt request A
	4	340	Option module 4 interrupt request A
	5	350	Option module 5 interrupt request A
	6	—	Not used
	7	—	Not used
2	0	304	Option module 0 interrupt request B
	1	314	Option module 1 interrupt request B
	2	324	Option module 2 interrupt request B
	3	334	Option module 3 interrupt request B
	4	344	Option module 4 interrupt request B
	5	354	Option module 5 interrupt request B
	6	—	Not used
	7	—	Not used

* Firmware establishes these vectors at power up.

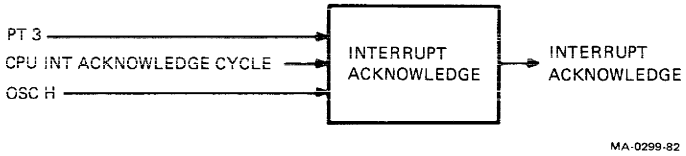


Figure 5-24 Interrupt Acknowledge Signal

5.3.6.1 Interrupt Service – A device interrupt can be generated at any time. The CPU, by reading the service register, knows when PHASE H is low. When the CPU receives an interrupt, the CPU stops processing, stores its current location and function internally, and changes to an interrupt handling routine. When the CPU asserts an interrupt acknowledgement signal (Figure 5-24), it is ready to read the vector of the highest interrupting device.

This signal begins the interrupt vector operation. The system I/O controllers determine the highest priority interrupt. Once determined, the appropriate controller places the vector on the LDAL bus.

The interrupt acknowledge signal performs the following functions.

1. Enables the LDAL-DAL buffer, putting the interrupt vector on the DAL bus when PHASE H is asserted.

2. Turns off the control line buffer to the CTI Bus, keeping AS H and all control signals from the CTI Bus.

3. Initiates the interrupt controllers to generate the vector for the highest pending interrupt.

A response in process signal from the interrupt controller (RIP L) asserts a reply signal. This changes PHASE to PHASE-BAR and clocks the vector into the CPU.

5.3.7 Direct Memory Access (DMA)

When a DMA-type device on the CTI Bus requires access to memory to read or write data, it requests a direct memory access (DMA). If a DMA device requests the bus, the CPU gets off the bus and allows the device to become bus master and access memory directly.

If two or more devices require DMA at the same time, an arbiter determines which device receives the grant first. There are two priority schemes in the Professional 350.

Each option controller module has a circuit to transmit its own priority level and monitor the priority of any device currently using the bus. If a low priority device is on the bus and a higher priority device requests DMA, the lower priority one unasserts its DMA request line.

There are three priority levels in the Professional 350. If the requesting devices are at the same priority level, then the one in the lowest slot number wins the decision.

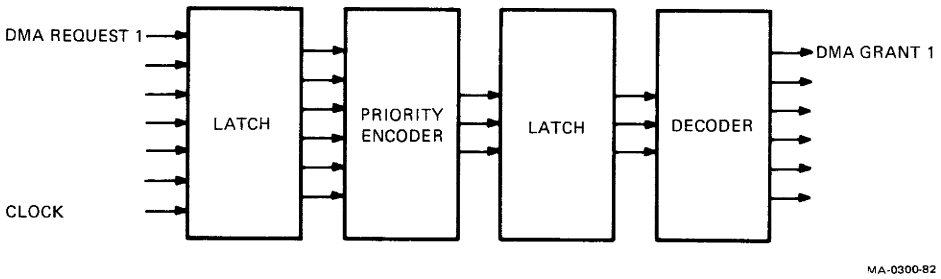


Figure 5-25 DMA Arbitor

5.3.7.1 DMA Detailed Description – Each slot on the CTI Bus has a DMA request line. An option controller module pulls the line low to assert a DMA request. A clock circuit samples the DMA requests and an 8:3 priority encoder drives a latch (Figure 5-25) which holds the winner of the arbitration. A decoder then enables the DMA grant to the requesting module. Once the request is granted, the priority encoder can latch for the next arbitration.

When the device receives the grant, it drops its request and asserts a bus busy (BBUSY) signal. This signal sets up timing circuits that prevent asserting a new DMA grant until the busy signal clears. The DMA arbitor circuit stops the system clock in PHASE time and disables the CPU until DMA is finished. If a second DMA request follows the first, the CPU remains idle.

The DMA arbiter also decides between devices on the bus and CPU bus cycles. If the CPU is using the bus, it prevents a DMA grant until it is finished with the bus.

5.3.8 (Read Only Memory) ROM

The system ROM contains power-up self-test code, configuration and initialization code, and the boot code. Some ROM is in the I/O page and some is in the memory address space. After addressing, the data in ROM is put out on the bus. Attempts to write to ROM result in nonexistent memory traps to location 4.

The power-up self-test is described in Section 5.2.3.4.

The following is the address and data read sequence. Refer to Figure 5-26 for ROM addressing and reading.

1. Addressing ROM

   If ROM is in the memory space, the following occurs.

   a. If A 21:15 are high, at Address Strobe (AS H), the ROM address decoder decodes A 14:12. This asserts ENB ROM H (valid ROM address) and LOCAL MEM L.

   b. ENB ROM H and Data Strobe (DS H) put addressed ROM data on the bus. High byte data is on the DAL bus (DAL 15:08), low byte data is on the LDAL bus (LDAL 07:00).

   c. LOCAL MEM L indicates the CPU is talking to either local ROM or RAM.

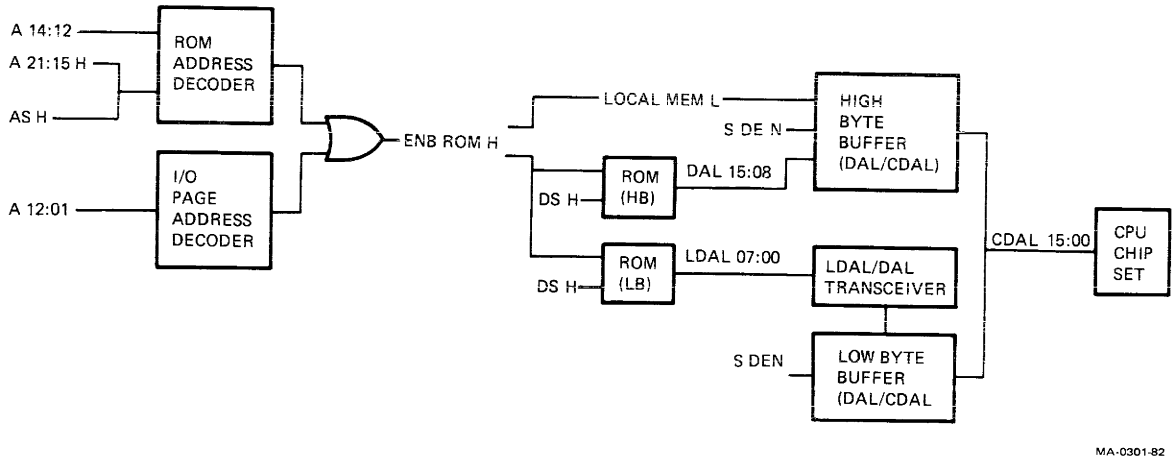


Figure 5-26 ROM Addressing and Reading

2. I/O Page Address Decoder
   If ROM is in the I/O page range, the following occurs.

   a. A 12 and LBSIO are decoded and assert ENB ROM L if the address is a valid ROM address in this range.

3. Reading Data from ROM

   a. High Byte

      (1) At Data Strobe (DS H), the DAL-CDAL buffer passes the data (DAL 15:08) from the DAL to the CDAL bus.

   b. Low Byte

      (1) LDAL 07:00 transfers data from the LDAL to DAL bus at DS H, and since the DAL-CDAL buffer is on at this time, the data (DAL 07:00) passes to the CDAL bus.

   c. Both Bytes

      (1) Data on the CDAL bus is read directly by the CPU chip set.

      (2) ENB ROM H also asserted LOCAL REPLY H five clock cycles later. One cycle after that, it asserts RREPLY 3 L. This ends PHASE time and the data transfer on the DAL bus.

5.3.8.1 ID PROM – Each Professional 300 Series computer module has an ID PROM containing a unique system identifier. When the CPU places an address in this PROM's range (17773600–17773676), the address is decoded, the PROM enabled, and the data asserted on the DAL bus.

5.3.9 Random Access Memory (RAM) on Daughter Modules

This section describes RAM on the Professional 350 system module. RAM is mounted on two daughter modules and in an option slot. Battery backed-up RAM, internal to the battery backed-up clock chip, is discussed in Section 5.3.13.

Each RAM daughterboard consists of 16 (64K × 1) dynamic MOS memory chips which provide capacity for 128 kilobytes of memory. The system can address up to 512 kilobytes per daughterboard slot. Inserting either module in either slot informs the CPU of available address space. Bank 0 is the slot physically farther from the CPU chip set, while bank 1 is closer.

RAM requires support timing circuits. Address and data come to RAM via the DAL bus. The DAL bus is multiplexed for address and data, but RAM requires two separate buses so an address can be held while data is read or loaded. The A Bus accepts address data from the DAL bus and the D bus accepts data, each at its respective time.

Additional memory is installed in the CTI Bus card cage. Memory added in the card cage requires its own support circuitry. The memory option module is a 256 kilobyte module containing 32 64K × 1 dynamic RAMs. A combination of memory option modules can be installed in the system module.

Refresh Cycles

Data in RAM requires periodic refreshes. The system generates a refresh signal every 12.7 μs (refresh clock). The memory chips used here only require a row address strobe for refresh. At the refresh signal, a counter and driver clock each row to refresh data. The refresh signal also enables a row address strobe signal described next. Refresh cycles occur after each instruction fetch or when the refresh clock times out at 12.7 μs. These time outs occur while executing long instructions, during DMA transfers (with no fetching), or when halted into ODT.

Read/Write Cycles

Reading from or writing to RAM requires loading an address into RAM. An address to the RAM chips is 16 or 18 bits wide. Since the RAM chips have only eight or nine address lines, row and column data are entered separately. First, the low bits are loaded as a row address. Then the high bits are loaded as a column address. Row address strobe and column address strobe clock in the row and column addresses.

1. A RAM address multiplexer takes the 16 or 18 address lines from the A Bus and first transfers the low half and then the high half to the MUX bus.

2. Row and column address strobes load the low and high parts of the address from the MUX bus to the RAM chips.

If a DMA device is reading from RAM, it places the RAM address on the bus. This enables the address on the chips and asserts the data on the D Bus. RAM outputs the full 16-bit data word. The device then reads whichever byte(s) it wants.

For a DMA device to write to RAM, it places the RAM address on the bus. This enables the address on the chips. A write signal is necessary. RAM writes may be low byte only, high byte only, or a full 16-bit data word.

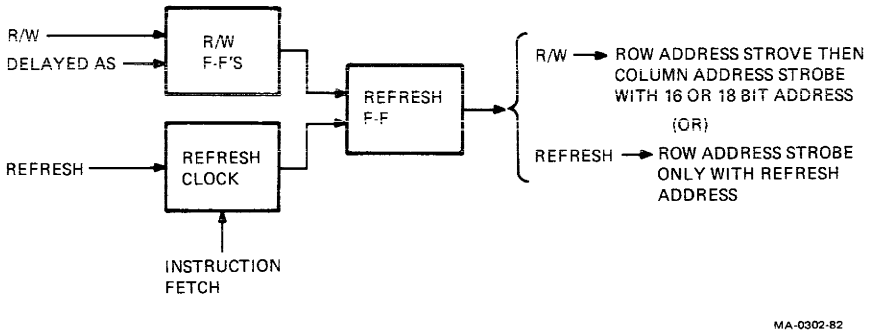


Figure 5-27 Refresh-R/W Arbitration

Refresh Read/Write Arbitration
The system must arbitrate between refresh and read/write (R/W) signals. Arbitration begins when a R/W signal clocks its respective flip-flop (Figure 5-27). Refresh wins the arbitration if the refresh clock gates the refresh flip-flop before delayed address strobe. If the R/W signal and delayed address strobe win, there is a memory cycle. If R/W wins, other circuits are also enabled for data transfer.

5.3.9.1 RAM Timing and Control (Refresh Cycles) – When power is applied to the Professional 350, a one-shot timer asserts a refresh clock signal (Figure 5-27). This signal clocks a flip-flop which generates the refresh signal. The following occurs when refresh is asserted.

1. Clocks an 8-bit binary counter which addresses all RAM address rows
2. Enables an octal tri-state buffer driver to put the refresh address on the MUX bus
3. Asserts row address strobe
4. Disables the D-DAL latch buffer
5. Disables column address strobe to the RAM chips

The following occurs when refresh is not asserted.

1. Starts the one-shot timer to clock the next refresh cycle
2. Allows normal RAM operations

Read/Write Cycles – If the CPU asserts a memory cycle, the MIB bus indicates the kind of cycle to take place. Control circuits set up other logic to carry it through. The signal LBSIO plus two bits on the A bus (A21 and A20) must all be asserted to enable the RAM address decoder. The address decoder asserts the memory row select signal for the RAM daughter module(s). The decoder plus a read or write signal enables circuitry that begins timing used for refresh R/W arbitration. If the CPU wants to read, a whole word is asserted on the D Bus. If it wants a byte, it ignores the undesired byte. When writing, the CPU can signal a write or write-byte. If it signals a write-byte, then it asserts a write-high-byte or write-low-byte. The undesired RAM byte is unaffected. If writing a word, then both write-byte signals are asserted.

Read and write are the inputs to their respective flip-flops. A delayed address strobe clocks each flip-flop. The delay assures the address decode is completed. Read is triggered at address time and there is no need to wait for data strobe. The outputs of either flip-flop combine with timing signals as the entry to refresh R/W arbitration.

If the R/W signal wins the arbitration, it does the following.

1. Blocks the refresh signal
2. Asserts timing signals
3. Allows reading from or writing to RAM

The timing signals perform the following.

1. Control the period of the refresh versus R/W cycle
2. Switch the RAM address multiplexer (Figure 5-26)
3. Enable the column address strobe
4. Clear the refresh and R/W flip-flop to be ready for the next arbitration
5. Enable the D-DAL latch buffer

Reading the RAM uses the D-DAL buffer. This buffer latches if there is a valid RAM request at delayed address strobe. As explained, RAM data is put out on the D Bus directly when addressed.

Writing to memory uses the DAL-D buffer which goes directly to the RAM chips. Writing requires the write command to enable this buffer. The write command also goes out to the CTI Bus.

Refresh R/W Arbitration – When there is no R/W signal, refresh occurs at regular intervals (12.7 μs). When a R/W signal occurs, RAM timing logic arbitrates between the refresh and R/W signals.

The RAM address decoder cannot assert an enable for system RAM until the address is stable on the A Bus. When clocked, the read and write provides an input to the refresh flip-flop. Arbitration begins when the R/W signals compare timing with the self-generated refresh signal (Figure 5-28). If the refresh signal arrives at an R-C timing circuit first, it provides a slower discharge time and a longer period. If R/W arrives at the R-C circuit, then it provides a faster discharge and holds the refresh flip-flop clear until the next arbitration begins.

Whichever signal wins begins a new timing cycle. The cycle enables a buffered delay line to provide pulses for RAM timing logic. The signal that starts this delay line holds itself on until the end of the cycle, ensuring that the cycle is the correct period.

Timing signals for both daughter modules enable the RAM chips. If it is a refresh cycle, the RAM column address strobe is blocked and the row address strobe only is sent to both modules (while the counter refreshes each address row). If it is a R/W cycle, a module select signal enables the RAM row address strobe for the module selected by the RAM address decoder. The timing signals then enable the column address strobe and switch the RAM address multiplexer for the high byte.

The refresh flip-flops clear at the end of the refresh cycle timing chain. This permits a new arbitration.

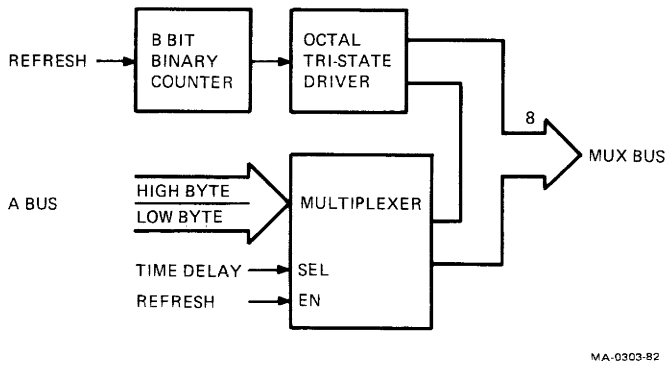


Figure 5-28 RAM Address Multiplexer

5.3.10 Keyboard I/O

The keyboard I/O is a serial port on the system module. It performs asynchronous serial communication to and from the keyboard. The keyboard interface uses a 2661 enhanced programmable communication interface (EPCI). The EPCI is an enhanced USART containing its own I/O buffers and shift registers for controlling asynchronous character protocol. This chip converts parallel data characters from the LDAL bus into serial data for transmission to the keyboard. Simultaneously, it converts serial data from the keyboard into parallel data for CPU processing. The keyboard, discussed in Chapter 6, has its own microprocessor to coordinate keyboard I/O at that level.

The EPCI requires standard EIA RS-423 signal levels and uses appropriate receivers and drivers for input and output. Keyboard connection to the system board is via a 15-pin male D-subminiature connector, J5 (see Section 5.5). The I/O signals to the keyboard are sent and received through the video/keyboard connector, J5. Signals are physically passed through the video monitor by the monitor's keyboard connector. Data to and from the keyboard is via the signals KBD XDATA and KBD RDATA. When a character is transmitted or received, the EPCI generates an interrupt (KBD XIRQ L or KDB RIRQ L). Refer to the sections on interrupts (Sections 5.3.6 and 5.4.6).

The EPCI uses a 5.0688 MHz clock for baud rate generation. The transmit and receive baud rates are programmable by the CPU. The keyboard runs at 4800 baud (the firmware programs the keyboard USART to 4800 baud). Refer to Figure 5-29.

Refer to Section 5.4 for a complete description of the registers and their interpretation.

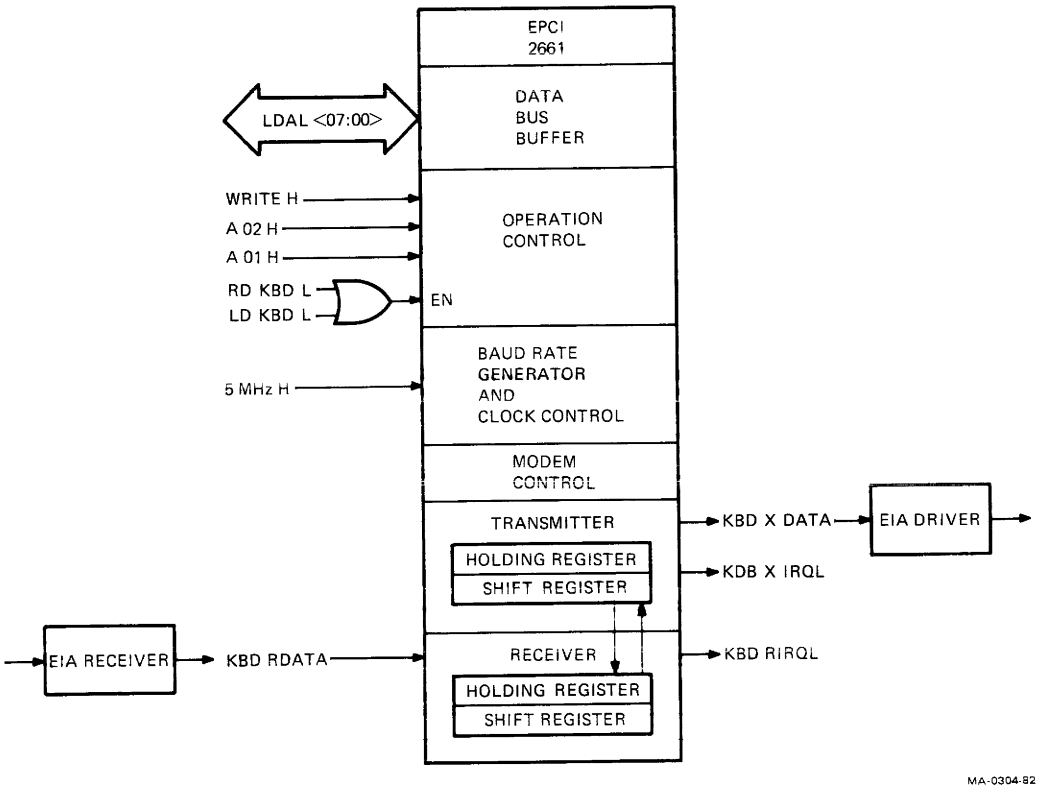


Figure 5-29 Keyboard Interface

5.3.11 Printer I/O

The printer I/O is a port on the system module that performs asynchronous serial communication to and from a serial printer. The printer interface uses a 2661 EPCI. This chip converts parallel data characters from the LDAL bus into serial data for transmission to the printer. Simultaneously, it converts serial data from the printer into parallel data for CPU processing (Figure 5-30).

The EPCI requires standard EIA RS-423 signal levels and uses appropriate receivers and drivers for input and output. Connection to the unit is via a 9-pin male D-subminiature connector, J6 (see Section 5.5).

The EPCI uses a 5.0688 MHz clock for baud rate generation. The transmit and receive baud rates are programmable by the CPU. The firmware programs the printer port to 4800 or 9600 baud depending upon the cable, printer (PN BCC05), or console (PN BCC 08).

A printer must be connected before the EPCI permits data output.

The EPCI generates an interrupt to the CPU when characters are transmitted or received. Refer to Sections 5.3.6 and 5.4.6.

Shorting pins 8 and 9 of the printer connector together tell the CPU a terminal DL console is connected for maintenance. The normal printer cable connector does not short these pins. The short pulls the line low, enabling break detection by the CPU. A received break asserts the CPU halt line (HALT H) to the CPU via the service register. This makes the CPU enter micro-ODT (Octal Debugging Technique) for maintenance and system level troubleshooting.

This micro-ODT function allows the conventional front panel on a processor to be replaced by any terminal generating ASCII code. If a conventional printer cable is used (pins 8 and 9 open), BREAK does not halt the CPU. The cable for this function is the console cable (PN BCC08).

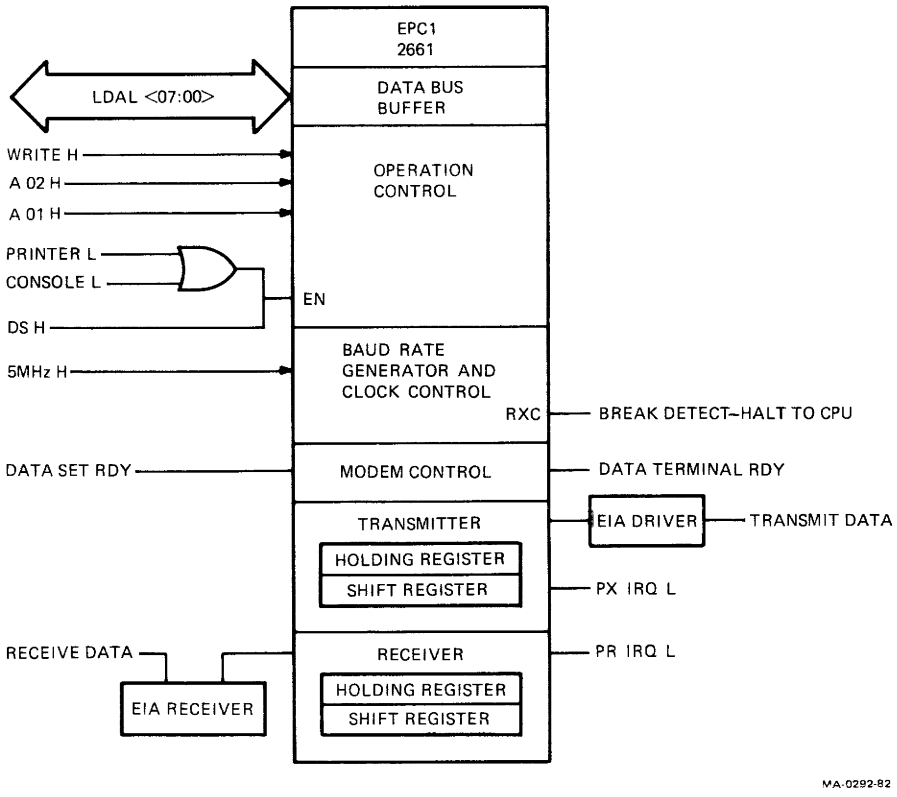


Figure 5-30 Printer Interface

The EPCI is enabled on DS H and received data is placed on the LDAL bus. The CPU then reads the data. Refer to Sections 5.4.14 and 5.4.15 for a description of addressing and register interpretation.

5.3.12 Communication I/O

The system module has a communication port capable of operating with asynchronous and bit or byte synchronous protocols. It uses a 7201 USART containing its own I/O buffers and shift registers. In asynchronous mode, it can run at split programmable baud rates up to 19.2K baud. In synchronous mode, it can run up to 740K baud. The transmitter is double buffered and the receiver is quad buffered. A full set of modem controls is also present for asynchronous communication. All the port signals are EIA RS-423 levels. Connection is made on the rear of the unit via a 25-pin male D-subminiature connector, J7 (see Section 5.5).

The communications port can assert two interrupts.

1. The first can interrupt the CPU if the USART chip requires receiver or transmitter service.

2. The second interrupt can indicate that a state change has occurred on one of four modem control signals.

These four modem control signals are Ring Indicator, Data Set Ready, Clear To Send, and Carrier Detect.

Communication I/O requires support circuits. A baud rate generator selects the clock speed for the USART. Modem controls monitor modem status signals.

- Modem Controls – EIA level buffers receive the modem signals mentioned above. These signals connect directly to the DAL bus through a buffer which is enabled via the I/O page address decoder. An exclusive or circuit compares the modem signals' states clocked in on PHASE time with their status on the previous PHASE time. If any of the states changes, the exclusive or circuit generates an interrupt (see Sections 5.3.6 and 5.4.6).

- Baud Rate Generator – A programmable baud rate generator (BRG) creates the clock signal for the USART. The I/O page address decoder selects the BRG. Section 5.4.13 provides a table of selectable baud rates for programming the BRG. Refer to Figure 5-31. Transmit and receive baud rates for the USART can be selected independently.

- USART – The communications USART is a parallel-to-serial, serial-to-parallel converter. It is programmable to check transmitted and received data integrity. It can generate an interrupt to the interrupt controller chips (see Sections 5.3.6 and 5.4.6).

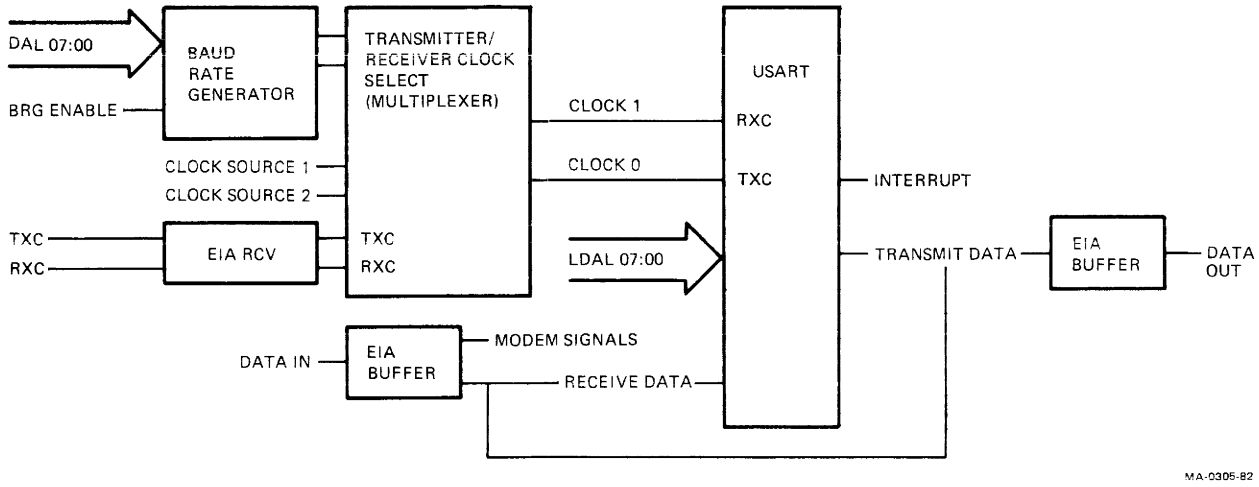


Figure 5-31 Communications Interface

5.3.12.1 Communications I/O Detailed Description – The following paragraphs provide a detailed description of the communications I/O features.

1. Modem Controls – The modem interface uses standard EIA 423 level signals for input and output. Four modem control signals are modem status indicators: Ring Indicator (RI), Data Set Ready (DSR), Clear to Send (CTS), and Carrier Detect (CD). At the beginning of each PHASE period, these signals are latched into a holding buffer. Each signal then provides input to exclusive NOR gates. If there is a change in state from the beginning of one PHASE time to the next, the NOR gates assert an interrupt to the interrupt controller chips. The CPU can read modem signals from the DAL bus by addressing the modem control registers (enabled via the I/O page address decoder).

2. Baud Rate Generator (BRG) – The baud rate generator uses the same 5 MHz clock as the printer EPCI (Figure 5-31).

   It generates clock signals for the USART. Table 5-10 shows the selection scheme for the transmit and receive clocks.

3. USART – The communications USART uses another clock oscillator. The CPU selects transmit and receive baud rate clocks as described above. Transmit data feeds back into the received data line (Figure 5-31) but is ignored except when in maintenance mode. When this happens, received data is ignored until the modem control register is cleared (at power up or by a reset instruction) or written with new data.

5.3.13 Battery Backed-Up Clock and RAM

The following paragraphs describe the battery backed-up clock and RAM.

1. Clock – This system clock maintains date and time even when the system is turned off. The clock is a 146818 CMOS chip. The power off backup uses a rechargeable nickel cadmium (NiCd) battery. The battery connector, J3, is on the system module (Section 5.5). The battery is mounted inside on the rear of the card cage. The clock uses its own 32.768 kHz oscillator as a time base.

2. RAM – The clock chip has 50 bytes of RAM which are also backed up by battery. The battery power maintains data in the chip when system power is turned off.

Table 5-10 Baud Rate Generator TX/RX Clock Selection

Clock Source	Clock
01	Asynchronous; determined by BRG
01	Modem supplies synchronous receive and transmit signals
10	Modem supplies receiver clock; transmit clock source is transmitter stage of BRG
11	Maintenance mode; transmit stage of BRG is the clock for transmit and receive

3. Battery – When the system is turned on, the power supply trickle charges the battery and powers an oscillator for the clock. When turned off, the battery powers the oscillator and clock. Fully charged (power on for 48 continuous hours minimum), the battery maintains clock operation for 10 days minimum if system power is turned off.

5.3.13.1 Clock and RAM Circuit – The clock chip is programmable for date and time functions. Alarm and interrupts also are programmable by writing to the clock's registers. Reads and writes to the clock require assertion of NV L (from the I/O Page Address decoder) and DS L. Reads require the signal WRITE L to be high (not asserted). The clock can assert an interrupt request (CLK IRQ L).

The clock chip power line is filtered to minimize spurious noise from the oscillator.

Addresses and data to and from the clock chip are multiplexed on the AD bus and are low byte only.

Refer to Section 5.4.13 for programming and register descriptions for both the clock and RAM.

5.3.13.2 Battery Charger and Voltage Sensor – The battery charging circuit supplies 10 mA to the battery when the system power is turned on. The charging circuit is a voltage divider that uses +12 Vdc in reference to +5 Vdc. When the system is turned off, the battery powers the oscillator and clock.

The clock/RAM has an internal bit which can be cleared (VRT in Status register 3) if power goes low. When set, this bit indicates clock and RAM data may not be valid. If there is insufficient battery power, the input pin for this circuit is pulled low when the system is first turned on (Figure 5-32). Table 5-11 shows the power sense when power is on and off.

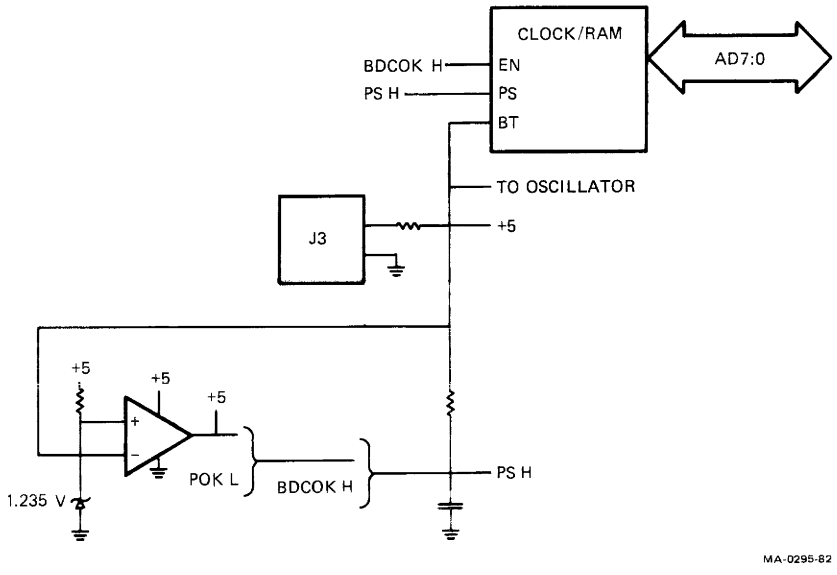


Figure 5-32 Functional Battery Charger and Voltage Sensor

Table 5-11 Power Sense

Battery Installed and Charged
Power Off:
Battery holds PS H.
VRT bit stays set.
Power On:
No change
Battery Not Present or Discharged
Power Off:
PS is low.
VRT bit is clear.
Power On:
RC circuit holds PS low until BDCOK H
(which sets chip enable)
then POK goes L, asserting PS H.

5.4 PROGRAMMING INFORMATION

This section describes the machine level programming for the Professional 350 system module. It contains information about how to access internally programmed functions for the CPU and support devices on the system module. It does not contain information about applications programming in high level languages.

5.4.1 Introduction

Each subsection gives a short description of the device and its function. Some sections provide a brief theory of operation for the devices. Also included are a description of the buffer or register, diagrams showing the bit names and arrangements, and definitions of each bit or groups of bits. Tables are included in the bit descriptions to show the effects of the bit combinations.

The de-bugging subsections provide examples that show how to use maintenance commands.

5.4.2 General Programming Information

The system module contains the CPU and other devices that need instructions to operate. The instructions must be entered at the beginning of each operating session or whenever a change in operating instructions is needed. This section contains the instructions for the CPU and all the supporting devices on the system module.

This section contains two types of programming information: information to change the program and information that tells what is happening. Depending on what is happening, the program might change the operating instructions.

Operating instructions are written to buffers. Information is read from registers. The CPU chip set, interrupt controllers, RAM, system clock, keyboard and printer USARTs, and communications controller all have buffers into which data can be written. They also all have registers which can be read (ROM can only be read).

User programs (in machine language) enter instructions to make the Professional 350 perform as needed. For example, to restructure the interrupt scheme, the priority of the preferred device can be raised. The necessary instructions must be entered to the interrupt controllers using their instruction set. If it is necessary to read the status of certain registers, these can be accessed by addressing the register and reading its current status.

Buffer contents can be entered and registers read via the printer port. This is described in Sections 5.4.14 and 5.4.15. Simple maintenance and diagnostic routines (in machine language) can be run through this port.

Refer to Table 5-8 for address ranges.

5.4.3 Central Processor

The following paragraphs provide information about the central processor.

Processor Chip Description

The central processor is a 2-die 40-pin hybrid integrated circuit. The data chip contains the PDP-11 general registers, the processor status word (PSW), working registers, the arithmetic logic unit (ALU), and conditional branching logic. It performs arithmetic and logical functions, handles all data and address (except relocation) transfers with the external bus, and operates most of the signals used for interchip communication and external system control.

The control chip contains microprogram logic and 552 words of local microprogram storage in PLA and ROM arrays. This chip accesses the appropriate microinstruction in PLA or ROM, sends it along the microinstruction bus (MIB) to other control and MMU chips, and generates the next microinstruction address. The control chip accesses only its local storage. However, additional control chips, like the floating point adapter (FPA), are added externally to provide additional microstorage.

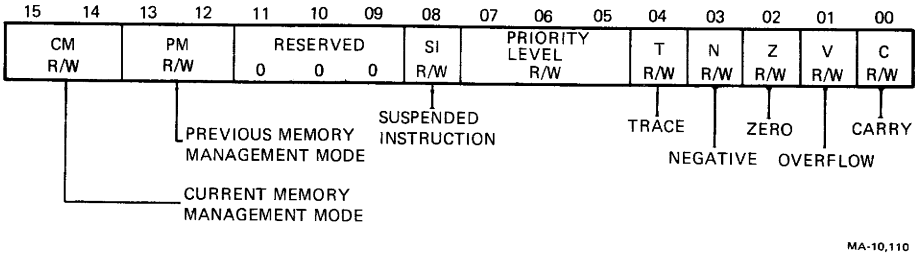
Instruction Set

The instruction set is the standard PDP-11 instruction set plus the Extended Instruction Set (EIS). This provides hardware fixed point arithmetic in double precision mode. The HALT instruction is executed differently in kernel mode and user mode. In user mode, a trap through location 10 occurs. In kernel mode, the CPU halts and enters micro-ODT (Sections 5.4.14 and 5.4.15). The floating point adapter adds additional instructions.

Processor Registers

Addresses	
17777750	Processor maintenance register
(R0)	General register 0
(R1)	General register 1
(R2)	General register 2
(R3)	General register 3
(R4)	General register 4
(R5)	General register 5
(R6 or SP)	General register 6 or stack pointer
(R7 or PC)	General register 7 or program counter
17777776	Processor status word

Processor Status Word



The processor status word (PSW) contains the following information on the current status of the PDP-11.

1. The current processor priority
2. The current and previous operational modes
3. The condition codes describing the results of the last instruction
4. An indicator for detecting the execution of an instruction to be trapped during program debugging
5. An indicator for detecting the presence of a suspended instruction

General Registers 0–7
The eight internal general registers (R0–R7) are used as accumulators and for operand addressing. Access to these registers is via software reference using the appropriate addressing mode or via the $ and R commands in ODT.

Stack Pointer – General register R6 is the hardware stack pointer (SP). This register saves and restores processor status word (PSW) information during hardware traps and interrupts. There are two stack pointer registers: one for kernel mode and one for user mode. For more information, refer to Section 5.4.3.2.

Program Counter – General register R7 is the program counter (PC). It contains the address of the next instruction to be executed. It is used for addressing purpose and not as an accumulator for arithmetic operations.

Processor Maintenance Register – The processor maintenance register is a 16-bit register that identifies the system architecture. It is always read as all 0s. All 0s in bits <7:4> indicate a Professional 300 series architecture product. Writes to the register have no effect but do not cause a nonexistent memory trap.

Processor Traps
Several instructions and conditions cause the processor to trap through vectors to service routines. The following list indicates the processor trap vectors and conditions.

Vectors	Conditions
004	Bus timeout trap or stack overflow trap
010	Illegal and reserved instruction traps
014	Breakpoint and trace trap
020	IOT Instruction trap
024	Power fail trap
030	Emulator trap
034	Trap instruction trap
114	Memory error (parity, ECC, etc.)
244	Floating point error
250	Memory management abort

Bus Timeout – A bus timeout prevents hanging the bus when attempting to address nonexistent memory location. A timeout occurs if the processor does not receive a REPLY signal from a slave device within approximately 6.5 μs from the start of the bus cycle. The timeout causes the bus cycle to terminate and the processor to trap through location 4.

5.4.3.1 Power Fail Trap – A power fail trap allows the processor to power down in an orderly way when ac power is lost. When the ac power loss is detected, the power supply clears the POK signal. The processor then traps through location 24 to allow the execution of a power fail routine.

5.4.3.2 Memory Management – The memory management unit (MMU) provides full 22-bit memory addressing capability of 2 megawords (4 megabytes). It also allows memory protection in a multitasking operating system environment.

A single die in one 40-pin package contains the MMU. Some of the floating point registers are in the MMU chip.

Memory Management Registers

Addresses	
17772300–17772316	Kernel page descriptor registers
17772340–17772356	Kernel page address registers
17777600–17777616	User page descriptor registers
17777640–17777656	User page address registers
–17777572	Status register 0
–17777574	Status register 1
–17777576	Status register 2
–17772516	Status register 3

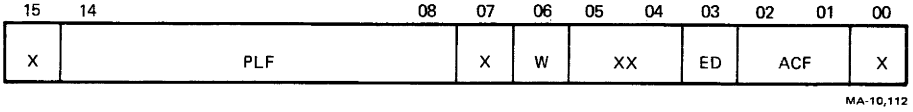
Vector	
250	MMU abort

Page Address and Page Descriptor Registers

Kernel Active Page Registers			User Active Page Registers		
No.	PAR	PDR	No.	PAR	PDR
0	17772340	17772300	0	17777640	17777600
1	17772342	17772302	1	17777642	17777602
2	17772344	17772304	2	17777644	17777604
3	17772346	17772306	3	17777646	17777606
4	17772350	17772310	4	17777650	17777610
5	17772352	17772312	5	17777652	17777612
6	17772354	17772314	6	17777654	17777614
7	17772356	17772316	7	17777656	17777616

Page Address Register (PAR) – The page address register (PAR) contains the 16-bit page address field (PAF) that specifies the base address of the page. The page address register is a relocation constant or a base register containing a base address. Either explanation indicates the basic function of the page address register (PAR) in the relocation scheme.

Page Descriptor Register (PDR) – The page descriptor register (PDR) contains information relative to page expansion, page length, and access control.



Bit 15 — It is not used and is always read as a 0.

Bits 14–08 — PLF – Page Length Field. This 7-bit field specifies the block number which defines the boundary of that page. The block number of the virtual address is compared against the PLF to detect length errors. An error occurs if the block number is higher than the PLF when expanding upwards or if the block number is less than the PLF when expanding downwards.

They are R/W bits.

Bit 07 — It is not used and is always read as a 0.

Bit 06 — W – Write Access Bit. This bit indicates this page was modified (written into) after either the PAR or PDR was loaded (W = 1 is affirmative). The W bit is useful in applications which include disk swapping and memory overlays. It is used to determine which pages were modified and must be saved in their new form and which pages were not modified and can be overlaid. Note that the W bit is reset to 0 when either the PAR or PDR is modified (written into).

It is a read-only bit.

Bits 05–04 — They are not used and are always read as 0s.

Bit 03 — ED – Expansion Direction. This bit specifies in which direction the page expands. If ED = 0, the page expands upwards from block number 0 to include blocks with higher addresses. If ED = 1, the page expands downwards from block number 127 to include blocks with lower addresses. Upward expansion is usually used for program space while downward expansion is used for stack space.

It is a R/W bit.

Bits 02–01 — ACF – Access Control Field. This 2-bit field describes the access rights of this specific page. The access codes or keys specify the way in which a page may be accessed and whether a given access results in an abort of the current operation. A memory reference that causes an abort is not completed, but terminated immediately.

Aborts are caused by attempts to access non-resident pages by page length errors or by access violations, such as attempting to write into a read-only page. Traps are used as an aid in collecting memory management information.

Table 5-12 lists the ACF keys and their functions. The ACF is written into the PDR under program control.

Bit 00 — It is not used and is always read as a 0.

Table 5-12 Access Control Field Keys

ACF	Key	Description	Function
00	0	Non-resident	Aborts any attempt to access this non-resident page
01	2	Resident read-only	Aborts any attempt to write into this page
10	4	(not used)	Aborts all accesses
11	6	Resident read/write	Read or write allowed No trap or abort Read/write bits

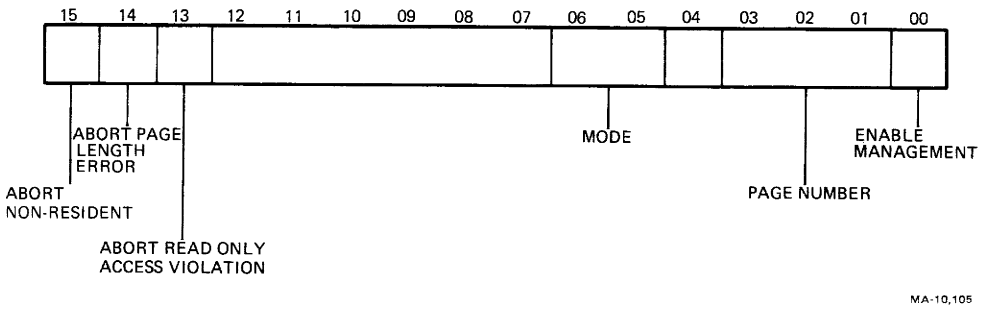
Status Register 0 (SR0)

SR0 contains abort error flags, memory management enable, plus other information needed to recover from an abort or to service a memory management trap. The following paragraphs describe the SR0 format.

Bits 15–13 are the abort flags. Abort bits can be set simultaneously by the same access attempt. They are in priority order; flags to the right are less significant and should be ignored. For example, a nonresident abort service routine ignores page length and access control flags. A page length abort service routine ignores an access control fault.

NOTE

When set (abort conditions), bits 15–13 cause the logic to hold the contents of SR0 bits 1 through 6 and status register SR2. This makes recovery from the abort easier.



Bit 15 — Abort Nonresident – This bit is automatically set by trying to access a page with an access control field (ACF) key equal to 0 or 4, or by enabling relocation with an illegal mode in the PS. When this occurs, the processor traps through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit because of hardware action is useful as a monitor of the MMU status. Setting this bit under program control does not cause a trap to occur. The program should reset this bit to 0 after an abort or trap has occurred to continue monitoring memory management.

It is a read/write bit.

Bit 14 — Abort Page Length – This bit is automatically set by accessing a location in a page with a block number (virtual address bits 12–6) not authorized by the PLF for that page. When this occurs, the processor traps through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit because of hardware action is useful as a monitor of the MMU status. Setting this bit under program control does not cause a trap to occur. The program should reset this bit to 0 after an abort or trap has occurred to continue monitoring memory management.

It is a read/write bit.

Bit 13 — Abort Read Only – This bit is automatically set by writing into a read-only page. When this occurs, the processor traps through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit because of hardware action is useful as a monitor of the MMU status. Setting this bit under program control does not cause a trap to occur. The program should reset this bit to 0 after an abort or trap has occurred to continue monitoring memory management.

It is a read/write bit.

Bits 12–07 — They are not used.

Bits 06–05 — Mode of Operation – These bits indicate the CPU mode (user or kernel) associated with the page causing the abort (kernel = 00, user = 11). They are automatically written at the time of the abort. These bits can also be written under program control. However, only that information which is automatically written in these bits as a result of hardware action is useful as a monitor of the MMU status.

They are read/write bits.

Bit 04 — It is not used.

Bits 03–01 — Page Number – These bits identify the page being accessed when an abort occurs. They are automatically written at the time of the abort. Pages, like blocks, are numbered from 0 upwards. These bits can also be written under program control. However, only that information which is automatically written in these bits as a result of hardware action is useful as a monitor of the MMU status.

They are read/write bits.

Bit 00 — Enable relocation and protection – This bit is the memory management enable bit. It is set and cleared under program control. When it is set to 1, all addresses are relocated and protected by the MMU. When cleared to 0, the MMU is disabled and addresses are neither relocated nor protected.

It is a read/write bit.

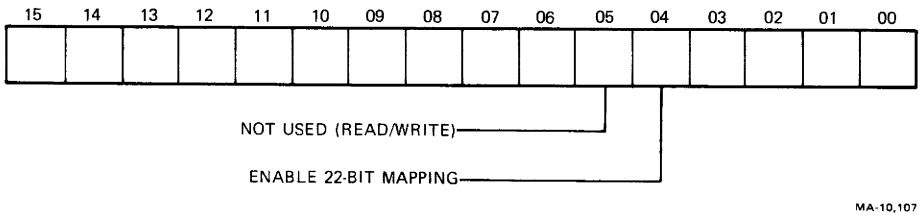
Status Register 1 (SR1)

SR1 is a read-only register which is always read as 0.

Status Register 2 (SR2)

SR2 is loaded with the 16-bit virtual address (VA) at the beginning of each instruction fetch. It is not updated if the instruction fetch fails. SR2 is read-only; a write attempt does not modify its contents. SR2 is the virtual address program counter. On an abort, setting SR0 bit 15, 14, or 13 holds SR2 until the SR0 abort flags are cleared.

Status Register 3 (SR3)



Bits 15–06 They are not used.

Bit 05 Reserved – This bit is a read/write bit that has no effect on system module operation.

It is a read/write bit.

Bit 04 Enable 22-bit mapping – This bit enables or disables the memory management 22-bit mapping. If memory management is not enabled (SR0 bit 0 is clear), this bit is ignored and the 16-bit address is not relocated. If memory management is enabled (SR0 bit 0 is set) and this bit is clear, the computer uses 18-bit mapping. If memory management is enabled and this bit is set, the computer uses 22-bit mapping.

It is a read/write bit.

NOTE

The 22-bit mapping should always be used. If 18-bit mapping is used, address bits <21:18> are always 0s and the I/O page is selected when bits <17:13> are all ones. In 18-bit mode, 12 of the 16 kilobytes of ROM are not accessible (along with any other memory devices above the 18-bit address range).

Bits 03–00 They are not used.

5.4.3.3 Memory Management Relocation – Figure 5-33 shows how the MMU relocates 16-bit virtual addresses into 22-bit physical addresses.

Refer to *Microcomputers and Memories* for a detailed description of the memory relocation process.

5.4.3.4 Default State After Power-Up – At the completion of the power-up self-test, clearing bit 00 in SR0 disables the MMU. Bit 04 in SR 3 is also cleared so 22-bit mapping is not selected.

5.4.3.5 Floating Point Precision – The floating point instruction set (FP11) is contained in the floating point adapter (FPA). Both single and double precision floating point capability are available together with other features including floating-to-integer and integer-to-floating conversion.

The microcode resides in two MOS/LSI chips contained in one 40-pin package (FPA). The FP11 needs the MMU chip and the base MOS/LSI chips because all the floating point accumulators and status registers are in the MMU. Figure 5-34 shows the location of the floating point adapter on the system module.

5.4.4 Computing Terminal Interconnect (CTI) Bus

The CTI Bus backplane is part of the system module. The backplane is designed to accept option modules using a zero insertion force (ZIF) connector. Six option module slots are provided. Figure 5-35 shows the position of the option slots on the system.

Each option slot has a 90-pin connector on the system module. The first 60 pins are used for the general section of the CTI Bus signals. The last 30 pins, 61 through 90, route signals from the option modules to connectors on the rear of the system module. These are referred to as the private section of the bus. An option module that only needs the CTI Bus signals can use a 60-pin ZIF connector. An option module that uses the rear connectors on the system module can use a 90-pin ZIF connector.

Bus signal timing is discussed in Sections 5.3.3 through 5.3.5. The bus signal descriptions and pin locations are in Section 5.6.

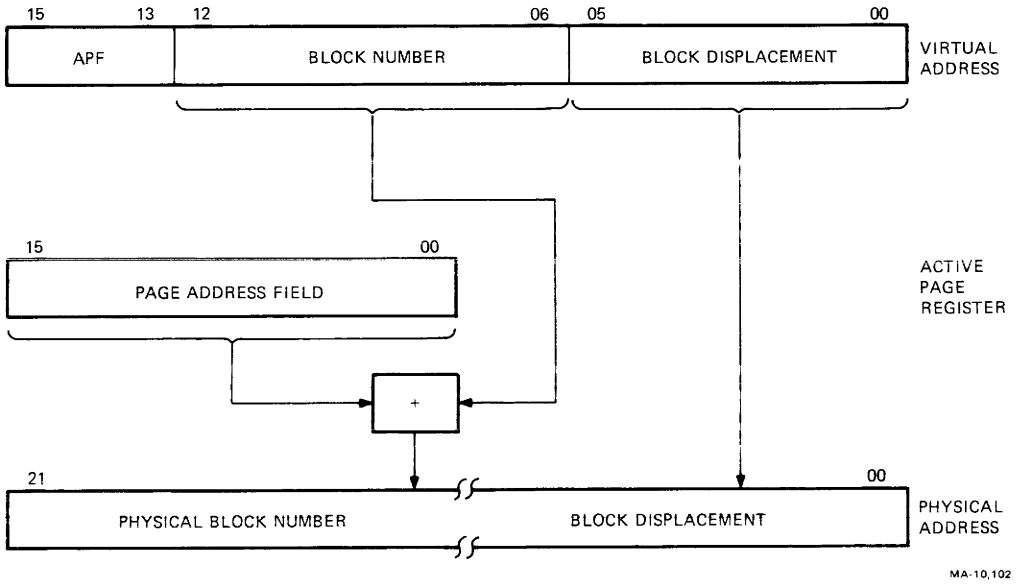


Figure 5-33 Memory Management Relocation

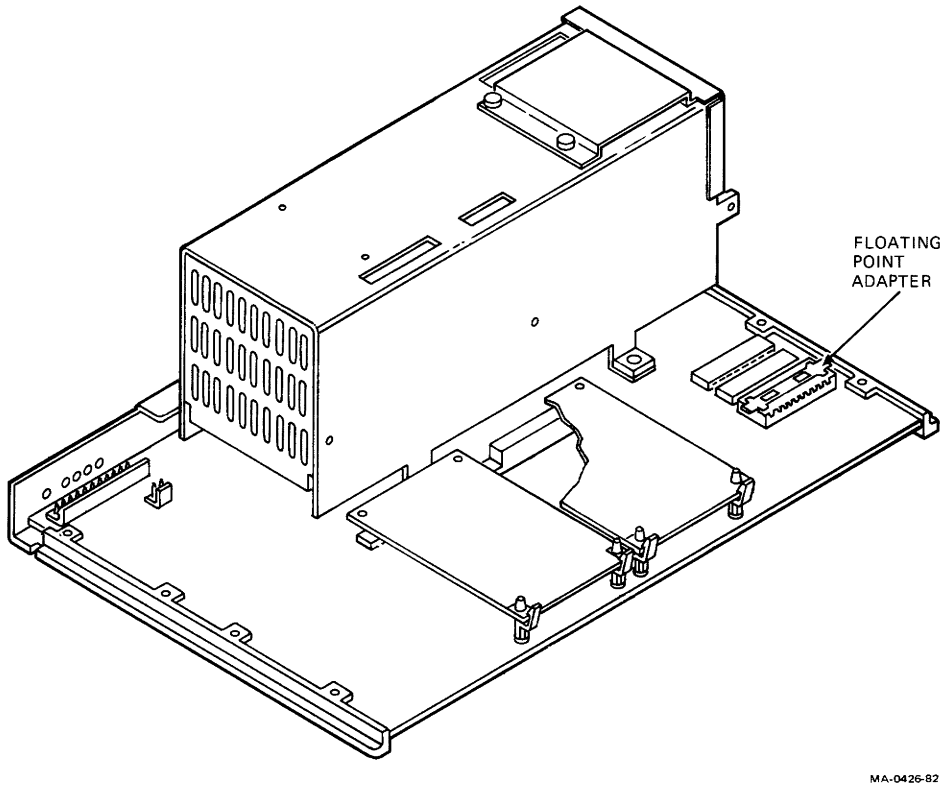


Figure 5-34 Floating Point Adapter Location

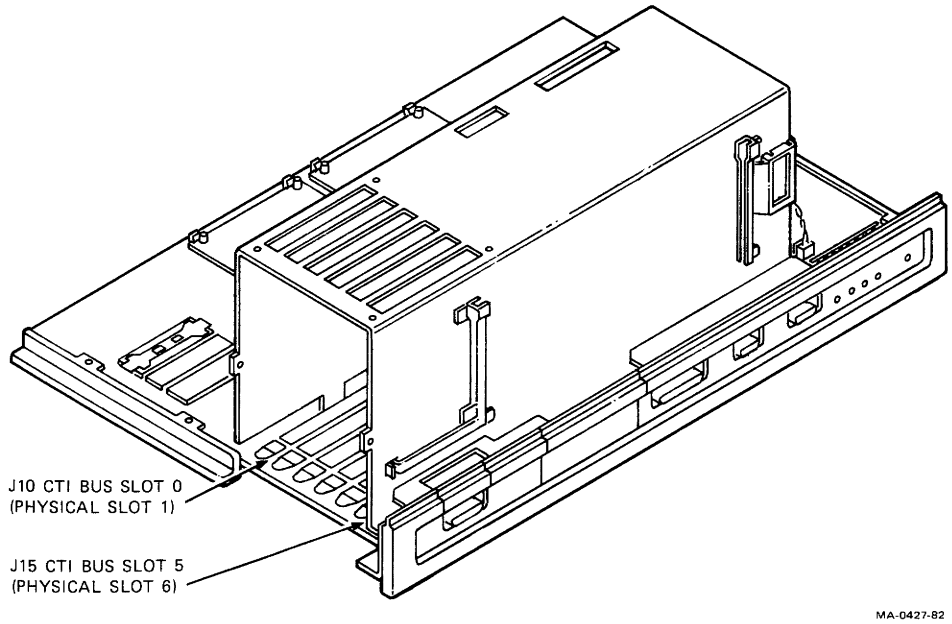


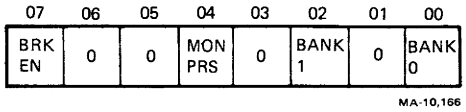
Figure 5-35 CTI Bus Option Slots

5.4.5 System Control and Status Register (SCSR)

Register Operation

Address
17773700 Control and status register

This register uses only the low byte. The high byte is always read as all 0s and writes to the high byte have no effect. The system control and status register provide certain configuration information and allow the selection of certain modes of operation. The bits in the register function are described in the following paragraphs.



Bit 07 BRK EN – Break Enable. This bit enables hardware break detect on the printer port when that port is used with a terminal. Mode register 1 of the printer port must be initialized before this bit is set. When BRK EN is set, hardware break detection is enabled. When cleared, break detection is disabled. If a printer is connected to the port, break detection is disabled regardless of the state of the BRK EN bit. BRK EN is cleared at power up.

It is a R/W bit.

Bits 06–05 They are not used and are always read as 0s.

They are read-only bits.

Bit 04 MON PRS – Monitor Present. This is a status bit to indicate that a video monitor is connected to the video interface. MON PRS asserted indicates a monitor is present and cleared indicates no monitor present.

It is a read-only bit.

Bit 03 512KB1. This is a status bit that indicates the size of the memory module in memory option slot 1. It is clear when the memory module contains 128 Kbytes or when memory option slot 1 is empty. The BANK1 bit indicates if the slot is empty.

It is a read-only bit.

Bit 02 BANK1. This is a status bit that indicates whether a memory module is present in memory option slot 1. It is set when a memory module is present and cleared when no memory module is present.

It is a read-only bit.

Bit 01 — 512KB0. This is a status bit that indicates the size of the memory module in memory option slot 0. It is clear when the memory module contains 128 Kbytes or when memory option slot 0 is empty. The BANK0 bit indicates if the slot is empty.

It is a read-only bit.

Bit 00 — BANK0. This is a status bit that indicates if a memory module is present in memory option slot 0. It is set when a memory module is present and cleared when no memory module is present.

It is a read-only bit.

5.4.5.1 Default State After Power-Up – When the power-up self-test is completed, the firmware sets the break enable bit in the system CS, bit 07. The other bits in the system CSR are read-only and depend upon the memory installed.

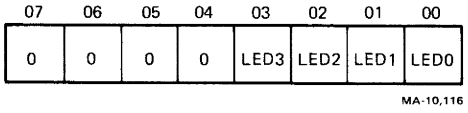
5.4.5.2 Indicator (LED) Display – There are five LEDs on the back of the system module. The green one lights when the DCOK signal from the power supply is asserted. The four red ones are error indicators controlled by the power-up self-test. At power up, all four red LEDs are lit. Table 5-13 indicates the error condition for each LED code.

Indicator (LED) Display Register

Address
17773704 — Indicator (LED) Display Register

The LED display register uses only the low byte. The register is always read as all 0s and writes to the high byte have no effect.

The register controls the state of the four red LEDs on the rear of the unit.



Bits 07–04 — They are not used and are always read as 0s.

Bits 03–00 — LED3–LED0. These bits control the state of the four red LEDs on the rear of the unit. Setting one of these bits causes the corresponding LED to be turned off. Clearing a bit causes the corresponding LED to light. All four bits are cleared (lit) at power up. The bits are always read as 0s.

They are write-only bits.

Table 5-13 Indicator (LED) Error Codes

LED 3	LED 2	LED 1	LED 0	Error Condition
off	off	off	off	None – self-test found no errors
off	off	off	on	Bus slot 0 error detected (physical slot 1)
off	off	on	off	Bus slot 1 error detected (physical slot 2)
off	off	on	on	Bus slot 2 error detected (physical slot 3)
off	on	off	off	Bus slot 3 error detected (physical slot 4)
off	on	off	on	Bus slot 4 error detected (physical slot 5)
off	on	on	off	Bus slot 5 error detected (physical slot 6)
off	on	on	on	Invalid – reserved
on	off	off	off	Invalid – reserved
on	off	off	on	Keyboard failed
on	off	on	off	No boot found
on	off	on	on	Monitor cable not present
on	on	off	off	Memory in slots 0 and 1 both failed
on	on	off	on	Memory in slot 1 failed (high bank)
on	on	on	off	Memory in slot 0 failed (low bank)
on	on	on	on	System module failed*

* All the indicators (LEDs) are lit at power up (lamp test). If they all stay lit, a system module error is indicated.

5.4.5.3 Indicator Display Default State After Power-Up – The power-up self-test firmware uses the display to indicate any detected errors. At the completion of the self-test, the indicator display contains the code for the first error detected. If no errors were found, the LED display turns off.

5.4.6 Interrupt Controllers

Each interrupt controller can handle up to eight interrupt requests. Every interrupt in the system is handled by one of the three interrupt controllers. Table 5-14 shows the interrupts that are handled by each controller. Interrupt controller 0 has a higher priority than controller 1 and controller 1 has a higher priority than controller 2.

Table 5-14 Interrupt Controller Use

Controller	Request Level		Vector*	Interrupt Description
	0	0	–	Not used
	0	1	200	Keyboard receiver interrupt
highest	0	2	204	Keyboard transmitter interrupt
priority	0	3	210	Communication port interrupt
controller	0	4	214	Modem controls change interrupt
	0	5	220	Printer receiver interrupt
	0	6	224	Printer transmitter interrupt
	0	7	230	Clock interrupt
	1	0	300	Option module 0 interrupt request A
	1	1	310	Option module 1 interrupt request A
	1	2	320	Option module 2 interrupt request A
	1	3	330	Option module 3 interrupt request A
	1	4	340	Option module 4 interrupt request A
	1	5	350	Option module 5 interrupt request A
	1	6	–	Not used
	1	7	–	Not used
	2	0	304	Option module 0 interrupt request B
	2	1	314	Option module 1 interrupt request B
lowest	2	2	324	Option module 2 interrupt request B
priority	2	3	334	Option module 3 interrupt request B
controller	2	4	344	Option module 4 interrupt request B
	2	5	354	Option module 5 interrupt request B
	2	6	–	Not used
	2	7	–	Not used

* These vectors are established at power up by the firmware. The firmware programs the interrupt controllers to contain these vectors. It is highly recommended that these vectors not be changed.

Within a given controller, the interrupt requests are received at a request level from 0 to 7. Request level 0 is the highest if the controller is programmed for fixed priority arbitration. The eight request levels have basically equal priority if the controller is programmed for rotating arbitration. See bit 00 of the mode register for more detail. Note that bits within certain internal registers correspond to certain request levels. For example, there is an 8-bit interrupt mask register which enables or disables the eight interrupts. Setting bit 02 in the mask register disables the interrupt at request level 2. Clearing bit 05 in the mask register enables the interrupt at request level 5. In the Professional 350 system, all interrupts occur at request level 4.

Addresses	
17773200	Interrupt controller 0 data register
17773202	Interrupt controller 0 CSR register
17773204	Interrupt controller 1 data register
17773206	Interrupt controller 1 CSR register
17773210	Interrupt controller 2 data register
17773212	Interrupt controller 2 CSR register

All interrupt controller registers use only the low byte. The high bytes are always read as all 0s and writes to high bytes have no effect.

The remainder of this section describes how these interrupt controllers function. Detail at the firmware level is important to understand the full module operation. However, at higher levels, only a part of the information is necessary and the rest may be scanned. Important paragraphs are indicated by a bullet (•).

Each of the interrupt controllers has a set of registers which controls the specific features of operation. These registers are accessed via the CSR and data registers. The following are the set of registers.

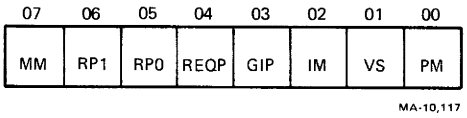
Interrupt Request Register (IRR) – The IRR is 8-bits long and stores the active transitions on the eight interrupt request lines. A bit in the IRR is set when the corresponding interrupt request line makes the appropriate transition. An IRR bit is cleared when the processor acknowledges its interrupt. The processor can clear or set the IRR bits by writing special commands into the controller CSR. The IRR contents may be read from the controller data register by preselecting it in the mode register (see mode register). The IRR bits are cleared by a RESET.

Interrupt Service Register (ISR) – The ISR is 8-bits long and stores the acknowledge status of the IRR bits. When acknowledged, the controller selects the highest priority request pending, clears the associated IRR bit, and sets the associated ISR bit. When the ISR bit is programmed for automatic clearing (see auto clear register), it is cleared at the end of the acknowledge cycle. If auto clear is not selected, the processor must clear the ISR bit by writing the appropriate command into the controller CSR. The ISR contents may be read from the controller data register by preselecting it in the mode register (see mode register). A RESET clears the ISR bits.

Interrupt Mask Register (IMR) – The IMR is 8-bits long and enables or disables each of the individual interrupt requests. Setting an IMR bit disables the corresponding interrupt request, while clearing an IMR bit enables the corresponding request. Only unmasked IRR bits cause a group interrupt. The state of an IMR bit has no effect on the operation of its IRR bit. The processor can clear or set the IMR bits by writing special commands into the controller CSR. The IMR contents may be read from the controller data register by preselecting it in the mode register (see mode register). The processor loads the IMR by writing a PRESELECT IMR command (see command definition in next section) into the controller CSR followed by a write to the data register. A RESET sets all the IMR bits.

Auto Clear Register (ACR) – The ACR is 8-bits long and specifies the automatic clearing option for each ISR bit. When an ACR bit is set, the corresponding ISR bit is automatically cleared at the end of the acknowledge cycle. When an ACR bit is cleared, the corresponding ISR bit is not cleared at the end of the acknowledge cycle. The processor must clear it by writing a command to the controller CSR. The processor loads the ACR by writing a PRESELECT ACR command (see command definition in next section) into the controller CSR followed by a write to the data register. The ACR contents may be read from the controller data register by preselecting it in the mode register (see mode register). A RESET clears all the ACR bits.

Mode Register – The mode register is 8-bits long and controls many of the controller options. It is loaded by writing commands into the controller CSR (see command definitions in next section). The mode register cannot be read. Bits 00, 02, and 07 are available in the controller CSR during read operations. A RESET clears the mode register. The mode register bit functions are as follows.



Bit 07• MM – Master Mask. When set, it enables group interrupts to the processor. When cleared, it disables group interrupts to the processor.

Bit 06–05• RP1–RP0 – Register Preselect. These bits determine which internal register will be read when the processor reads the controller data register. The internal register is selected as follows.

RP1	RP0	Register
0	0	Interrupt service register
0	1	Interrupt mask register
1	0	Interrupt request register
1	1	Auto clear register

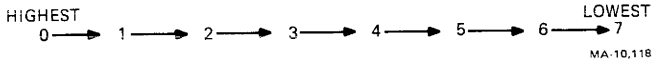
Bit 04 REQP – Interrupt Request Polarity. This bit determines the active transition for setting IRR bits. When set, an IRR bit is set when the corresponding interrupt request line makes a low to high transition. When cleared, a high to low transition on the interrupt request line sets the IRR bit. This bit should always be cleared because the system hardware provides high to low transitions for all interrupts to all three controllers.

Bit 03 GIP – Group Interrupt Polarity. This bit determines the polarity of the group interrupt output to the processor. When set, the group interrupt output is asserted high. When cleared, the group interrupt output is asserted low. This bit should always be cleared because the system hardware recognizes active low group interrupts from all three controllers.

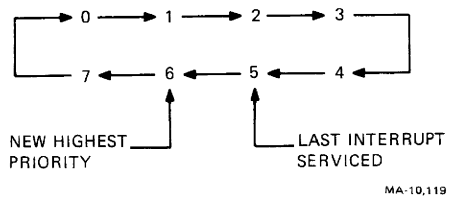
Bit 02 IM – Interrupt Mode. This bit determines whether the controller is operating in interrupt mode or polled mode. When IM is cleared, interrupt mode is selected and the group interrupt output functions normally. When IM is set, the polled mode is selected and the group interrupt output is disabled so the controller does not interrupt the processor. In polled mode, the processor can read the controller CSR to see if any interrupt requests are pending. See section on status register.

Bit 01 VS – Vector Selection. This bit determines whether the controller generates a common vector for all the interrupt requests or an individual vector for each request. The response memory contains eight vectors, one for each request level (see response memory section). When VS is cleared, each interrupt level is associated with its own unique vector in the response memory. When VS is set, all interrupt levels are associated with the vector in the request level 0 response memory location. In this mode, the controller generates the same vector regardless of the interrupt request being acknowledged.

Bit 00 PM – Priority Mode. This bit determines whether a fixed priority or rotating priority selects the highest pending interrupt request. When cleared, fixed priority is selected. In fixed priority mode, interrupt request line 0 is always the highest level and request line 7 is always the lowest level.



When PM is set, rotating priority is selected. In rotating mode, a circular chain determines the priorities.



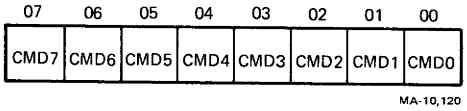
The last interrupt level serviced becomes the lowest priority in the circular chain.

Response Memory – The response memory stores the vectors for each of the eight interrupt requests. The response memory contains eight bytes, one for each vector. The controller, using the response memory, determines which vector to generate in response to a processor interrupt acknowledge. The processor loads the response memory by writing a PRESELECT RESPONSE MEMORY command (see command definition in next section) into the controller CSR followed by a write to the data register. The response memory is not effected by a RESET.

All three interrupt controllers program in the same way. The programming and data transfers are all done with two addressable registers: the data register and the CSR register. These two registers are described in the following paragraphs.

5.4.6.1 Control/Status Register (CSR) – The CSR operates as a command register on writes and as a status register on reads. Commands are written into the CSR to select specific controller operation. The CSR can be read to determine specific controller status.

Command Register (CSR – write operations)



Bits 07–00• CMD7–CMD0 – Command. These bits determine the command to the controller. The available commands are given in the following paragraphs.

They are write-only bits.

The following commands are available.

- RESET – 0 0 0 0 0 0 0 0
  The reset command establishes a known state in the controller. The response memory and byte count registers are not effected. The interrupt mask register is set to all ones. The interrupt request register, interrupt service register, auto clear register, and the mode register are cleared to all 0s.

- CLEAR IRR AND IMR – 0 0 0 1 0 X X X
  All bits in the interrupt request register and the interrupt mask register are cleared.

- CLEAR SINGLE IRR AND IMR BIT – 0 0 0 1 1 B2 B1 B0

  The bit specified by B2–B0 is cleared in both the interrupt request register and the interrupt mask register.

- CLEAR IMR – 0 0 1 0 0 X X X
  The interrupt mask register is cleared to all 0s.

- CLEAR SINGLE IMR BIT – 0 0 1 0 1 B2 B1 B0
  The bit specified by B2-B0 is cleared in the interrupt mask register.

- SET IMR – 0 0 1 1 0 X X X
  The interrupt mask register is set to all ones.

- SET SINGLE IMR BIT – 0 0 1 1 1 B2 B1 B0
  The bit specified by B2-B0 is set in the interrupt mask register.

- CLEAR IRR – 0 1 0 0 0 X X X
  The interrupt request register is cleared to all 0s.

- CLEAR SINGLE IRR BIT – 0 1 0 0 1 B2 B1 B0
  The bit specified by B2-B0 is cleared in the interrupt request register.

SET IRR - 0 1 0 1 0 X X X
The interrupt request register is set to all ones.

SET SINGLE IRR BIT - 0 1 0 1 1 B2 B1 B0
The bit specified by B2-B0 is set in the interrupt request register.

CLEAR HIGHEST PRIORITY ISR BIT - 0 1 1 0 X X X X
The highest priority bit in the interrupt service register is cleared.

CLEAR ISR - 0 1 1 1 0 X X X
The interrupt service register is cleared to all 0s.

CLEAR SINGLE ISR BIT - 0 1 1 1 1 B2 B1 B0
The bit specified by B2-B0 is cleared in the interrupt service register.

LOAD MODE BITS M0 THRU M4 - 1 0 0 M4 M3 M2 M1 M0
The five low order bits of the command are transferred to the five low order bits of the mode register.

CONTROL MODE BITS M5 THRU M7 - 1 0 1 0 M6 M5 N1 N0
The M5 and M6 bits of the command are transferred to bits 05 and 06 of the mode register. The N0 and N1 bits of the command control bit 07 of the mode register are as follows.

N1	**N0**	
0	0	No change to bit 07 in mode register
0	1	Set bit 07 in mode register
1	0	Clear bit 07 in mode register
1	1	Illegal

PRESELECT IMR FOR WRITING - 1 0 1 1 X X X X
Following this command, all write operations to the controller data register load the data into the interrupt mask register. This condition continues until a different preselect command is entered.

PRESELECT ACR FOR WRITING - 1 1 0 0 X X X X
Following this command, all write operations to the controller data register load the data into the auto clear register. This condition continues until a different preselect command is entered.

PRESELECT RESPONSE MEMORY FOR WRITING - 1 1 1 0 0 L2 L1 L0
Following this command, all write operations to the controller data register load the data into a response memory location. L2 through L0 specify which interrupt request level response memory location is loaded as follows.

L2	**L1**	**L0**	**Level**
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

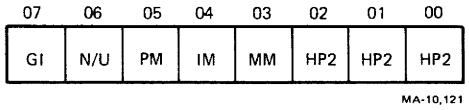
This condition continues until a different preselect command is entered.

NOTE

For the above commands that use B2-B0, the bit specified is as follows.

B2	B1	B0	Bit	
0	0	0	0	LSB
0	0	1	1	
0	1	0	2	
0	1	1	3	
1	0	0	4	
1	0	1	5	
1	1	0	6	
1	1	1	7	MSB

Status Register (CSR – read operations)



Bit 07 GI – Group Interrupt. When set, it indicates that no unmasked bits are set in the interrupt request register. When cleared, it indicates that at least one unmasked bit is set in the interrupt request register. This bit is valid even when polled mode operation is selected.

It is a read-only bit.

Bit 06 N/U – It is not used.

It is a read-only bit.

Bit 05 PM – Priority Mode. PM indicates the state of mode register bit 00. When cleared, it indicates fixed priority operation. When set, it indicates rotating priority operation.

It is a read-only bit.

Bit 04 IM – Interrupt Mode. IM indicates the state of mode register bit 02. When cleared, it indicates that interrupt mode is selected. When set, it indicates that polled mode is selected.

It is a read-only bit.

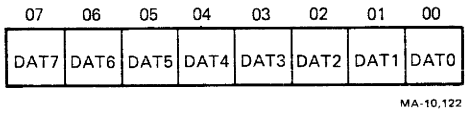
Bit 03 MM – Master Mask. MM indicates the state of mode register bit 07. When cleared, it indicates that the controller is disarmed and will not generate a group interrupt to the processor. When set, the controller is armed and group interrupts to the processor can occur.

It is a read-only bit.

Bits 02–00 HP2–HP0 – Highest Pending Interrupt. These bits indicate the highest unmasked request level bit that is set in the interrupt request register. These bits should only be considered valid when the GI bit is cleared. This indicates that at least one unmasked interrupt request is present. The highest pending interrupt is determined by the bits set in the interrupt request register and the priority mode.

They are read-only bits.

5.4.6.2 Data Register



Bits 07–00• DAT7–DAT0 – Data. During write operations, the data in this register is transfered to the internal register specified by the last PRESELECT command. The data can be transferred to the interrupt mask register, the auto clear register, or the response memory. During read operations, the contents of one of the internal registers is transferred to the data register. The internal register transferred is determined by the preselect bits in the mode register (bits 06 and 05). The interrupt request register, interrupt service register, interrupt mask register, or the auto clear register may be preselected.

They are read/write bits.

5.4.6.3 Interrupt Controller Default State After Power-Up – The three interrupt controller chips are initialized by the firmware at power up. The state of each controller is programmed as follows.

1. Interrupt Controller 0

   IRR = 000 (interrupt request register)
   IMR = 377 (interrupt mask register)
   ACR = 377 (auto-clear register)

   Vector 0 = 234
   Vector 1 = 200
   Vector 2 = 204
   Vector 3 = 210 (response memory)
   Vector 4 = 214
   Vector 5 = 220
   Vector 6 = 224
   Vector 7 = 230

   IMR preselected for reads from data register.
   IMR preselected for writes to data register.
   Fixed priority mode selected.
   Master mask bit set (enabled).

2. Interrupt Controller 1

   IRR = 000 (interrupt request register)
   IMR = 377 (interrupt mask register)
   ACR = 377 (auto-clear register)

   Vector 0 = 300
   Vector 1 = 310
   Vector 2 = 320
   Vector 3 = 330 (response memory)
   Vector 4 = 340
   Vector 5 = 350
   Vector 6 = 360
   Vector 7 = 370

   IMR preselected for reads from data register.
   IMR preselected for writes to data register.
   Rotating priority mode selected.
   Master mask bit set (enabled).

3. Interrupt Controller 2

IRR = 000 (interrupt request register)
IMR = 377 (interrupt mask register)
ACR = 377 (auto-clear register)

Vector 0 = 304
Vector 1 = 314
Vector 2 = 324
Vector 3 = 334 (response memory)
Vector 4 = 344
Vector 5 = 354
Vector 6 = 364
Vector 7 = 374

IMR preselected for reads from data register.
IMR preselected for writes to data register.
Rotating priority mode selected.
Master mask bit set (enabled).

5.4.7 Direct Memory Access (DMA)

The bus and the system module permit direct memory access by the option modules. A DMA device requests the bus from the CPU by asserting its DMA request line, DMR n L. The DMA device becomes the bus master when it receives a grant from the CPU on its DMA grant line, DMG n L. The DMA devices and the system module each perform part of the DMA arbitration. DMA devices monitor the bus DMA priority lines, BP 0 L and BP 1 L, and only request the bus if they are at the current DMA priority level or higher. The system module arbitrates between the DMA devices that are requesting the bus and the CPU. DMA devices always have priority over the CPU and are granted the bus when the processor completes any bus cycle already in progress. When multiple DMA devices at a specific DMA priority level request the bus at the same time, the arbitor grants the bus to the one in the lowest numbered slot, for example, slot 0 is selected before slot 3. If a DMA device does not assert the BUS BUSY signal in response to its grant within the permitted time (see Section 5.6), the system module removes the grant and continues.

All the signals are bused through all six slots with the exception of six signals. The six bidirectional non-bused signals provide slot dependent signals to the system module for handling address decoding, interrupts, and DMA. These signals are as follows.

OPRES n L	Option present indicator
SS n L	Slot select from address decoder
IRQA n L	Interrupt request A from option
IRQB n L	Interrupt request B from option
DMR n L	DMA request from option
DMG n L	DMA grant from arbiter

where n = slot number (0–5)

5.4.7.1 Option Module Addresses – Each option module is allocated 128 bytes in the I/O page. The system module decodes the addresses and asserts a slot select (SS) to the appropriate option module if an option module address is detected. Table 5-15 shows the byte addresses for each option module.

NOTE

DMA devices may address the option modules. In this condition, the system module decodes the address output by the DMA device and asserts a slot select to the appropriate option module if an option module address is detected.

5.4.7.2 Option Module Vectors – Each option module has two interrupt request lines so each slot needs two vectors. Table 5-16 shows the vectors for the option module interrupts.

All interrupt vectors are soft because they can be programmed to any 8-bit number in the interrupt controller chips (see Section 5.4.6). However, the vectors given are established at power up by the firmware. It is highly recommended that the vectors not be changed.

Table 5-15 Option Slot Addresses

Slot	I/O Page Addresses
0	17774000-17774177
1	17774200-17774377
2	17774400-17774577
3	17774600-17774777
4	17775000-17775177
5	17775200-17775377

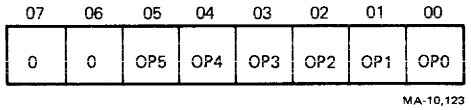
Table 5-16 Option Slot Vectors

Slot	Interrupt Request Vector A	Vector B
0	300	304
1	310	314
2	320	324
3	330	334
4	340	344
5	350	354

5.4.7.3 Option Module Present Register (OMPR) –

Address
17773702 data buffer

The option module present register indicates which of the six option module slots contains a module. It is a read only register which uses only the low byte. The high byte is read as all 0s and all writes to the register have no effect.



Bits 07–06 They are not used and are always read as 0s.

They are read-only bits.

Bits 05–00 OP5–OP0 – Option Present. A one in an OP bit indicates that a module is present in the corresponding option module slot. For example, if OP1 is set, a module is present in option module slot 1. A 0 in an OP bit indicates no module is present in the corresponding slot.

They are read-only bits.

5.4.8 ROM

The system module contains 16 kilobytes of ROM. It contains the power-up self-test code, configuration and initialization code, and the boot code. Table 5-16 shows that some of the ROM is in the I/O page and some is in the memory address space. Any attempt to write to the ROM locations results in a nonexistent memory trap to location 4.

Refer to Section 5.2.3.4 for a description of the system power-up self-test.

5.4.8.1 ID PROM – Each system module board contains a PROM with a unique 32-byte ID.

Addresses
17773600–17773676 32 bytes PROM

All 32 word locations use only the low byte. The high bytes are always read as all 0s. Any attempt to write to the ID PROM locations results in a non-existent memory trap to location 4.

The ID code is a 12-BCD digit (6-byte) random number. The ID PROM should be blasted with the ID as shown in Table 5-17.

Table 5-17 ROM Address Space

Address	Size	Location
17730000–17757777	12 kilobytes	memory space
17760000–17767777	4 kilobytes	I/O page

OCTAL PROM ADDRESS	PROM CONTENTS	22-BIT SYSTEM ADDRESS
00	RANDOM ID BYTE 1	17773600
01	RANDOM ID BYTE 2	17773602
02	RANDOM ID BYTE 3	17773604
03	RANDOM ID BYTE 4	17773606
04	RANDOM ID BYTE 5	17773610
05	RANDOM ID BYTE 6	17773612
06	ERROR CHK BYTE 1*	17773614
07	ERROR CHK BYTE 2*	17773616
10	RANDOM ID BYTE 1	17773620
11	RANDOM ID BYTE 2	17773622
12	RANDOM ID BYTE 3	17773624
13	RANDOM ID BYTE 4	17773626
14	RANDOM ID BYTE 5	17773630
15	RANDOM ID BYTE 6	17773632
16	ERROR CHK BYTE 1*	17773634
17	ERROR CHK BYTE 2*	17773636
20	RANDOM ID BYTE 1	17773640
21	RANDOM ID BYTE 2	17773642
22	RANDOM ID BYTE 3	17773644
23	RANDOM ID BYTE 4	17773646
24	RANDOM ID BYTE 5	17773650
25	RANDOM ID BYTE 6	17773652
26	ERROR CHK BYTE 1*	17773654
27	ERROR CHK BYTE 2*	17773656
30	00000000	17773660
31	11111111	17773662
32	01010101	17773664
33	10101010	17773666
34	11111111	17773670
35	00000000	17773672
36	ERROR CHK BYTE 3†	17773674
37	ERROR CHK BYTE 4†	17773676

* CHECK BYTES 1 AND 2 FORM A WORD CHECK ON THE PREVIOUS 6 BYTES

† CHECK BYTES 3 AND 4 FORM A WORD CHECK ON THE ENTIRE PROM

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5.4.9 RAM

The module contains support circuitry for two memory option modules. There are two 40-pin connectors on the system module to accept the memory modules. Figure 5-36 shows the position of the memory option modules. Refer to Table 5-22 for the memory connects pinning.

Additional memory is installed in the CTI Bus card cage. Memory added in the card cage has its own support circuitry. The memory option module is a 256 kilobyte module containing 16 64K × 1 dynamic RAMs. A combination of memory option modules can be installed in the system module. The following table shows the memory addressing for each combination of daughter modules.

When both slots contain memory boards, the memory in slot 0 always starts at address 00000000 and the memory in slot 1 starts where the first one ends (Table 5-18).

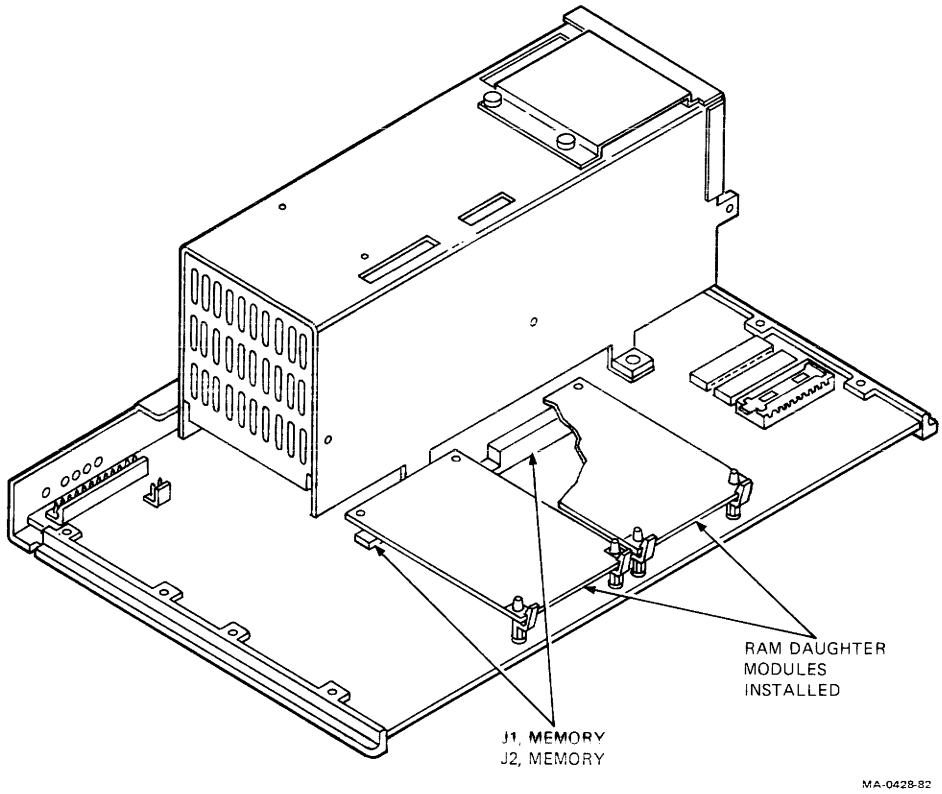


Figure 5-36 Memory Option Sets

Table 5-18 Memory Configurations

Slot 0	Slot 1	Memory	Address
128 kilobytes	—	128 kilobytes	00000000–00377777
—	128 kilobytes	128 kilobytes	00000000–00377777
128 kilobytes	128 kilobytes	256 kilobytes	00000000–00777777
512 kilobytes	—	512 kilobytes	00000000–01777777
—	512 kilobytes	512 kilobytes	00000000–01777777
512 kilobytes	128 kilobytes	640 kilobytes	00000000–02377777
128 kilobytes	512 kilobytes	640 kilobytes	00000000–02377777
512 kilobytes	512 kilobytes	1024 kilobytes	00000000–03777777

The system control and status register (at 17773700) can be read to determine the memory configuration. Bits 03–00 should be interpreted as follows.

Bit	State	Meaning
00	0	No memory module present in memory slot 0.
00	1	Memory slot 0 contains a memory module.
01	0	The memory module in slot 0 is 128 kilobytes.
01	1	The memory module in slot 0 is 512 kilobytes.
02	0	No memory module present in memory slot 1.
02	1	Memory slot 1 contains a memory module.
03	0	The memory module in slot 1 is 128 kilobytes.
03	1	The memory module in slot 1 is 512 kilobytes.

The system module has circuits for address decoding and multiplexing, for timing, and for cycle-stealing refresh.

5.4.10 Keyboard

There is a serial keyboard port on the system module. It can perform asynchronous serial communications at programmable baud rates up to 19.2 kilobaud. The port uses EIA RS-423 signal levels and connection is made on the rear of the unit via a 15-pin male D-subminiature connector, J5. Section 5.6 shows the pinning of J5 on the system module.

This port is included primarily to communicate with the Professional 300 series keyboard. However, it is a general serial port that can be used to communicate with any serial device. The mode of operation is completely programmable as described in the following paragraphs. When using the port with the Professional 300 series keyboard, the mode must be set to the following.

1. 8-bit character length
2. No parity
3. One stop bit
4. 4800 baud clock rate

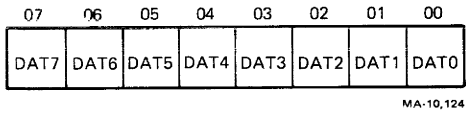
5.4.10.1 Keyboard Interface

Addresses	
17773500	Data buffer register
17773502	Status register
17773504	Mode registers
17773506	Command register

Vectors	
200	Receiver
204	Transmitter

All the keyboard port registers use only the low byte. The high bytes are always read as all 0s and writes to high bytes have no effects. This port is not a standard DL type interface.

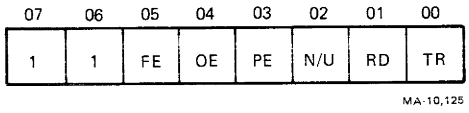
Data Buffer Register (DBUF)



Bits 07–00 DAT7–DAT0 – Data. On read operations, this register operates as the receiver holding register and contains the last received character. The character is right justified if the character length is less than eight bits. On write operations, this register serves as the transmitter holding register and should be loaded with the next character to be transmitted.

They are read/write bits.

Status Register (STAT)



Bits 07–06 They are not used and are always read as 1s.

They are read-only bits.

Bit 05 FE – Framing Error. When set, it indicates that the received character was not framed by the programmed number of stop bits. If the received character is all 0s and FE is set, a break condition was detected. When cleared, FE indicates that the received character was correctly framed. FE is cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register).

It is a read-only bit.

Bit 04 OE – Overrun Error. When set, it indicates that the previous character loaded into the receiver holding register was not read by the processor by the time that a new received character was loaded into it. When cleared, it indicates that no overrun condition occurred. OE is cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register).

It is a read-only bit.

Bit 03 PE – Parity Error. When set, it indicates that the received character had a parity error. When cleared, it indicates that no parity error was detected. This bit only functions when parity is enabled (see section on mode register). PE is cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register).

It is a read-only bit.

Bit 02 N/U – It is not used.

It is a read-only bit.

Bit 01 RD – Receiver Done. When set, it indicates that a character was received and loaded into the receiver holding register for the processor to read. When cleared, it indicates that no new character was loaded into the receiver holding register. RD is cleared by reading the receiver holding register or by disabling the receiver in the command register (see section on command register). RD is not set when characters are received if remote loopback mode is enabled in the command register (see section on command register).

It is a read-only bit.

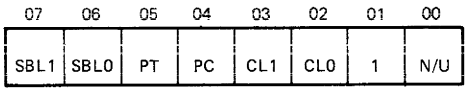
Bit 00 TR – Transmitter Ready. TR is only valid when the transmitter is enabled in the command register (see section on command register). When TR is cleared, it indicates that the transmitter holding register is not ready to receive another character for transmission from the processor. When set, it indicates that the processor may load the next character for transmission into the transmitter holding register. TR is cleared when operating in auto echo or remote loopback modes (see section on command register).

It is a read-only bit.

Mode Registers (MR1 AND MR2)

There are two mode registers that select the operating mode of the keyboard port. Both registers reside at the same address. Operations (read or write) to a mode register cause an internal pointer to point to the other mode register for the next operation. Reading the command register always causes the internal pointer to point to mode register 1. Both mode registers are cleared when system power is turned on. The processor has to initialize both registers to the specified mode of operation. The two mode registers are in the following paragraphs.

Mode Register 1 (MR1)



Bits 07–06 SBL1–SBL0 – Stop Bit Length. These bits select character framing of 1, 1.5, or 2 stop bits for both the transmitter and the receiver. The stop bits are selected as follows.

SBL1	SBL0	Stop	Bit Length
0	0	0	Invalid
0	1	1	Stop bit
1	0	1.5	Stop bits
1	1	2	Stop bits

They are read/write bits.

Bit 05 PT – Parity Type. When set, PT selects even parity. When cleared, PT selects odd parity. Parity type is the same for the transmitter and the receiver. This bit has no effect if parity is not enabled (see PC bit).

It is a read/write bit.

Bit 04 PC – Parity Control. When cleared, parity is disabled for the transmitter and the receiver. When set, the transmitter adds a parity bit to the transmitted character and the receiver performs a parity check on incoming characters. The PT bit selects odd or even parity.

It is a read/write bit.

Bits 03–02 CL1–CL0 – Character Length. These bits select the number of data bits per character for the transmitter and the receiver. The character length does not include the parity bit (if any), the start bit, or the stop bits. Character length is selected as follows.

CL1	CL0	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

They are read/write bits.

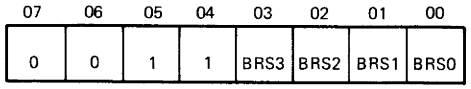
Bit 01 1. – This bit must always be set to a one for correct operation. When the system power is turned on, this bit is cleared. The processor must set it to a 1 before using the keyboard port.

It is a read/write bit.

Bit 00 N/U – It is not used.

It is a read/write bit.

Mode Register 2 (MR2)



Bits 07–04 0011 – These bits must always be programmed to 0011 for correct operation. When the system power is turned on, these bits are cleared. The processor must program them before using the keyboard port.

They are read/write bits.

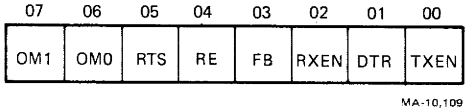
Bits 03–00 BRS3–BRS0 – Baud Rate Select. These bits determine the frequency of the internal baud rate generator. The frequency is 16 times the selected baud rate. These bits select the clock for both the transmitter and receiver. The accuracy of the input frequency to the baud rate generator is ±0.01%. The baud rate is selected as follows.

BRS3	BRS2	BRS1	BRS0	Baud Rate	Baud Rate Generator Percent Error
0	0	0	0	50	–
0	0	0	1	75	–
0	0	1	0	110	–
0	0	1	1	134.5	+0.016
0	1	0	0	150	–
0	1	0	1	300	–
0	1	1	0	600	–
0	1	1	1	1200	–
1	0	0	0	1800	–
1	0	0	1	2000	+0.253
1	0	1	0	2400	–
1	0	1	1	3600	–
1	1	0	0	4800	–
1	1	0	1	7200	–
1	1	1	0	9600	–
1	1	1	1	19200	+3.125

They are read/write bits.

Command Register (CMD)

The command register also controls the keyboard port operator. The command register is cleared when system power is turned on. The processor has to initialize the register to the specified mode of operation. The command register is described in the following paragraphs.



Bits 07–06 OM1–OM0 – Operating Mode. These bits select the operating mode of the port as follows.

OM1	OM0	Operating Mode
0	0	Normal operation
0	1	Automatic echo mode
1	0	Local loopback
1	1	Remote loopback

These modes are described in the following paragraphs.

Normal – The transmitter and receiver operate independently according to the mode and status registers.

Automatic Echo – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver continues to assert Receiver Done each time a character is received but the transmitter no longer asserts Transmitter Ready. Only the first character of a break condition is echoed. The transmitter goes to the mark state until the next valid start is detected.

Local Loopback – In this mode, the transmitter output is internally connected to the receiver input. The external transmitter output is held in the mark state. The transmitter must be enabled but the receiver need not be enabled (see RxEN and TxEN bits). The DTR and RTS bits must both be set for local loopback to function correctly.

Remote Loopback – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver no longer asserts Receiver Done each time a character is received and the transmitter no longer asserts Transmitter Ready. Only the first character of a break condition is echoed. The transmitter goes to the mark state until the next valid start is detected. The error status bits, PE, OE, and FE still function in this mode.

They are read/write bits.

Bit 05 RTS – Request To Send. There is no external hardware support for this signal. However, it must be set for local loopback mode to function correctly (see OM1–OM0 bits).

It is a read/write bit.

Bit 04 RE – Reset Error. Setting RE causes the error bits, PE, OE, and FE in the status register to be cleared. It is always read as a 0.

It is a write-once bit.

Bit 03 FB – Force Break. When cleared, normal transmitter operation occurs. When set, the transmitter output signal enters and holds the space condition at the end of the current transmitted character.

It is a read/write bit.

Bit 02 RxEN – Receiver Enable. When set, the receiver is enabled for normal operation. When cleared, the receiver immediately terminates operation and clears Receiver Done. Disabling the receiver clears the error bits PE, OE, and FE in the status register.

It is a read/write bit.

Bit 01 DTR – Data Terminal Ready. There is no external hardware support for this signal. However, it must be set for local loopback mode to function correctly (see OM1–OM0 bits).

It is a read/write bit.

Bit 00 TxEN – Transmitter Enable. When set, the transmitter is enabled for normal operation. When cleared, the transmitter is disabled. If the transmitter is disabled, it completes transmitting any character that was already begun before terminating operation (not a character pending in the transmitter holding register). When disabled, the transmitter output stays in the mark state and the transmitter ready bit is cleared.

It is a read/write bit.

5.4.10.2 Keyboard Default State After Power-Up – After the power-up self-test is completed, the firmware initializes the keyboard port as follows.

Mode Register 1
1 stop bit
Parity disabled
8 bits per character

Mode Register 2
4800 baud

Command Register
Normal operation
RTS enabled
Force break disabled
Receiver enabled
DTR enabled
Transmitter enabled

5.4.11 Printer

There is a serial printer port on the system module. It can perform asynchronous serial communications at programmable baud rates up to 19.2 kilobaud. The port uses EIA RS-423 signal levels and connection is made on the rear of the unit via a 9-pin male D-subminiature connector, J6. Section 5.6 shows the pinning and position of J6 on the system module. The printer cable part number is PN BCC05.

5.4.11.1 Printer Port Interface –

Addresses

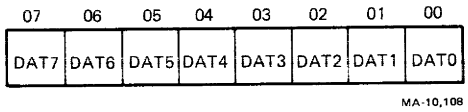
17773400	Data buffer register
17773402	Status register
17773404	Mode registers
17773406	Command register

Vectors

220	Receiver
224	Transmitter

All the printer port registers use only the low byte. The high bytes are always read as all 0s and writes to high bytes have no effects. This port is not a standard DL type interface. It can be made to look like a standard DL interface without the interrupt enable bits at the terminal address of 17777560. See Section 5.4.15 on maintenance terminal registers.

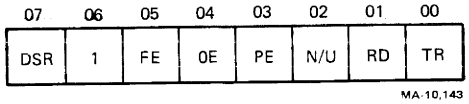
Data Buffer Register (DBUF)



Bits 07–00 DAT7–DAT0 – Data. On read operations, this register operates as the receiver holding register and contains the last received character. The character is right justified if the character length is less than eight bits. On write operations, this register operates as the transmitter holding register and should be loaded with the next character to be transmitted.

They are read/write bits.

Status Register (STAT)



Bit 07 DSR – Data Set Ready. This bit shows the state of the DSR signal input and can be used to determine that the printer is connected and ready. When DSR is set, it indicates that the DSR signal input is asserted and the printer is present and ready. When DSR is cleared, it indicates that the DSR signal input is not asserted and the printer is either not present or not ready.

It is a read-only bit.

Bit 06 It is not used and is always read as a 1.

It is a read-only bit.

Bit 05 FE – Framing Error. When set, it indicates that the received character was not framed by the programmed number of stop bits. If the received character is all 0s and FE is set, a break condition was detected. When cleared, FE indicates that the received character was correctly framed. FE can be cleared by disabling the receiver or by a Reset Error command in the command register. See section on command register.

It is a read-only bit.

Bit 04 OE – Overrun Error. When set, it indicates that the previous character loaded into the receiver holding register was not read by the processor by the time that a new received character was loaded into it. When cleared, no overrun condition occurred. OE can be cleared by disabling the receiver or by a Reset Error command in the command register. See the section on command register.

It is a read-only bit.

Bit 03 PE – Parity Error. When set, it indicates that the received character had a parity error. When cleared, it indicates that no parity error was detected. This bit functions when parity is enabled. See section on mode register. PE can be cleared by disabling the receiver or by a Reset Error command in the command register. See the section on command register.

Is is a read-only bit.

Bit 02 N/U – It is not used.

It is a read-only bit.

Bit 01 RD – Receiver Done. When set, it indicates that a character was received and loaded into the receiver holding register for the processor to read. When cleared, it indicates that no new character was loaded into the receiver holding register. RD can be cleared by reading the receiver holding register or by disabling the receiver in the command register. See the section on command register. If remote loopback mode is enabled in the command register, RD is not set when characters are received. See the section on command register.

It is a read-only bit.

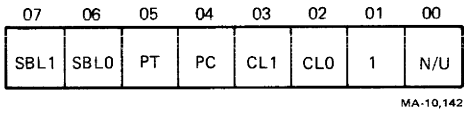
Bit 00 TR – Transmitter Ready. TR is only valid when the transmitter is enabled in the command register. See the section on command register. When TR is cleared, it indicates that the transmitter holding register is not ready to receive another character for transmission from the processor. When set, it indicates that the processor may load the next character for transmission into the transmitter holding register. TR is cleared when operating in auto echo or remote loopback modes. See the section on command register.

It is a read-only bit.

Mode Registers (MR1 AND MR2)

There are two mode registers that select the operating mode of the printer port. Both registers reside at the same address. Operations (read or write) to a mode register cause an internal pointer to point to the other mode register for the next operation. Reading the command register always causes the internal pointer to point to mode register 1. Both mode registers are cleared when the system power is turned on. The processor has to initialize both registers to the specified mode of operation. The two mode registers are described in the following paragraphs.

Mode Register 1 (MR1)



Bits 07–06 SBL1–SBL0 – Stop Bit Length. These bits select character framing of 1, 1.5, or 2 stop bits for both the transmitter and the receiver. The stop bits are selected as follows.

SBL1	SBL0	STOP	Bit Length
0	0		Invalid
0	1	1	Stop bit
1	0	1.5	Stop bits
1	1	2	Stop bits

They are read/write bits.

Bit 05 PT – Parity Type. When set, PT selects even parity. When cleared, PT selects odd parity. Parity type is the same for the transmitter and the receiver. This bit has no effect if parity is not enabled (see PC bit).

It is a read/write bit.

Bit 04 PC – Parity Control. When cleared, parity is disabled for the transmitter and the receiver. When set, the transmitter adds a parity bit to the transmitted character and the receiver performs a parity check on incoming characters. The PT bit selects odd or even parity.

It is a read/write bit.

Bits 03–02 CL1–CL0 – Character Length. These bits select the number of data bits per character for the transmitter and the receiver. The character length does not include the parity bit if any, the start bit, or the stop bits. Character length is selected as follows.

CL1	CL0	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

They are read/write bits.

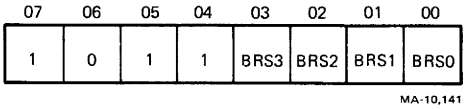
Bit 01 — 1 – This bit must always be set to a one for correct operation. When the system power is turned on, this bit is cleared. The processor must set it to a one before attempting to use the printer port.

It is a read/write bit.

Bit 00 — N/U – It is not used.

It is a read/write bit.

Mode Register 2 (MR2)



Bits 07–04 — 1011 – These bits must always be programmed to 1011 for correct operation. When the system power is turned on, these bits are cleared. The processor must program them before attempting to use the printer port.

They are read/write bits.

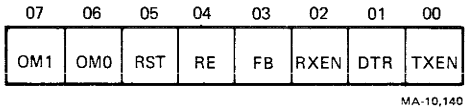
Bits 03–00 — BRS3–BRS0 – Baud Rate Select. These bits determine the frequency of the internal baud rate generator. The frequency is 16 times the selected baud rate. These bits select the clock for both the transmitter and receiver. The accuracy of the input frequency to the baud rate generator is ±0.01%. The baud rate is selected as follows.

BRS3	BRS2	BRS1	BRS0	Baud Rate	Baud Rate Generator Percent Error
0	0	0	0	50	
0	0	0	1	75	
0	0	1	0	110	
0	0	1	1	134.5	+0.016
0	1	0	0	150	
0	1	0	1	300	
0	1	1	0	600	
0	1	1	1	1200	
1	0	0	0	1800	
1	0	0	1	2000	+0.253
1	0	1	0	2400	
1	0	1	1	3600	
1	1	0	0	4800	
1	1	0	1	7200	
1	1	1	0	9600	
1	1	1	1	19200	+3.125

They are read/write bits.

Command Register (CMD)

The command register also controls the printer port operator. The command register is cleared when system power is turned on. The processor has to initialize the register to the specified mode of operation. The command register is described in the following paragraphs.



Bits 07–06 OM1–OM0 – Operating Mode. These bits select the operating mode of the port as follows.

OM1	OM0	Operating Mode
0	0	Normal operation
0	1	Automatic echo mode
1	0	Local loopback
1	1	Remote loopback

These modes are described in the following paragraphs.

Normal – The transmitter and receiver operate independently according to the mode and status registers.

Automatic Echo – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver continues to assert Receiver Done each time a character is received but the transmitter no longer asserts Transmitter Ready. Only the first character of a break condition is echoed. The transmitter goes to the mark state until the next valid start is detected.

Local Loopback – In this mode, the transmitter output is connected to the receiver input internally. The external transmitter output is held in the mark state. The transmitter must be enabled but the receiver need not be enabled (see RxEN and TxEN bits). The DTR and RTS bits must both be set for local loopback to function correctly.

Remote Loopback – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver no longer asserts Receiver Done each time a character is received and the transmitter no longer asserts Transmitter Ready. Only the first character of a break condition is echoed. The transmitter goes to the mark state until the next valid start is detected. The error status bits, PE, OE, and FE still function in this mode.

They are read/write bits.

Bit 05 RTS – Request To Send. There is no external hardware support for this signal. However, it must be set for local loopback mode to function correctly (see OM1–OM0 bits).

It is a read/write bit.

Bit 04 RE – Reset Error. Setting RE clears the error bits, PE, OE, and FE in the status register. It is always read as a 0.

It is a write-once bit.

Bit 03 FB – Force Break. When cleared, normal transmitter operation occurs. When set, the transmitter output signal enters and holds the space condition at the end of the current transmitted character.

It is a read/write bit.

Bit 02 RxEN – Receiver Enable. When set, the receiver is enabled for normal operation. When cleared, the receiver immediately terminates operation and clears Receiver Done. Disabling the receiver clears the error bits, PE, OE, and FE in the status register.

It is a read/write bit.

Bit 01 DTR – Data Terminal Ready. When set, the Data Terminal Ready signal is asserted on the printer port connector. When cleared, the DTR signal is not asserted on the printer connector. This bit must be set for local loopback mode to function correctly (see OM1–OM0 bits).

It is a read/write bit.

Bit 00 TxEN – Transmitter Enable. When set, the transmitter is enabled for normal operation. When cleared, the transmitter is disabled. If the transmitter is disabled, it finishes transmitting any character that was already begun before terminating operation (not a character pending in the transmitter holding register). When disabled, the transmitter output stays in the mark state and the transmitter ready bit is not asserted.

It is a read/write bit.

5.4.11.2 Printer Default State After Power-Up – After the power-up self-test has completed, the firmware initializes the printer port as follows.

Mode Register 1
1 stop bit
Parity disabled
8 bits per character

Mode Register 2
4800 baud (9600 baud if terminal cable is attached)

Command Register
Normal operation
RTS enabled
Force break disabled
Receiver enabled
DTR enabled
Transmitter enabled

5.4.12 Communications

A communication port on the system module operates in asynchronous and bit or byte synchronous protocols. In asynchronous mode, it can be run at split programmable baud rates up to 19.2 kilobaud. In synchronous mode, it can run up to 740 kilobaud. The transmitter is double-buffered and the receiver is quad-buffered. A full set of modem controls is also present. All the port signals are EIA RS-423 levels. Connection is made on the rear of the unit via a 25-pin male D-subminiature connector, J7. Refer to Section 5.6 for a pin listing of J7 on the system module.

There are two interrupts associated with the communications port. The first interrupts the CPU if the USART chip needs service for the receiver or transmitter. The second interrupt indicates that a state change has occurred on one of four modem control signals. These four modem control signals are Ring Indicator (RI), Data Set Ready (DSR), Clear To Send (CTS), and Carrier Detect (CD).

5.4.12.1 Communication Port Interface –

Addresses

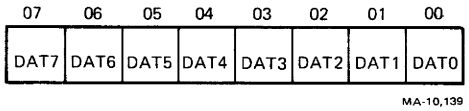
17773300	Data buffer register
17773302	Control/status register A
17773304	Reserved
17773306	Control/status register B
17773310	Modem Control register 0
17773312	Modem control register 1
17773314	Baud rate register

Vectors

210	Receive/transmit
214	Modem change

All the communication port registers use only the low byte. The high bytes are always read as all 0s and writes to the high bytes have no effects. The reserved register (17773304) responds to read and write accesses but reads always produce all 0s and writes have no effect. The other registers are described in the following paragraphs.

Data Buffer Register



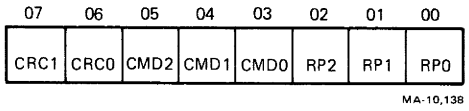
Bits 07–00 DAT7–DAT0 – Data. On read operations, this register contains data bytes received by the communication port. The receiver has a 3-byte buffer for holding received characters. On write operations, this register operates as a transmitter holding register and should be loaded with the next character to be transmitted.

They are R/W bits.

Control/Status Register A

This register operates as a window to 11 internal registers. The internal registers are eight write registers and three read registers. The write registers are labeled WR0-WR7 and control the different operating modes of the communication port. The read registers are labeled RR0-RR2 and provide status information. An internal pointer register selects which command or status registers to be read or written during an access to control/status register A. After reset, the pointer register contents are 0. The first write to the control/status register loads the data into WR0. The three least significant bits of WR0 operate as the pointer register. The next access to the control/status register accesses the internal register selected by the pointer register. The pointer is reset after the read or write operation is completed.

Write Register 0 (WR0)



Bits 07–06 CRC1–CRC0 – CRC Reset Code. When written, these bits have the following effect.

CRC1	CRC0	Effect
0	0	Null – It has no effect.
0	1	Resets receive CRC checker – resets the CRC checker to 0s. If in SDLC mode the CRC checker is set to all 1s.
1	0	Resets transmit CRC generator – resets the CRC generator to 0s. If in SDLC mode, the CRC generator is set to all 1s.
1	1	Resets Transmitter Underrun/End of Message Latch.

They are write-only bits.

Bits 05–03 CMD2–CMD0 – Command Bits. These bits determine which of seven commands to perform.

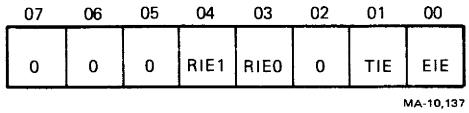
Command (octal)	Effect
0	Null – no effect.
1	Send Abort – generates eight to thirteen 1s when in SDLC mode.
2	Reset External/Status Interrupts – resets the latched status bits of RR0 and reenables them, allowing interrupts to occur again.
3	Channel Reset – resets the latched status bits of RR0, the interrupt priority logic, and all control registers in the channel. Allow two microseconds for the channel reset time before any additional commands or controls are written into the channel.
4	Enable Interrupt on Next Receive Character – if the interrupt on first receive character mode is selected, this command reactivates that mode again after each complete message is received to prepare for the next message.
5	Reset Transmitter Interrupt Pending – if the transmit interrupt enable mode is selected, the channel automatically interrupts when the transmit buffer becomes empty. When there are no more characters to be sent, issuing this command prevents additional transmitter interrupts until the next character has been completely sent.
6	Error Reset – error latches, parity, and overrun errors in RR1 are reset.
7	End of Interrupt – resets the interrupt-in-service latch of the highest priority internal device under service and allows lower priority devices to interrupt.

They are write-only bits.

Bits 02–00 RP2–RP0 – Register Pointer bits. These bits determine which write register the next byte is written into or which read register the next byte is read from. After reset, the first byte written goes into WR0. Following a read or a write to any register (except WR0) the pointer points to WR0.

They are write-only bits.

Write Register 1 (WR1)



Bits 07–05 N/U – They are not used and must always be written as 0s.

They are write-only bits.

Bits 04–03 RIE1–RIE0 – Receiver Interrupt Enable bits. These bits enable receiver interrupts in the following modes.

RIE1	RIE0	Function
0	0	Disables receiver and special condition interrupts
0	1	Enables interrupt on first received character only or special condition
1	0	Enables interrupt on all receive characters or special condition (parity error is a special receive condition)
1	1	Enables interrupt on all receive characters or special condition (parity error is not a special receive condition)

They are write-only bits.

Bit 02 N/U – It is not used and must always be written as a 0.

It is a write-only bit.

Bit 01 TIE – Transmitter Interrupt Enable. When set, it allows transmitter interrupts to occur when the transmitter buffer is empty. When cleared, no transmitter interrupts occur.

It is a write-only bit.

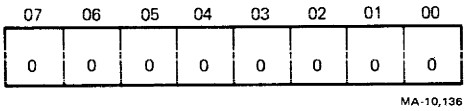
Bit 00 EIE – External Interrupt Enable. When set, it allows interrupts when one of the following occur.

1. Entering or leaving synchronous hunt phase
2. Break detection or termination
3. SDLC abort detection or termination
4. Idle/CRC latch becoming set (CRC being sent)

When cleared, no such interrupt occurs.

It is a write-only bit.

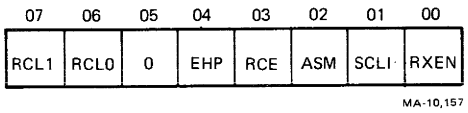
Write Register 2 (WR2)



Bits 07–00 N/U – They are not used. If this register is written, it must be written with all 0s.

They are write-only bits.

Write Register 3 (WR3)



Bits 07–06 RCL1–RCL0 – Receiver Character Length. These bits determine the receiver character length as follows.

RCL1	RCL0	Data Bits/Character
0	0	5
0	1	7
1	0	6
1	1	8

They are write-only bits.

Bit 05 N/U – It is not used and must be written as a 0.

It is a write-only bit.

Bit 04 EHP – Enter Hunt Phase. After initialization, the channel automatically enters the hunt mode. If synchronization is lost, the hunt phase may be reentered by writing a 1 to this bit.

It is a write-only bit.

Bit 03 RCE – Receiver CRC Enable. Writing a 1 to this bit enables (or reenables) CRC calculation. CRC calculation starts with the last character placed in the receiver buffer. Writing a 0 to this bit disables but does not reset the receiver CRC generator.

It is a write-only bit.

Bit 02 ASM – Address Search Mode. In SDLC mode, all frames are received if this bit is 0. If this bit is a 1, frames are only received with address bytes that match the global address (11111111) or the value loaded into WR6. This bit must be 0 in non-SDLC modes.

It is a write-only bit.

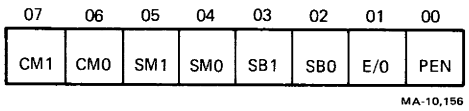
Bit 01 SCLH – Sync Character Load Inhibit. Setting this bit prevents the receiver from loading sync characters into the receive buffer.

It is a write-only bit.

Bit 00 RXEN – Receiver Enable. Setting this bit enables the receiver to start. It should be set only after the receiver is initialized.

It is a write-only bit.

Write Register 4 (WR4)



Bits 07–06 CM1–CM0 – Clock Mode. These bits select the clock rate multiplier for both the receiver and transmitter as follows.

CM1	CM0	Clock Rate
0	0	1 x
0	1	16 x
1	0	32 x
1	1	64 x

In synchronous modes, 1 x must be selected.

They are write-only bits.

Bits 05–04 SM1–SM0 – Synchronous Mode. These bits select the synchronous protocol when synchronous operation is selected. They are ignored when asynchronous operation is selected.

SM1	SM0	Mode
0	0	8-bit internal sync character (monosync)
0	1	16-bit internal sync character (bisync)
1	0	SDLC
1	1	Invalid

They are write-only bits.

Bits 03–02 SB1–SB0 – Stop Bits. These bits select the number of stop bits for asynchronous operation. They also select whether the mode of operation is asynchronous or synchronous.

SB1	SB0	Mode
0	0	Select synchronous operation
0	1	1 stop bit – asynchronous operation
1	0	1.5 stop bits – asynchronous operation
1	1	2 stop bits – asynchronous operation

They are write-only bits.

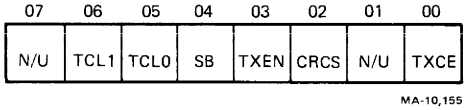
Bit 01 E/O – Even/Odd Parity. This bit selects even or odd parity for both the receiver and transmitter when parity is enabled. A 1 selects even parity and a 0 selects odd parity.

It is a write-only bit.

Bit 00 PEN – Parity Enable. When cleared, parity is disabled. When set, parity is enabled for both the receiver and transmitter. If the receiver character length is programmed to 8 data bits, the parity bit is not transferred to the processor. With other receiver character lengths, the parity bit is transferred to the processor.

It is a write-only bit.

Write Register 5 (WR5)



Bit 07 N/U – It is not used.

Bit 06–05 TCL1–TCL0 – Transmitter Character Length. These bits determine the transmitter character length as follows.

TCL1	TCL0	Data Bits/Character
0	0	5 or less
0	1	7
1	0	6
1	1	8

Normally each character is sent to the transmitter right-justified and the unused bits are ignored. However, when sending 5 or less bits per character, the data should be formatted as follows.

D7	D6	D5	D4	D3	D2	D1	D0	Bits/Character
0	0	0	D4	D3	D2	D1	D0	5
1	0	0	0	D3	D2	D1	D0	4
1	1	0	0	0	D2	D1	D0	3
1	1	1	0	0	0	D1	D0	2
1	1	1	1	0	0	0	D0	1

They are write-only bits.

Bit 04 SB – Send Break. Writing a 1 to this bit causes the transmit data line to immediately go to the space condition. Writing a 0 to the bit allows normal transmitter operation.

It is a write-only bit.

Bit 03 TXEN – Transmitter Enable. Writing a 1 to this bit enables the transmitter and should only be done after the transmitter is initialized. Writing a 0 to this bit disables the transmitter and enters either the idle or mark state.

Bit 02 CRCS – CRC Select. This bit selects which CRC polynomial to be used by both the receiver and transmitter.

CRCS	Mode	Polynomial
0	CRC-CCITT	$\times16 + \times15 + \times5 + 1$
1	CRC-16	$\times16 + \times15 + \times2 + 1$

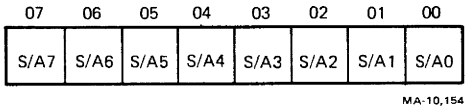
It is a write-only bit.

Bit 01 N/U – It is not used.

Bit 00 TXCE – Transmitter CRC Enable. Writing a 1 to this bit enables the transmitter CRC generator. Writing a 0 to this bit disables the transmitter CRC generator.

It is a write-only bit.

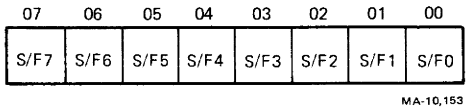
Write Register 6 (WR6)



Bits 07–00 S/A7–S/A0 – Sync/Address Register. This register should be loaded with the transmit sync character in monosync mode, the low order 8 sync bits in bisync mode, or the address byte in SDLC mode.

They are write-only bits.

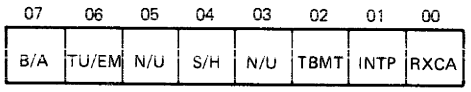
Write Register 7 (WR7)



Bits 07–00 S/F7–S/F0 – Sync/Flag Register. This register should be loaded with the receive sync character in monosync mode, the high order 8 sync bits in bisync mode, or the flag character (01111110) in SDLC mode.

They are write-only bits.

Read Register 0 (RR0)



Bit 07 B/A – Break/Abort. When this bit is a 1 in asynchronous mode, it indicates the detection of a break (a null character plus a framing error which occurs when the receive input line is held in the space state for more than one character time). The B/A bit resets to a 0 when the line returns to the mark state. In SDLC mode, a 1 indicates the detection of an abort sequence (seven or more 1s received in sequence). The B/A bit resets when a 0 is received. Any transition of the Break/Abort bit causes an external/status interrupt.

It is a read-only bit.

Bit 06 TU/EM – Transmitter Underrun/End of Message. This bit is set following a reset. It can only be reset by writing a Reset Transmitter Underrun/End of Message Latch command into WR0. When the transmit underrun condition occurs, this bit is set and an external/status interrupt is generated.

It is a read-only bit.

Bit 05 N/U – It is not used.

It is a read-only bit.

Bit 04 S/H – Sync/Hunt. The meaning of this bit depends on the mode of operation. In asynchronous mode, the bit is read as a 0. In monosync, bisync, or SDLC modes, this bit indicates whether the receiver is in the sync hunt or receive data operation phase. A 0 indicates the receive data phase and a 1 indicates the sync hunt phase. A transition of this bit causes an external/status interrupt.

It is a read-only bit.

Bit 03 N/U – It is not used.

It is a read-only bit.

Bit 02 TBMT – Transmit Buffer Empty. This bit is set when the transmitter buffer is empty except during the transmission of CRC.

It is a read-only bit.

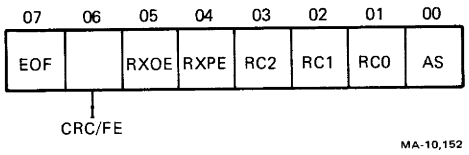
Bit 01 INTP – Interrupt Pending. This bit is set when the vector of a pending interrupt is read from control/status register B. It is reset when an End of Interrupt command is issued in WR0 and no other interrupt is pending at the time.

It is a read-only bit.

Bit 00 RXCA – Receive Character Available. This bit is set when the receiver buffer contains data and is reset when the buffer is empty.

It is a read-only bit.

Read Register 1 (RR1)



Bit 07 EOF – End of Frame. This bit is valid only in SDLC mode. A 1 indicates that a valid ending flag is received. EOF is reset by either an Error Reset command (in WR0) or when it receives the first character of the next frame.

It is a read-only bit.

Bit 06 CRC/FE – CRC/Framing Error. In asynchronous mode, a 1 indicates a receiver framing error. In synchronous modes, a 1 indicates that the calculated CRC value does not match the last two bytes received. CRC/FE is reset by issuing an error reset command in WR0.

It is a read-only bit.

Bit 05 RXOE – Receiver Overrun Error. When set, this bit indicates that the receiver buffer is overloaded by the receiver. The last character in the buffer (the third character) is overwritten and flagged with this error. Once the overwritten character is read, this error is latched until reset by the error reset command in WR0.

It is a read-only bit.

Bit 04 RXPE – Receiver Parity Error. If parity is enabled, this bit is set for received characters whose parity does not match the programmed sense (odd/even). This bit is latched until it is reset by issuing a error reset command in WR0.

It is a read-only bit.

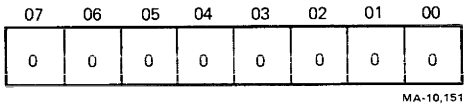
Bit 03–01 RC2–RC0 – Residue Codes. Bit synchronous protocols allow I-fields that are not an integral number of characters. Because transfers from the communications port to the CPU are character oriented, the residue codes provide the capability of receiving leftover bits. Residue bits are right-justified in the last two data bytes received.

They are read-only bits.

Bit 00 AS – All Sent. In asynchronous mode, this bit is set when the transmitter is empty and reset when a character is present in either the transmitter buffer or the transmitter shift register. In synchronous mode, this bit is always a 1.

It is a read-only bit.

Read Register 2 (RR2)



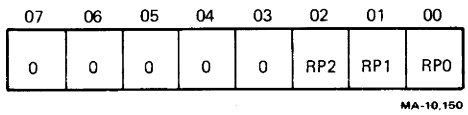
Bits 07–00 N/U – They are not used and are always read as 0s.

They are read-only bits.

Control/Status Register B

This register operates as a window to 11 internal registers as did control/status register A. The internal registers consist of eight write registers and three read registers. The write registers are labeled WR0-WR7 and the read registers are labeled RR0-RR2. An internal pointer register selects which WR or RR registers to be read or written during an access to control/status register B. After reset, the pointer register contents are 0. The first write to the control/status register loads the data into WR0. The three least significant bits of WR0 are the pointer register. The next access to the control/status register accesses the internal register selected by the pointer register. The pointer is reset after the read or write operation is completed. In control/status register B, only WR0, WR1, WR2, and RR2 should be accessed. These four registers are described in the following paragraphs.

Write Register 0 (WR0)



Bits 07–06 N/U – They are not used and must always be written as 0s.

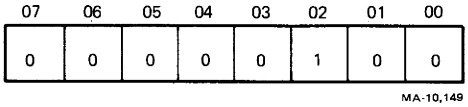
They are write-only bits.

Bits 02–00 RP2–RP0 – Register Pointer bits. These bits determine which write register the next byte is written into or which read register the next byte is read from. After reset, the first byte written goes into WR0.

Following a read or a write to any register (except WR0) the pointer points to WR0. The pointer should only be used to access WR0, WR1, WR2, and RR2.

They are write-only bits.

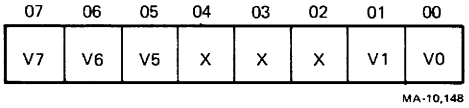
Write Register 1 (WR1)



Bits 07–00 This register must be loaded with 00000100 for correct vector information when servicing interrupts from the communication port. No other data should ever be written into this register.

They are write-only bits.

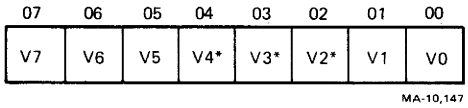
Write Register 2 (WR2)



Bits 07–00 V7–V0 – Vector bits. This register should be written with a base vector for the channel interrupts (receiver, special receive, transmitter, and external/status interrupts). It is used when reading RR2 to get the vector. It does not matter what bits 04-02 are because they are modified to identify the four channel interrupts. Refer to the next section on RR2 for details.

They are write-only bits.

Read Register 2 (RR2)



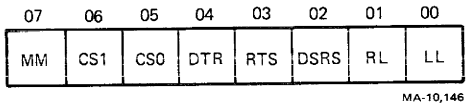
Bits 07–00 V7–V0 – Vector. This register is used to get the vector of the highest priority interrupt pending in the communication channel. The vector is the same as the contents that were written into WR2. Bits V4–V2 are modified to identify which condition caused the interrupt. After a receive/transmit interrupt causes the CPU to vector through location 210, the interrupt service routine should read RR2 to get the secondary vector that identifies which condition caused the interrupt.

V4	V3	V2	Condition Causing Interrupt
0	0	0	Transmitter buffer empty
1	0	1	External/status change
1	1	0	Receiver character available
1	1	1	Special receiver condition

If RR2 is read when no interrupt is pending, the vector is read with the variable bits V4–V2 set to all 1s.

They are read/write bits.

Modem Control Register 0



Bit 07 MM – Maintenance Mode. When set, this bit loops the communications channel transmit data line onto the receiver data line. The transmit data signal to the modem is held in the mark state and the receive data from the modem is ignored. It is cleared at power up or by a RESET instruction.

It is a read/write bit.

Bit 06–05 CS1–CS0 – Clock Source. These bits select the source of the transmit and receive baud rate clocks to the communications channel. The clock sources can be either the baud rate generator or the modem. The communication port can also provide the transmit clock to the modem. The following indicates how the selection is made.

		Sources for Clocks		
CS1	**CS0**	**RXC**	**TXC**	**TXC/DTE**
0	0	RBRG	TBRG	None
0	1	RXC/DCE	TXC/DCE	None
1	0	RXC/DCE	TBRG	TBRG
1	1	TBRG	TBRG	None

RBRG – clock is from receiver baud rate generator.

TBRG – clock is from transmitter baud rate generator.

RXC/DCE – clock is the receive clock line from modem.

TXC/DCE – clock is the transmit clock line from modem.

NONE – no clock signal is sent to modem.

The RXC column gives the source of the receiver baud rate clock to the channel. The TXC column gives the source of the transmitter baud rate clock. The TXC/DTE column indicates the clock that the communications port sends to the modem. It is cleared at power up or by a RESET instruction.

They are read/write bits.

Bit 04 DTR – Data Terminal Ready. When set, this signal is asserted to the modem. When cleared, the DTR signal is removed from the modem. It is cleared at power up or by a RESET instruction.

It is a read/write bit.

Bit 03 RTS – Request To Send. When set, this signal is asserted to the modem. When cleared, the RTS signal is removed from the modem. It is cleared at power up or by a RESET instruction.

It is a read/write bit.

Bit 02 DSRS – Data Signaling Rate Select. When set, this signal is asserted to the modem. When cleared, the DSRS signal is removed from the modem. It is cleared at power up or by a RESET instruction.

It is a read/write bit.

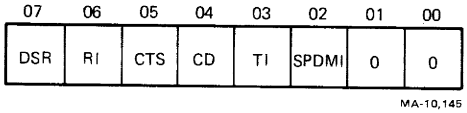
Bit 01 RL – Remote Loopback. When set, this signal is asserted to the modem. When cleared, the RL signal is removed from the modem. It is cleared at power up or by a RESET instruction.

It is a read/write bit.

Bit 00 LL – Local Loopback. When set, this signal is asserted to the modem. When cleared, the LL signal is removed from the modem. It is cleared at power up or by a RESET instruction.

It is a read/write bit.

Modem Control Register 1



Bit 07 DSR – Data Set Ready. This bit indicates the state of the DSR signal from the modem. A 1 indicates that DSR is asserted and a 0 indicates that it is not asserted. A transition of this signal generates a modem change interrupt.

It is a read-only bit.

Bit 06 RI – Ring Indicator. This bit indicates the state of the RI signal from the modem. A 1 indicates that RI is asserted and a 0 indicates that it is not asserted. A transition of this signal generates a modem change interrupt.

It is a read-only bit.

Bit 05 CTS – Clear To Send. This bit indicates the state of the CTS signal from the modem. A 1 indicates that CTS is asserted and a 0 indicates that it is not asserted. A transition of this signal generates a modem change interrupt.

It is a read-only bit.

Bit 04 CD – Carrier Detect. This bit indicates the state of the CD signal from the modem. A 1 indicates that CD is asserted and a 0 indicates that it is not asserted. A transition of this signal generates a modem change interrupt.

It is a read-only bit.

Bit 03 TI – Test Indicator. This bit indicates the state of the TI signal from the modem. A 1 indicates that TI is asserted and a 0 indicates that it is not asserted.

It is a read-only bit.

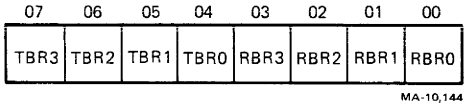
Bit 02 SPDMI – Speed Mode Indicator. This bit indicates the state of the SPMI signal from the modem. A 1 indicates that SPDMI is asserted and a 0 indicates that it is not asserted.

It is a read-only bit.

Bits 01–00 N/U – They are not used and are always read as 0s.

They are read-only bits.

Baud Rate Register



Bits 07–04 TBR3–TBR0 – Transmitter Baud Rate select. These bits program the transmitter baud rate generator. The accuracy of the input frequency to the baud rate generator is ±0.01%.

TBR3	TBR2	TBR1	TBR0	ASYNC 16 X Clock Baud Rate	SYNC 1 X Clock Baud Rate	Baud Rate Generator Percent Error
0	0	0	0	50		
0	0	0	1	75	1200	
0	0	1	0	110		
0	0	1	1	134.5		+0.016
0	1	0	0	150	2400	
0	1	0	1	300	4800	
0	1	1	0	600	9600	
0	1	1	1	1200	19200	
1	0	0	0	1800		
1	0	0	1	2000		+0.253
1	0	1	0	2400		
1	0	1	1	3600		
1	1	0	0	4800		
1	1	0	1	7200		
1	1	1	0	9600		
1	1	1	1	19200		+3.125

They are write-only bits.

Bits 03–00 RBR3–RBR0 – Receiver Baud Rate select. These bits program the receiver baud rate generator. The accuracy of the input frequency to the baud rate generator is ±0.01%.

RBR3	RBR2	RBR1	RBR0	ASYNC 16 X Clock Baud Rate	Baud Rate Generator Percent Error
0	0	0	0	50	
0	0	0	1	75	
0	0	1	0	110	
0	0	1	1	134.5	+0.016
0	1	0	0	150	
0	1	0	1	300	
0	1	1	0	600	
0	1	1	1	1200	
1	0	0	0	1800	
1	0	0	1	2000	+0.253
1	0	1	0	2400	
1	0	1	1	3600	
1	1	0	0	4800	
1	1	0	1	7200	
1	1	1	0	9600	
1	1	1	1	19200	+3.125

They are write-only bits.

5.4.12.2 Communications Port Default State After Power Up – When the power-up self-test is completed, the firmware initializes the communications port. The firmware issues a Channel Reset command to both control/status register A and control/status register B. This clears all the internal control registers in the communications USART. In addition, the firmware loads the modem and baud rate registers as follows.

Modem Control Register 0 = 000
Baud Rate Register = 356

5.4.13 Battery Backed-Up System Clock and RAM

The battery backed-up system clock and RAM are part of the same chip. A battery, charged when the system is turned on, maintains the clock and RAM.

The clock's internal system contains a bit to indicate if the clock power gets too low and the time and date may no longer be valid. The bit is in the CSR3 register and is called the VRT (valid RAM and time) bit. See section on CSR3 for details of the VRT bit.

The chip can also be programmed to interrupt the CPU at a specified alarm time or at a periodic rate. The periodic rate can be programmed to one of 13 frequencies from 2 Hz to 8.192 KHz. There is no line time clock.

The clock keeps time accurate to within 1 minute per month. This assumes that the system module is installed in the Professional 300 series system box and operates within the specified temperature limits for the system. See Section 5.6 for accuracy and temperature specifications.

5.4.13.1 Clock Interface –

Addresses

17773000	Seconds
17773002	Seconds alarm
17773004	Minutes
17773006	Minutes alarm
17773010	Hours
17773012	Hours alarm
17773014	Day of week
17773016	Date of month
17773020	Month
17773022	Year
17773024	CSR0
17773026	CSR1
17773030	CSR2
17773032	CSR3

Vector
230

All 14 registers use only the low byte. The high bytes are always read as all 0s. Writes to high bytes have no effect.

Time, Date, Alarm Registers

The first 10 registers (17773000–17773022) handle the time, date, and alarm functions. Refer to Table 5-19. The contents of these 10 registers can be programmed into either binary or BCD format. All of the registers must be the same format. Bit 02 in CSR1 determines the data format. The hours and hours alarm registers can be programmed into either 12 or 24 hour format. Both registers must be the same format. When the 12 hour format is selected, bit 07 of the two registers indicates AM (when cleared) or PM (when set). The day of week register counts cyclicly from 1 to 7 where 1 represents Sunday. The year register counts cyclicly from 00 to 99. The three alarm registers can generate an interrupt to the processor at the specified time if the alarm interrupt enable bit is set in CSR1. Each of the alarm registers can be programmed to a "don't care" state by setting bits 06 and 07. This allows alarm interrupts to occur every hour, every minute, or every second if specified. All 10 time, date, and alarm registers can be read or written to, but it must be done according to the procedures described in the following paragraphs.

A time and date update cycle starts once each second. The time and date increment by one second and the time is compared to the alarm registers during the update cycle. The update cycle continues for 1984 μs, during which the 10 time, date, and alarm registers are not accessible. Undefined data results if any of these registers are read during an update cycle. There are two methods of assuring correct data:

Table 5-19 Time, Date, and Alarm Modes

Address	Function	Decimal Range	Binary Mode	BCD Mode in Hexadecimal
17773000	Seconds	00–59	000–073	00–59
17773002	Seconds alarm	00–59	000–073	00–59
17773004	Minutes	00–59	000–073	00–59
17773006	Minutes alarm	00–59	000–073	00–59
17773010	Hours: 12-hour AM mode	01–12	001–014	01–12
	Hours: 24-hour PM mode	01–12	201–214	81–92
	Hours: 24-hour mode	00–23	000–027	00–23
17773012	Hours alarm: 12-hour AM mode	01–12	001–014	01–12
	Hours alarm: 12-hour PM mode	01–12	201–214	81–92
	Hours alarm: 24-hour mode	00–23	000–027	00–23
17773014	Day of week	01–07	001–007	01–07
17773016	Date of month	01–31	001–037	01–31
17773020	Month	01–12	001–014	01–12
17773022	Year	00–99	000–143	00–99

1. Bit 07 in CSR0 is the update-in-progress bit (UIP).
   The UIP bit pulses once per second. After the UIP bit goes high, the update cycle begins 244 μs later. If the UIP bit is read as a low, the program has at least 244 μs to read the time and date before the update cycle begins and makes the information inaccessible. If the UIP bit is read as a high, the time and date may not be available.

   CAUTION
   If this method is used, the program should avoid interrupts with service routines that would cause the time needed to read the time and date to exceed 244 μs.

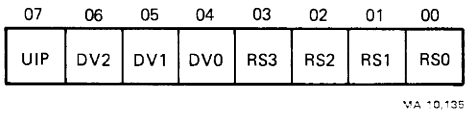
2. An update ended interrupt is provided to indicate that the update cycle is completed. This interrupt occurs at the end of the update cycle if the update interrupt enable bit is set in CSR1. This method gives the program almost a full second to read the time and date before the next update cycle. The interrupt service routine must clear the update ended flag bit in CSR2 for correct operation. See the section on CSR2 for more details.

Care must also be taken when writing to the 10 time, date, and alarm registers. Setting the time and date or programming the alarm must not be done during an update cycle. The following procedures should be used.

1. Setting the time and date is done by using the SET bit in CSR1. Setting the SET bit inhibits update cycles. If an update is in progress when the program sets the SET bit, the update is completed. With updates halted, the program should select the specified formats in CSR1, initialize the time and date registers with the appropriate information, and initialize the alarm registers if used. The SET bit can then be cleared to enable update cycles to occur normally.

2. The alarm registers can be initialized when the time and date are set or when an update cycle is not in progress (using one of the two previously described methods).

Control/Status Register 0 (CSR0)



Bit 07 UIP – Update in Progress. The UIP bit is a status flag that may be monitored by the program. It is set 244 μs before an update cycle starts and is cleared immediately after the update cycle is complete. UIP is not effected by a RESET.

It is a read-only bit.

Bits 06–04 DV2–DV0 – Divider Control. These bits should be initialized to the following.

DV2	DV1	DV0
0	1	0

Any other state of these 3 bits cause incorrect clock operation. These bits are not affected by RESET.

They are read/write bits.

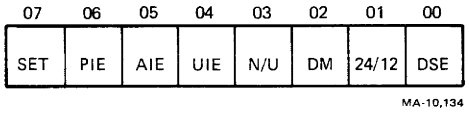
Bits 03–00 RS3–RS0 – Rate Select. These 4 bits select one of 13 periodic rates to generate an interrupt. These bits are not affected by RESET. The periodic rates are selected as follows.

RS3	RS2	RS1	RS0	Periodic Rate	Frequency
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 μs	8192 Hz
0	1	0	0	244.141 μs	4096 Hz
0	1	0	1	488.281 μs	2048 Hz
0	1	1	0	976.562 μs	1024 Hz
0	1	1	1	1.95313 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125.0 ms	8 Hz
1	1	1	0	250.0 ms	4 Hz
1	1	1	1	500.0 ms	2 Hz

The accuracy of these rates is ±0.0025 %.

They are read/write bits.

Control/Status Register 1 (CSR1)



Bit 07 SET – The SET bit halts update cycles to initialize the time and date registers. When set, update cycles are inhibited. If the bit is set during an update, the update cycle is completed. When cleared, normal update cycles occur. SET is not effected by RESET.

It is a read/write bit.

Bit 06 PIE – Periodic Interrupt Enable. When set, it enables periodic interrupts at the rate selected by bits RS3–RS0 in CSR0. When cleared, no periodic interrupts occur. PIE is cleared by RESET.

It is a read/write bit.

Bit 05 AIE – Alarm Interrupt Enable. When set, it enables alarm interrupts to occur at the time specified in the alarm registers. When cleared, no alarm interrupts occurs. AIE is cleared by RESET.

It is a read/write bit.

Bit 04 UIE – Update ended Interrupt Enable. When set, it enables an interrupt to occur at the end of each update cycle. When cleared, no update interrupts occur. UIE is cleared by RESET.

It is a read/write bit.

Bit 03 N/U – It is not used and is cleared by RESET.

It is a read/write bit.

Bit 02 DM – Data Mode. When set, it indicates that the time, date, and alarm registers are in binary format. When cleared, BCD format is selected. DM is not effected by RESET. DM should only be changed when initializing all the time and date registers.

It is a read/write bit.

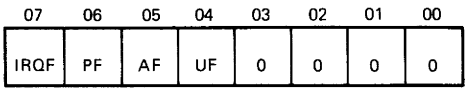
Bit 01 24/12 – 24 Hour Mode/12 Hour Mode. When set, it selects 24 hour clock format. When cleared, it selects 12 hour clock format. AM or PM is indicated by bit 07 in the hours register. 24/12 is not affected by RESET. 24/12 should only be changed when initializing all the time and date registers.

It is a read/write bit.

Bit 00 DSE – Daylight Savings Enable. When set, two special updates are enabled. On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time reaches 1:59:59 AM for the first time, it changes to 1:00:00 AM. When DSE is cleared, these special updates do not occur. DSE is not effected by RESET. DSE should not be changed during an update cycle.

It is a read/write bit.

Control/Status Register 2 (CSR2)



Bit 07 IRQF – Interrupt Request Flag. When set, it indicates that the clock is generating an interrupt to the processor. IRQF is set when one or more of the following conditions occur.

1. The PIE and PF bits are both set.
2. The AIE and AF bits are both set.
3. The UIE and UF bits are both set.

It is a read-only bit.

Bit 06 PF – Periodic Interrupt Flag. PF is set at the end of each period time. The period time is determined by the periodic rate bits RS3–RS0. PF is set independently from the state of the PIE bit. PF set generates a clock interrupt to the processor and causes a one to appear in the IRQF bit if the PIE bit is also set. PF is cleared by RESET or by reading CSR2.

It is a read-once bit.

Bit 05 AF – Alarm Interrupt Flag. AF is set when the time matches the alarm time. AF is set independently from the state of the AIE bit. AF set generates a clock interrupt to the processor and causes a 1 to appear in the IRQF bit if the AIE bit is also set. AF is cleared by RESET or by reading CSR2.

It is a read-once bit.

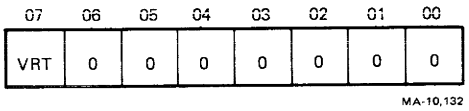
Bit 04 UF – Update-ended Interrupt Flag. UF is set after each update cycle has completed. UF operates independently from the state of the UIE bit. UF set generates an interrupt to the processor and causes a 1 to appear in the IRQF bit if UIE is also set. UF is cleared by RESET or by reading CSR2.

It is a read-once bit.

Bits 03–00 They are not used and are always read as 0s.

They are read-only bits.

Control/Status Register 3 (CSR3)



Bit 07 VRT – Valid RAM and Time. When set, it indicates that the clock has not lost power and that the time and date have been updated correctly since last initialized. If cleared, it indicates that the power to the clock got too low and the time and date may not be valid. The processor should set the VRT bit when it initializes the clock. Reading CSR3 sets the VRT bit. VRT is not effected by RESET. This bit also indicates the validity of the battery backed up RAM.

It is a read-once bit.

Bits 06–00 They are not used and are always read as 0s.

They are read-only bits.

5.4.13.2 System Clock Default State After Power Up – The firmware initializes the clock after the power-up self-test is completed. This default state follows.

CSR 0:
bits <06:04> = 0 1 0 (divider control)
bits <03:00> = 0 0 0 0 (no periodic rate)

CSR 1:
bit 07 (the set bit) is cleared if the battery power got too low and is not effected otherwise
bits <06:04> = 0 0 0 (interrupt enables cleared)
bits <03:00> are not effected

CSR 2:
read-only register not initialized by firmware

CSR 3:
bit 07 = 1 (VRT bit always set)

5.4.13.3 Battery Backed-Up RAM

Addresses
17773034–17773176 50 bytes RAM

All 50 RAM locations use only the low byte. The high bytes are always read as all 0s and writes to high bytes have no effect.

5.4.14 Maintenance ODT

A part of the microcode in the processor emulates the capability found on a "lights and switches" console. However the Professional 350 computer does not have a "lights and switches" console or a console switch register at bus address 17777570. Therefore, a terminal at the standard bus address of 17777560 can perform console functions. Communication between the processor and the user is through a series of ASCII characters which the processor interprets as console commands. The terminal addresses, 17777560 through 17777566 are generated in microcode and can not be changed.

This feature is called microcode on-line debugging technique (Micro-ODT). Micro-ODT accepts 16-bit addresses, allowing it to access 56 kilobytes of memory plus the 8 kilobyte I/O page.

5.4.14.1 Terminal Interface – The hardware interface for a terminal (serial line) to communicate with ODT is the printer port. A terminal cable (PB BCC08) must be used instead of the printer cable (PN BCC05). If the terminal cable is not used, read accesses of the terminal CSRs (addresses 17777560 and 17777564) results in all 0s indicating that the transmitter and the receiver are not ready. See Section 5.4.15 for details about these cables and the maintenance terminal.

5.4.14.2 Entry Conditions – The ODT console mode can be entered as follows.

1. Execution of a HALT instruction in kernel mode.

   or

2. From the maintenance terminal by pressing the BREAK key on the keyboard. The BREAK ENABLE bit in the system CSR must be set and the terminal cable must be used or BREAK is ignored.

On entry, ODT causes the following initialization.

1. Prints a <CR> and <LF>.

2. Prints the PC (program counter contents) in 6 digits (16-bit octal).

3. Performs a read from RBUF (input data buffer at 17777562) and then ignores the character present in the buffer. This prevents ODT interpreting false characters or user program characters as a command.

4. Prints a <CR> and <LF>.

5. Prints the prompt character "@".

6. Enters a wait loop for terminal input. The DONE flag (bit 7) in RCSR at 17777560 is continuously tested via a read by the processor for a 1. If it is a 0, the processor keeps testing.

5.4.14.3 ODT Operation of Serial Line Interface – The processor's microcode operates the serial interface in half-duplex mode by using program I/O techniques instead of interrupts. This means that when the ODT microcode is busy printing characters using the output side of the interface, the microcode is not monitoring the input side for incoming characters. In this condition, all incoming characters are lost. Although the USART chip may post overrun errors, the microcode does not check any error bits in the serial interface.

NOTE

Do not try to type ahead to ODT because those characters will not be recognized. More importantly, if another processor is at the end of the serial line, it must use half duplex operation. No input characters should be sent until ODT's output is completed.

The input sequence for ODT is on entry to ODT, the RBUF register is read and the character ignored to eliminate a possible false command ODT before continuing with the input sequence.

1. Read RCSR bit 7 (Done Flag). If a 0, continue testing.

2. If RCSR bit 7 is a 1, read low byte of RBUF.

The following is the output sequence of ODT.

1. Read XCSR bit 7 (Done Flag). If a 0, continue testing.

2. If XCSR bit 7 is a 1, write the character into the low byte of XBUF.

5.4.14.4 Command Set – This section describes the ODT command set. For these examples, the processor's response appears in boldface type and the user's entry is depicted in medium type. The commands are a subset of ODT-11 and use the same command characters. ODT has 10 internal states. Each state recognizes certain characters as valid input and responds with a "?" to all others. Table 5-20 describes these states.

The parity bit (bit 7) on all input characters is ignored, not stripped, by ODT. If the input character is echoed, the state of the parity bit is copied to the output buffer (XBUF). Output characters internally generated by ODT (for example, <CR>) have the parity bit equal to 0. All commands are echoed except for <LF>.

To describe the use of a command, some commands are referred to before they are defined. This section should be scanned first for familiarity and then re-read for detail. The word location refers to a bus address, processor register, or processor status word (PSW).

/ (ASCII 057) Slash

This command opens a bus address, processor register, or PSW and is normally preceded by other characters that specify a location. In response to /, ODT prints the location contents (for example, six characters) and then a space (ASCII 40). After printing is complete, ODT waits for either new data for that location or a valid close command. The space character is issued so that the location's contents and possible new contents entered by the user can be seen on the terminal.

Example: **@001000/012525 <SPACE>**

where:

@	=	ODT prompt character
001000	=	octal location in the address space specified by the user (leading 0s are not needed)
/	=	command to open and print contents of location
012525	=	contents of octal location 1000
<SPACE>	=	space character generated by ODT

Table 5-20 ODT States

State	Example of Terminal	Valid Output	Input	Comments
1	@ R, $ G P CTL-SHIFT-S H	0-7	Octal digits	
2	@R OR @$ S	0-7		
3	@1000/123456	0-7	 CR LF	
4	@R1/123456	0-7	 CR LF	
5	@1000 /	0-7	 G	
6	@R1 OR @RS S /	0-7		
7	@1000/123456 1000	0-7	 CR LF	
8	@R1/123456 1000	0-7	 CR LF	
9	@ /			Previous location was opened
10	@ CTL-SHIFT-S			2 binary bytes

The / command can be used without a location specifier to verify the data just entered into a previously opened location. The / produces this result only if it is entered immediately after a prompt character. A / issued immediately after the processor enters ODT mode prints a ? <CR> <LF> because a location has not yet been opened.

Example: **@1000/012525 <SPACE> 1234 <CR> <CR> <LF>**
@/001234 <SPACE>

where:

first line	=	new data of 1234 entered into location 1000 and location closed with <CR>.
second line	=	a / was entered without a specified location and the previous location was opened to show that the new contents were correctly entered.

<CR> (ASCII 15) Carriage Return
This command closes an open location. If a location's contents are to be changed, precede the <CR> with the new data. If no change is specified, <CR> closes the location without changing its contents.

Example: **@R1/004321 <SPACE> <CR> <CR> <LF>**
@

Processor register R1 was opened and no change was specified so the user issued <CR>. In response to the <CR>, ODT printed <CR> <LF> and @.

Example: **@R1/004321 <SPACE> 1234 <CR> <CR> <LF>**
@

In this condition, the user wanted to change R1 and the new data, 1234, was entered before issuing the <CR>. ODT deposited the new data in the open location and then printed <CR> <LF> and @.

ODT echoes the <CR> entered by the user and then prints <CR> <LF> @.

<LF> (ASCII 12) Line Feed
This command closes an open location and then opens the next contiguous location. Bus addresses and processor registers are incremented by two and one respectively. If the PSW is open when a <LF> is issued, it closes and prints a <CR> <LF> @; no new location is opened. If the open location's contents are to be changed, the new data should precede the <LF>. If no data is entered, the location is closed without being modified.

Example: **@R2/123456 <SPACE> <LF> <CR> <LF>**
@R3/054321 <SPACE>

In this example, the user entered <LF> with no data preceding it. In response, ODT closed R2 and then opened R3. When a user has the last register, R7, open and issues <LF>, ODT returns to the beginning register, R0.

Example: **@R7/000000 <SPACE> <LF> <CR> <LF>**
@R0/123456 <SPACE>

Unlike other commands, ODT does not echo the <LF>. Instead it prints <CR> then <LF> so that teletype printers operate correctly. In order to make this easier to decode, ODT also does not echo ASCII 0, 2 or 10, but responds to these 3 characters with ? <CR> <LF> @.

$ (ASCII 044) or R (ASCII 122) Internal Register Designator
Either character, when followed by a register number up to 7, or PSW designator, S, opens that specific processor register.

The $ character is compatible with ODT-11. The R character provides an easy one key stroke and is representative of what it does (R = Register).

Example: **@$0/000123 <SPACE>**

Example: **@R7/000123 <SPACE>**

If more than one character (digit or S) after the $ or R is typed, ODT uses the last character as the register designator. An exception: If the last three digits equal 077 or 477, ODT opens the PSW instead of R7.

S (ASCII 123) Processor Status Word
This designator opens the PSW (processor status word) and must be used after the user enters an $ or R register designator.

Example: **@RS/100377 <SPACE> 0 <CR> <CR> <LF>**

@/000010 <SPACE>

Note that the trace bit (bit 4) of the PSW can not be modified by the user. This is so that PDP-11 program debug utilities (for example, ODT-11), which use the T bit for single stepping, are not accidentally damaged by the user. If the user issues a <LF> while the PSW is open, the PSW closes and ODT prints a <CR> <LF> @. No new location is opened in this example.

G (ASCII 107) GO
This command starts program execution at a location entered immediately before the G. This function is equivalent to the LOAD ADDRESS and START switch sequence on other PDP-11 consoles.

Example: **@200G <NULL> <NULL>**

The following is the ODT sequence for a G.

1. Prints two nulls (ASCII 0) so the bus initialize that follows does not purge the G character from the double buffered USART chip in the serial line interface.

2. Loads R7 (PC) with the entered data. If no data is entered, 0 is used. In the above example, R7 equals 200 and this is where program execution will start.

3. The PSW and FPS (floating point status) registers are cleared to 0.

P (ASCII 120) Proceed
This command continues execution of a program and corresponds to the CONTINUE switch on other PDP-11 consoles. No programmer visible machine state is modified using this command.

Example: **@P**

Program execution continues at the place pointed to by R7. After the P is echoed, the ODT state is left and the processor immediately enters the state to fetch the next microinstruction. If a HALT request is asserted, it is recognized at the end (during the service state) of the instruction and the processor enters the ODT state. On entry, the PC (R7) contents are printed. A user can single instruction step through a program and get a PC "trace" displayed on the terminal, a HALT request can be asserted by using the H command.

H (ASCII 110) Halt
The H command asserts a HALT request to the processor and corresponds to the HALT switch on other PDP-11 consoles. Each time the H command is typed, an internal halt request flip-flop is toggled. On entering ODT, the halt request flip-flop is cleared (not asserting a halt request). Typing the H toggles the flip-flop and asserts a halt request. Typing the H again resets the flip-flop and clears the halt request. This allows the user to single step through this code. To single step, the H command should be used to assert a halt request to the processor. Then, each time the P command is typed, one instruction is executed. When single stepping is no longer wanted, type the H command followed by one more P command.

Example: **@H <CR> <LF>**
@

<CONTROL-SHIFT-S> (ASCII 23) Binary Dump
This command is for manufacturing test purposes and is not a normal user command. It displays a part of memory more efficiently than using the / and <LF> commands. The protocol is as follows.

1. After a prompt character, ODT receives a control-shift S command and echoes it.

2. The host system at the other end of the serial line must send two 8-bit bytes which ODT interprets as a starting address. These 2 bytes are not echoed.

   The first byte specifies starting address bits <15:8> and the second byte specifies starting address bits <7:0>. Bus address bits <21:16> are always forced to 0; the dump command is limited to the first 64 kilobytes of address space.

3. After the second address byte has been received, ODT outputs to the serial line 12 octal bytes starting at the address specified previously. When the output is done, ODT prints <CR> <LF> @.

   To exit from the command, if accidentally entered, enter two @ characters (ASCII 100) as a starting address. After the binary dump, the user will receive a prompt character, @.

5.4.14.5 Address Specification – The Professional 300 series Micro-ODT accepts 16-bit addresses, allowing it to access 56 kilobytes of memory plus the 8 kilobyte I/O Page. Addresses 000000 through 157776 correspond to the first 56 Kilobytes of physical memory. Addresses 160000 through 177776 correspond to the I/O page (physical locations 17760000 through 17777776). If an address with more than 16 bits is specified, only the 16 least significant bits are used.

Processor I/O Addresses
Certain processor and MMU registers have I/O addresses assigned to them for programming purposes. If referenced in ODT, the PSW responds to its bus address, 177776. Processor registers R0 through R7 do not respond (time out occurs) to bus addresses 177700 through 177707 if referenced in ODT.

The MMU contains status registers and PAR/PDR pairs. These registers can be accessed from ODT by entering their bus address.

Example: **@177572/000001 <SPACE>**

In this example, memory management status register 0 was opened and the memory management enable bit is set.

The floating point accumulators, which are also in the MMU chip, cannot be accessed from ODT. Only floating point instructions can access these registers.

Stack Pointer Selection
Accessing kernel and user stack pointer registers is done as follows. When R6 is referenced in ODT, it accesses the stack pointer specified by the PS current mode bits (PS<15:14>). This is done for convenience only. If a program operating in kernel mode (PS<15:14> = 00) is halted and R6 is opened, the kernel stack pointer is accessed.

Similarly, if a program is operating in user mode (PS<15:14> = 11), R6 accesses the user stack pointer. If a different stack pointer is wanted, the user must change PS<15:14> to the appropriate value and then the R6 command can be used. If an operating program is halted, the original value of PS<15:14> must be restored to continue execution.

Example:
PS = 140000
@R6/123456 <SPACE>
The user mode stack pointer has been opened.
@RS/140000 <SPACE> <CR> 0 <CR> <CR> <LF>
@R6/001000 <SPACE> <CR> <CR> <LF>
@RS/000000 <SPACE> 140000 <CR> <CR> <LF>
@P

In this example, the kernel mode stack pointer was specified. The PS was opened and PS<15:14> was set to 00 (kernel mode). Then R6 was examined and closed. The original value of PS<15:14> was restored and then the program was continued using the P command.

If PS<15:14> are set to 01, another unique register within the processor is accessed. This register is reserved for future Digital use.

Entering Octal Digits
In general, when specifying an address or data, ODT uses the last six octal digits if more than six have been entered. The user need not enter leading 0s for either address or data; ODT forces 0s as the default. If an odd address is entered, the low order bit is ignored and a full 16-bit word is displayed.

ODT Timeout
If the user specifies a non-existent address, ODT responds to the bus timeout by printing ? <CR> <LF> @. The bus timeout is approximately 6.5 μs.

5.4.14.6 Invalid Characters – In general, any character which ODT does not recognize during a specific sequence is echoed (except the ASCII codes 0, 2, 10, or 12) and ODT prints a ? <CR> <LF> @.

ODT has 10 internal states and each state has its own set of valid input characters. Some commands are only allowed when in certain states or sequences. This lowers the chance of a user accidentally destroying data by pressing the wrong key. Table 5-20 defines the states and valid input characters.

5.4.15 Maintenance Terminal
The maintenance terminal is included as a debugging and testing feature. Physically, it is the same port as the printer port. The printer port can be made to simulate a standard PDP-11 DL interface. When a terminal is connected to the port instead of a printer, accesses to the maintenance terminal addresses 17777560–17777566 function like the standard DL interface. In this mode, the port programs like a DL serial device with a receiver CSR, a receiver data buffer, a transmitter CSR, and a transmitter data buffer. Accesses to these registers when a terminal is not connected to the port result in reads of all 0s and writes that have no effect. Accesses to the printer port registers, 17773400–17773406 operate normally regardless of the device connected to the port.

Interrupts are not handled like a standard terminal DL. There are no interrupt enable bits in the CSR registers at locations 17777560 and 17777564. Interrupts must be enabled, disabled, and handled through interrupt controller 0 like the printer port interrupts. The vectors can be changed from the printer port vectors of 220 and 224 to the terminal vectors of 60 and 64 by reprogramming the response memory in interrupt controller 0 (see Section 5.4.6).

Hardware break detection can be enabled when a terminal is connected to the port. This allows the processor to halt into micro-ODT when the break key is depressed on the terminal. The hardware break detection has no effect if a printer is connected to the port.

The hardware determines that a terminal is connected to the port when pins 8 and 9 of the printer port connector, J6, are shorted. When using the port for a printer, a printer port cable (PN BCC05) should be used. The printer cable does not short pins 8 and 9. When using the port for a terminal, a terminal port cable (PN BCC08) should be used. The terminal cable shorts pins 8 and 9.

5.4.15.1 Maintenance Terminal Interface

Addresses

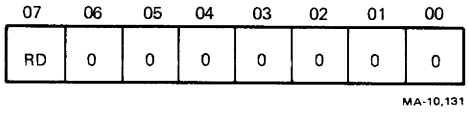
17777560	Receiver CSR
17777562	Receiver data buffer
17777564	Transmitter CSR
17777566	Transmitter data buffer

Vectors

220*	Receiver
224*	Transmitter

All four registers use only the low byte. Writes to high bytes have no effect and high bytes are read as all 0s. The operation of each terminal register is given below.

Receiver Control and Status Register (RCSR)



Bit 07 — RD – Receiver Done. This bit indicates that a character was received by the interface receiver. Each time a new character is received, the RD bit is set. RD is cleared by reading the receiver data buffer register or by a RESET.

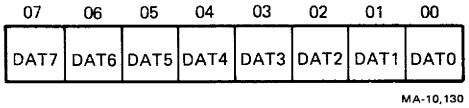
It is a read-only bit.

Bits 06–00 — They are not used and are always read as 0s.

They are read-only bits.

* Vectors of 60 and 64 can be obtained by programming interrupt controller 0. Interrupts on this port are not handled like a standard PDP11 DL (see description above).

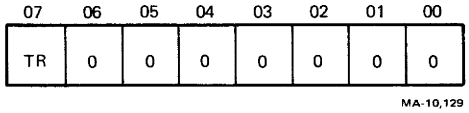
Receiver Data Buffer Register (RBUF)



Bits 07–00 DAT7–DAT0 – Data. This register contains the last received character. Reading the register clears RD. Writes to the register have no effect on the data in the register nor the RD bit.

They are read-only bits.

Transmitter Control and Status Register (XCSR)



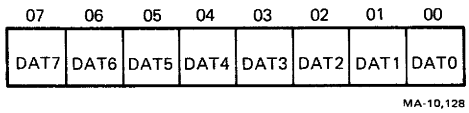
Bit 07 TR – Transmitter Ready. This bit indicates that the transmitter data buffer register is ready to be loaded with another character. Each time the transmitter data buffer is loaded, the TR bit is cleared. TR is set by a RESET or when the transmitter data buffer becomes ready.

It is a read-only bit.

Bits 06–00 They are not used and are always read as 0s.

They are read-only bits.

Transmitter Data Buffer Register (XBUF)



Bits 07–00 DAT7–DAT0 – Data. This register should be loaded with characters to be transmitted. Writing to the register clears TR. Reading the register returns unpredictable data and has no effect on the TR bit.

They are write-only bits.

5.5 CONNECTORS

There are 15 connectors on the Professional 350 system module (Table 5-21). Tables 5-22 – 5-29 show the pin connections for all but the CTI Bus connectors. Table 5-30 shows the connectors for jacks 10–15, the CTI Bus.

Table 5-21 System Module Connectors

Connector	Function
J1, J2	Memory boards
J3	Battery
J4	DC power
J5	Video/keyboard
J6	Printer
J7	Communication
J8	Remote access
J9	Network
J10–J15	CTI Bus options

Table 5-22 J1, J2 RAM Module Pin Location

Pin	Signal	Pin	Signal
1	+5.0 V	21	D08 H
2	MUXA 1 L	22	D15 H
3	+5.0 V	23	D09 H
4	MUXA 2 L	24	D14 H
5	GND	25	D10 H
6	MUXA 0 L	26	D13 H
7	GND	27	D11 H
8	MUXA 4 L	28	MUXA 6 L
9	GND	29	D12 H
10	MUXA 7 L	30	MUXA 5 L
11	GND	31	GND
12	MUXA 3 L	32	MUXA 8 L
13	D03 H	33	GND
14	D04 H	34	RCV WLB H
15	D02 H	35	GND
16	D05 H	36	RAS n L
17	D01 H	37	BANK n L
18	D06 H	38	CAS H
19	D00 H	39	Reserved
20	D07 H	40	RCV WHB H

Table 5-23 J3, Battery Back-Up

Pin	Signal
1	+3.6 V
2	GND

Table 5-24 J4, DC Power

Pin	Signal
1	BDCOK H
2	KEY
3	BPOK H
4	−12.0 V
5	+12.0 V
6	+5.0 V
7	+5.0 V
8	+5.0 V
9	+5.0 V
10	GND
11	GND
12	GND
13	GND
14	GND
15	GND
16	GND

Table 5-25 J5, Video/Keyboard

Pin	Signal
1	BLUE RETURN
2	GREEN RETURN
3	RED RETURN
4	MONO RETURN
5	GND
6	GND
7	+12.0 V
8	+12.0 V
9	BLUE VIDEO
10	GREEN VIDEO
11	RED VIDEO
12	MONO VIDEO
13	MON PRES L
14	KBD RDATA
15	KBD XDATA

Table 5-26 J6, Printer Port

Pin	Signal	CCITT V.24	EIA RS-232-C
1	PROTECTIVE GND	101	AA
2	TRANSMIT DATA	103	BA
3	RECEIVE DATA	104	BB
4			
5	DATA TERMINAL READY	108/2	CD
6	DATA SET READY	107	CC
7	SIGNAL GND	102	AB
8	GND		
9	TERMINAL L		

Table 5-27 J7, Modem Communications

Pin	Signal	CCITT V.24	EIA RS-232-C
1	PROTECTIVE GND	101	AA
2	TRANSMIT DATA	103	BA
3	RECEIVE DATA	104	BB
4	REQUEST TO SEND	105	CA
5	CLEAR TO SEND	106	CB
6	DATA SET READY	107	CC
7	SIGNAL GND	102	AB
8	CARRIER DETECT	109	CF
9			
10			
11			
12	SPEED MODE INDICATION	112	CI
13			
14			
15	TRANSMIT CLOCK (DCE)	114	DB
16			
17	RECEIVE CLOCK (DCE)	115	DD
18	LOCAL LOOPBACK	141	
19			
20	DATA TERMINAL READY	108/2	CD
21	REMOTE LOOPBACK	140	
22	RING INDICATOR	125	CE
23	DATA SIGNAL RATE SELECT	111	CH
24	TRANSMIT CLOCK (DTE)	113	DA
25	TEST INDICATOR	142	

Table 5-28 J8, Remote Access Connector

Pin	Signal
1	RAL 01
2	RAL 02
3	RAL 03
4	GND
5	RAL 04
6	RAL 05
7	+12.0 V*
8	RAL 06
9	RAL 07
10	GND
11	RAL 08
12	RAL 09
13	+5.0 V†
14	RAL 10
15	RAL 11
16	GND
17	RAL 12
18	RAL 13
19	−12.0 V*
20	RAL 14
21	RAL 15
22	RAL 16

* Line fused with 0.25A
† Line fused with 0.50A

Table 5-29 J9, Network (NET1)

Pin	Signal
1	SHIELD
2	COLLISION PRESENCE +
3	TRANSMIT +
4	
5	RECEIVE +
6	POWER RETURN (GND)
7	
8	
9	COLLISION PRESENCE −
10	TRANSMIT −
11	
12	RECEIVE −
13	POWER (+12.0 V)*
14	
15	

* Line fused with 0.50A

Table 5-30 CTI Bus Pin-Out and Signal Descriptions

General Section of the CTI Bus

Pin No.	Signal Name and Active State*	Transmit/ Receive†	Description
1	BDCOK H	R	DC voltage level OK (Section 5.3.2.5)
2	+5.0 V		
3	BPOK H	R	Sufficient voltage in power supply to run emergency power loss program
4	GND		
5	BINIT L	T	Initialize system on power up (Section 5.3.2.4)
6	−12.0V		
7	BDAL 15 L	T/R	Buffered data/address line (Section 5.3.3)
8	BDAL 13 L	T/R	Buffered data/address line (Section 5.3.3)
9	BDAL 14 L	T/R	Buffered data/address line (Section 5.3.3)
10	BDAL 12 L	T/R	Buffered data/address line (Section 5.3.3)
11	BSPARE 0		Reserved
12	BDAL 11 L	T/R	Buffered data/address line (Section 5.3.3)
13	BRPLY L	R	Reply (Section 5.3.3.1)
14	BDAL 10 L	T/R	Buffered data/address line (Section 5.3.3)
15	GND		
16	BDAL 09 L	T/R	Buffered data/address line (Section 5.3.3)

* B at beginning of signal name indicates a bused signal
† Transmit/receive with reference to the system module

Table 5-30 CTI Bus Pin-Out and Signal Descriptions (Cont)

General Section of the CTI Bus

Pin No.	Signal Name and Active State*	Transmit/ Receive†	Description
17	BMDEN L	T	Master drive enable (CPU puts data or address on bus (Section 5.3.3.1)
18	BDAL 08 L	T/R	Buffered data/address line (Section 5.3.3)
19	BWRITE L	T	Write (Section 5.3.9.1)
20	BDAL 07 L	T/R	Buffered data/address line (Section 5.3.3)
21	BWLB L	T	Write low byte (Section 5.3.9.1)
22	BDAL 06 L	T/R	Buffered data/address line (Section 5.3.3)
23	BWHB L	T	Write high byte (Section 5.3.9.1)
24	BDAL 05 L	T/R	Buffered data/address line (Section 5.3.3)
25	BSDEN L	T	Slave drive enable (slave device should put data on bus) (Section 5.3.3.1)
26	BDAL 04 L	T/R	Buffered data/address line (Section 5.3.3)
27	GND		
28	BDAL 03 L	T/R	Buffered data/address line (Section 5.3.3)
29	SS n L	T	Slot select (n = slot number) (Section 5.3.5.1)
30	BDAL 02 L	T/R	Buffered data/address line (Section 5.3.3)
31	IRQB n L	R	Interrupt request B from slot n (Section 5.3.6)
32	BDAL 01 L	T/R	Buffered data/address line (Section 5.3.6)

Table 5-30 CTI Bus Pin-Out and Signal Descriptions (Cont)

General Section of the CTI Bus

Pin No.	Signal Name and Active State*	Transmit/ Receive†	Description
34	BDAL 00 L	T/R	Buffered data/address line (Section 5.3.3)
35	OPRES n L	R	Option present in slot n (Section 5.3.4.2)
36	GND		
37	BDS L	T	Data strobe (Section 5.3.3.1)
38	+5.0 V		
39	BAS L	T	Address strobe (Section 5.3.3.1)
40	+12.0 V		
41	BSPARE 2		Reserved
42	BSPARE 3		Reserved
43	BIOSEL L	T	I/O select (Section 5.3.5.1)
44	BDAL 21 L	T/R	Buffered data/address line (Section 5.3.3)
45	BP 0 L	T/R	Bus priority level (Section 5.3.7)
46	BDAL 20 L	T/R	Buffered data/address line (Section 5.3.3)
47	BP 1 L	T/R	Bus priority level (Section 5.3.7)
48	BDAL 19 L	T/R	Buffered data/address line (Section 5.3.3)
49	BSPARE 1		Reserved
50	BDAL 18 L	T/R	Buffered data/address line (Section 5.3.3)
51	GND		

* B at beginning of signal name indicates a bused signal
† Transmit/receive with reference to the system module

Table 5-30 CTI Bus Pin-Out and Signal Descriptions (Cont)

General Section of the CTI Bus

Pin No.	Signal Name and Active State*	Transmit/ Receive†	Description
52	BDAL 17 L	T/R	Buffered data/address line (Section 5.3.3)
53	BMER L	R	Bus memory error (Section 5.3.2.5)
54	BDAL 16 L	T/R	Buffered data/address line (Section 5.3.3)
55	DMR n L	R	DMA request from slot n (Section 5.3.7)
56	DMG n L	T	DMA grant to slot n (Section 5.3.7)
57	BBUSY L	T/R	Bus busy (Section 5.3.7.1)
58	+5.0V		
59	BSPARE 4		Reserved
60	GND		

Private Section of the CTI Bus

The following connect to J8, remote access connector

61-76RAL 01-RAL 16

The following connect to J9, Network Connector (NET1)

77	TRANSMIT +	(J9 pin 3)
78	TRANSMIT –	(J9 pin 10)
79	RECEIVE +	(J9 pin 5)
80	RECEIVE –	(J9 pin 12)
81	COLLISION PRESENCE +	(J9 pin 2)
82	COLLISION PRESENCE –	(J9 pin 9)

Table 5-30 CTI Bus Pin-Out and Signal Descriptions (Cont)

General Section of the CTI Bus

Pin No.	Signal Name and Active State*	Transmit/ Receive†	Description
The following connect to J5, Video/Keyboard Connector			
83	RED RETURN		(J5 pin 3)
84	RED VIDEO		(J5 pin 11)
85	GREEN RETURN		(J5 pin 2)
86	GREEN VIDEO		(J5 pin 10)
87	BLUE RETURN		(J5 pin 1)
88	BLUE VIDEO		(J5 pin 9)
89	MONO RETURN		(J5 pin 4)
90	MONO VIDEO		(J5 pin 12)

* B at beginning of signal name indicates a bused signal
† Transmit/receive with reference to the system module

5.6 SPECIFICATIONS

The following paragraphs provide the specifications for the system module.

5.6.1 Physical Specifications

The following paragraphs provide the physical specifications of the system module.

5.6.1.1 Dimensions and Weight – The dimension and weight of the system module are as follows.

Length	40.0 cm (16 in)
Width	26.0 cm (10.4 in)
Height	2.25 cm (0.9 in) (without back panel and card cage)
	15.25 cm (6.1 in) (with back panel and card cage)
Weight	1.12K kg (2.5 lb) (with 2 memory boards installed) (approximate)

5.6.1.2 Module Interconnects – Figure 5-37 shows the position of all the connectors on the Professional 350 system module. Table 5-31 indicates the type and function of each connector. The pin location for each connector is listed in Section 5.5.

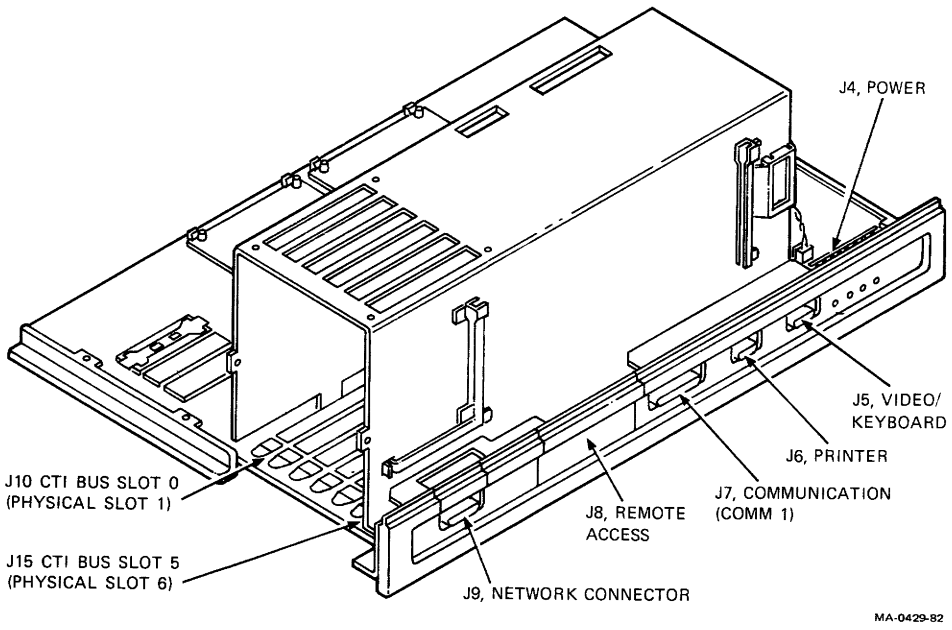


Figure 5-37 Connector Placement

Table 5-31 Connector Types

Connector	Function	Type
J1,J2	Memory boards	40-pin male
J3	Battery	2-pin male
J4	DC power	16-pin male
J5	Video/keyboard	15-pin male D-subminiature
J6	Printer	9-pin male D-subminiature
J7	Communication	25-pin male D-subminiature
J8	Remote access	22-pin finger receptacle
J9	Network	15-pin female D-subminiature
J10–J15	CTI Bus options	90-pin ZIF T-rail

5.6.2 Power Requirements

The following paragraphs provide the power requirements.

5.6.2.1 DC Power Requirements – The dc power requirements are as follows.

Voltage	Current Tolerance	Typical	Maximum
+12.0 V	+5%, −5%	320 mA	500 mA
+ 5.0 V	+5%, −5%	5.0 A	6.0 A
−12.0 V	+5%, −5%	60 mA	100 mA

(This data includes two 128 kilobyte memory modules but has no devices connected to any of the I/O ports.)

5.6.3 Environmental Specifications

The following paragraphs provide the environmental specifications.

5.6.3.1 Temperature – Operating and storage temperatures for the system module are as follows.

Operating
5°C (41°F) min
60°C (140°F) max

The temperature limits are specified as the free air ambient temperature around the module. See Section 5.6.3.4 for airflow and temperature requirements when the module is enclosed in the system box.

The maximum allowable operating temperature is reduced by 1.8°C per 1000 meters (1°F per 1000 feet) above sea level.

NOTE
The accuracy of the real time clock oscillator is ±0.002% over the temperature range of +10° to +50°C (50° to 122°F). Beyond these limits the clock still functions but the accuracy is degraded.

Storage
−40°C (−40°F) min
66°C (151°F) max

Before operating a module which is at a temperature beyond the operating range, that module must first be brought to an environment within the operating range and then must be allowed to stabilize for a reasonable length of time. (Five or more minutes depending on the air circulation.)

5.6.3.2 Relative Humidity – Operating and storage relative humidities are as follows.

Operating
10% min
95% max

The wet bulb temperature must not exceed 32°C (90°F) and the dew point must not be less than 2°C (36°F).

Storage
10% min
95% max

5.6.3.3 Altitude – Operating and storage altitudes are as follows.

Operating
50,000 ft (90 mm mercury) max

The maximum operating temperature must be derated at high altitudes (Section 5.6.3.1).

Storage
50,000 ft (90 mm mercury) max

The module is not mechanically or electrically damaged at altitudes up to 50,000 feet.

5.6.3.4 Operating Airflow – Adequate airflow must be provided to limit the inlet to outlet temperature rise across the module. When operating above 55°C (131°F), the outlet temperature must not exceed 65°C (149°F). When operating below 55°C (131°F), the inlet to outlet temperature rise must not exceed 10°C (18°F).

CHAPTER 6
PROFESSIONAL 380
SYSTEM MODULE

6.1 INTRODUCTION

This chapter describes the Professional 380 system module. The following introductory sections outline the chapter contents, all related documentation, and the hardware components of the system module.

NOTE
Refer to Table 6-21 in Section 6.5 for the names and definitions of all signals discussed in this chapter.

6.1.1 Chapter Organization

Chapter 6 is divided into five sections. Table 6-1 lists and describes these sections.

6.1.2 Related Documentation

Title	Document Number
KDJ11-C Field Maintenance Print Set	MP-01957-01
PDP-11/70 Processor Handbook	EB 05962 20/77 02 030 (08722)
Microcomputers and Memories	EB 20912 20/82

6.1.3 System Module Components

The following list describes all the primary components and features of the Professional 380 system module. Figure 6-1, a diagram of the system, identifies its primary components.

- J11 microprocessor with full memory management and floating point capabilities
- J11 microprocessor DC365 control gate array
- DC362 I/O interface gate array
- Video gate array and associated random access memory (RAM) and video generation logic
- Six-slot T-rail backplane to support the full CTI Bus and option modules
- System memory of 512 kilobyte dynamic RAM
- 16 kilobyte read-only memory (ROM) for initialization, configuration, and system boot code and self-test diagnostics

Table 6-1 Chapter Organization

Section	Title	Description
6.1	Introduction	This section describes the chapter and how it is organized, provides a list of related documentation, and lists all system module components.
6.2	Functional Description	This section describes the purpose of each major circuit within the system module. System level block diagrams are used to illustrate the discussion.
6.3	Detailed Description	This section provides a detailed description of the operation of each major circuit and corresponding support circuits to the primary signal level. Circuit block diagrams and timing flowcharts are used to illustrate this discussion.
6.4	Programming Information	This section presents information on all registers used by the system module. Bitmap illustrations and definitions are used to explain each register.
6.5	System Module Specifications	This section presents all the specifications associated with the system module.

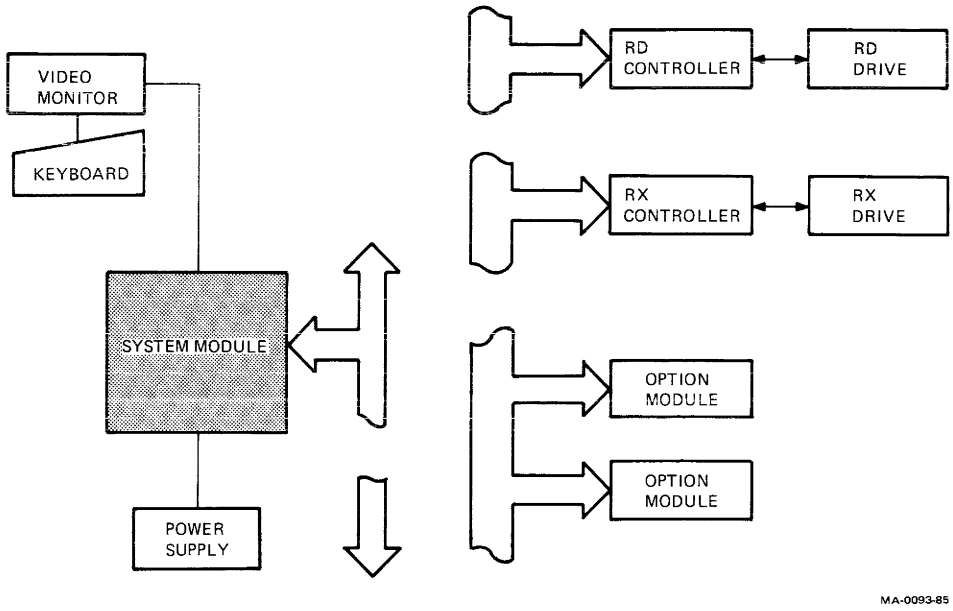


Figure 6-1 Professional 380 System Diagram

- Support of up to 1 megabyte of RAM with one optional one half a megabyte daughter module
- A full modem communications interface that supports both asynchronous and synchronous communications
- A printer interface that supports all Digital serial printers
- A video/keyboard combination interface that supports black and white and color video as well as keyboard interfacing
- A 22-pin auxiliary signal port to support the telephone management system (TMS) option
- Support of the extended bit map option daughter module
- Battery backed-up real-time system clock
- 22-bit ODT console emulator
- A 4-bit LED error display and a dc power OK LED
- A network interface (NI) port to support Ethernet activity

6.2 FUNCTIONAL DESCRIPTION

The following sections provide a functional description of the Professional 380 system module. The functionality of each major circuit group is described based upon a system-level block diagram. Refer to Figure 6-3, the Professional 380 system-level block diagram, when reading the functional description section.

6.2.1 J11 Microprocessor

The J11 microprocessor is a hybrid circuit that incorporates a PDP-11 processor with memory management and floating point functionality. It consists of two integrated circuits mounted on a 60-pin hybrid package, a data chip, and a base control chip. See Figure 6-2, the Professional 380 system module, for the location of the J11 microprocessor.

1. **Data Chip**
   The data chip contains the data path and relocation logic for the Professional 380. The data chip performs all arithmetic and logic functions. It contains a memory management unit and performs all data transfers and memory relocations. It also controls all signals used for system timing and interchip communication

2. **Base Control Chip**
   The base control chip contains the microprogram sequence logic and 1280 words of local program storage in the form of programmable logic arrays (PLA) and ROM arrays. The base control chip emulates the PDP-11 instruction set, the extended instruction set (EIS), and the FP-11 floating point unit instruction set

6.2.2 J11 Microprocessor DC365 Control Gate Array

The J11 microprocessor DC365 control gate array is the interface between the J11 microprocessor and the rest of the Professional 380 system. It contains the logic to perform the functions listed below. See Figure 6-2 for the location of the controller gate array on the system module.

1. Provides direct access to local memory

2. Generates bus timing signals

3. Performs bus arbitration between the J11 microprocessor and all direct memory access (DMA) devices

4. Provides power-up information for the J11 microprocessor

5. Contains logic used for single-stepping in micro ODT (on-line debugging technique)

6. Generates specific J11 service routine conditions

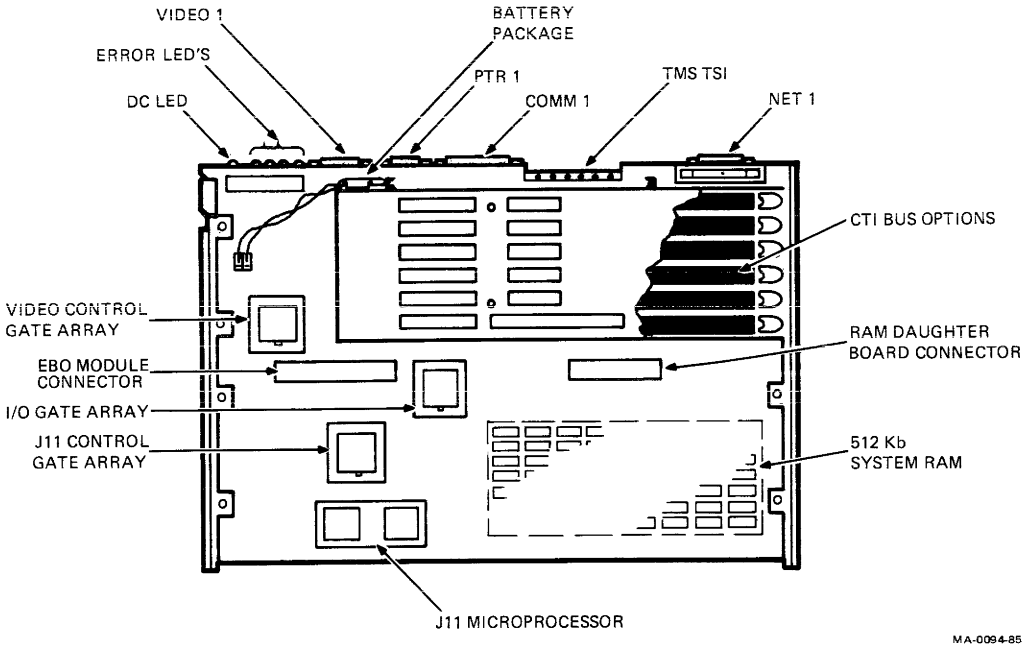


Figure 6-2 Professional 380 System Module

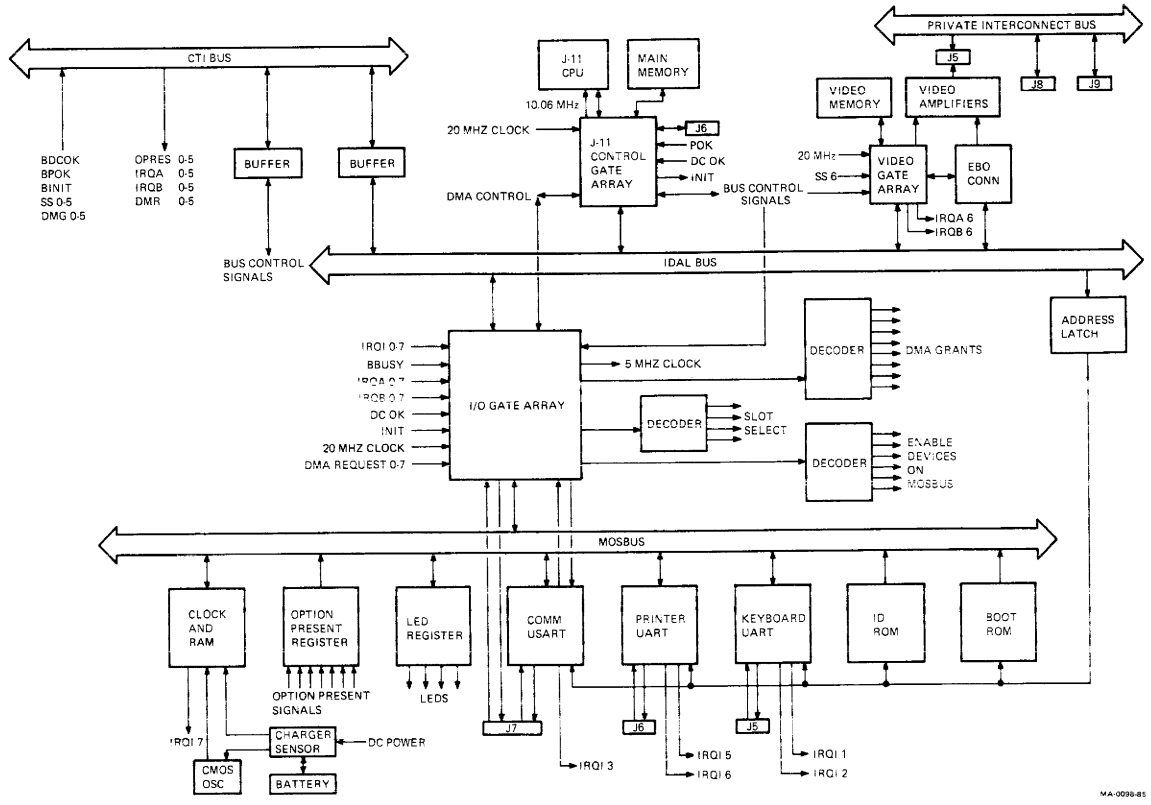


Figure 6-3 Professional 380 System Module Block Diagram

6.2.3 DC362 I/O Interface Gate Array

The DC362 I/O interface gate array provides a path to the local I/O devices connected to the system module. It handles all system interrupts and arbitrates all DMA activity occurring over the Bus. The I/O gate array performs the functions listed below. See Figure 6-2 for the location of the I/O gate array on the system module.

1. Acts as an address decoder to aid in the selection of slot selection; local I/O devices, interrupt controllers, modem registers, baud rate register, and console register

2. Provides an interface for the J11 to the boot ROM

3. Provides a baud rate clocking signal to the printer and keyboard universal synchronous/asynchronous receiver/ transmitter (USART) circuits

4. Contains logic to support all communication interface logic functions

5. Controls all system interrupts

6. Controls all DMA device requests for the CTI Bus

7. Controls the direction of the CTI Bus buffers

8. Contains support logic for the maintenance terminal mode

9. Provides a maintenance status register

6.2.4 System Memory

System memory for the Professional 380 consists of two memory device areas: the read only memory (ROM) and the local random access memory (RAM).

1. **16 Kilobyte Diagnostic/Boot ROM Memory**
   The Professional 380 contains 16 kilobytes of memory in a ROM device. ROM memory contains the power-up self-test code, configuration and initialization codes, and the boot loader code. The programs (firmware) in ROM test the system when powering on the Professional 380 and load the operating system software.

2. **RAM Memory**
   The system module contains 512 kilobytes of RAM memory using 64 64K × 1 dynamic RAM integrated circuit chips. This is expandable up to 1 megabyte by installing the optional RAM daughter board onto the system module.

   Figure 6-2 shows the location of RAM, ROM, and the RAM daughter board connector on the system module.

6.2.5 Real-Time System Clock

The real-time system clock keeps track of the date and time whether the system is on or off. The clock circuit is implemented by a CMOS device integrated circuit. A rechargeable nickel-cadmium battery maintains the clock circuit operation when the system is not powered on. Figure 6-2 shows the location of the real-time system clock on the system module.

6.2.6 Printer Interface Logic

The printer interface logic provides a connection to the Professional 380 system for a serial Digital printer. The primary circuit is a universal synchronous/asynchronous receiver/transmitter (USART) circuit. The printer logic performs asynchronous serial communications at programmable baud rates of up to 19.2 kilobaud. Figure 6-2 shows the location of the printer interface logic on the system module.

6.2.7 Keyboard Interface Logic

The keyboard interface logic provides a connection to the Professional 380 system for the Professional 380 keyboard. Again, the primary circuit is a USART circuit. The keyboard logic communicates in asynchronous serial mode at programmable baud rates of up to 19.2 kilobaud.

6.2.8 Communication Interface Logic

The Professional 380 implements a port that supports RS-423 communications. The communication interface logic uses a USART as its primary circuit. In asynchronous mode, it can support communications at programmable baud rates of up to 19.2 kilobaud. In synchronous mode, it can support communications at programmable baud rates of up to 740 kilobaud. Figure 6-2 shows the location of the communication interface logic on the system module.

6.2.9 Video Generation Integrated Logic

The video generation integrated logic consists of the video gate array, video amplifiers, support logic for the extended bit map option daughter module, and 16 64K $\times$ 1 dynamic RAM chips. Figure 6-2 shows the location of the video generation integrated logic on the system module.

6.2.10 LED Display Circuit

The LED display consists of five LEDs located on the rear of the system module. The display indicates power and error conditions in the Professional 380 computer system. Figure 6-2 shows the location of the LED display on the system module.

6.2.11 CTI Bus Option Connectors

The CTI Bus option connectors are an integral part of the system module. Each option slot of the card cage has a 90-pin zero insertion force (ZIF) connector mounted directly on the system module. The first 60 pins route all CTI Bus signals. The last 30 pins route signals from the option modules to the connectors on the rear of the system module. Figure 6-2 shows the location of the CTI Bus option module connectors on the system module. Refer to section 6.5, System Module Connectors, for a listing of all connectors on the system module.

6.2.12 System Power-On Bootstrap Sequence

The following sections describe the power-on and bootstrap sequences of the Professional 380 computer system. Any operations beyond those described here are dependent upon the operating system and application program(s) and are beyond the scope of this document.

1. **Power-On Sequence** – When power is applied to the Professional 380, the power cycling sequence causes an initialization of all device parameters, with the exception of the battery backed-up RAM and clock circuits. The J11 does a read and instruction fetch at the starting location of the 16 kilobyte diagnostic/boot ROM upon receiving an "indicated safe operating voltage" (DCOK) from the power supply. The DCOK LED on the rear of the system module will light when DCOK is active.

   This is the start of the self-test. Each device of the Professional 380 computer system is tested. The device parameters are loaded into a configuration table in RAM and each device is initialized for operation (assuming there are no error conditions found during the self-test). Self-test errors will be reported to the operator through LED display and with error message displayed on the monitor. The Professional 380 system is initialized for operation once the power-on sequence has been successfully completed.

2. **Bootstrap Sequence** – The bootstrap sequence occurs in three phases: primary, secondary, and tertiary.

   a. **Primary Phase** – The Professional 380 searches each slot in the CTI Bus card cage for a removable media device, starting with slot 1. Each time one is found it tries to boot it into the system. If a device cannot be booted, it goes on to the next slot until all slots have been tried.

   b. **Secondary Phase** – The Professional 380 will attempt to boot whatever device (according to its ID number) is found in the battery backed-up RAM. The information in the battery backed-up RAM is proven valid or invalid by applying an error checking sequence to it. The system will then attempt to boot those devices identified. If no boot device was found or if a device cannot be booted, the Professional 380 goes on to the last sequence.

   c. **Tertiary Phase** – The third sequence searches each slot in the card cage looking for any bootable device. The system will continue the tertiary phase until a bootable device is found or all slots have been tried for all devices in the Professional 380 system. If no boot was was found or initialized, the system will display a floppy diskette with a question mark next to it and repeat the entire three-phase sequence.

6.3 DETAILED DESCRIPTION

The following sections describe each major circuit on the system module to the primary signal level. Each circuit description is supported with illustrations, timing diagrams, and component block diagrams as needed. Refer to the *KDJ11-C Field Maintenance Print Set* when reading this section.

NOTE

Refer to Figure 6-3, Professional 380 system module block diagram, for the system module detailed descriptions.

6.3.1 J11 Microprocessor Overview

The J11 is a 16-bit microprocessor that uses VLSI technology to implement PDP-11 architecture.

1. **Internal Data/Information Paths**
   It contains a 32-bit wide internal data path to optimize floating point operations. A four-level deep instruction prefetch pipeline that uses four internal high speed controllers enables the J11 to perform instruction-stream memory references and internal instruction executions simultaneously. It contains an internal prefetch buffer memory that buffers data between the J11 and external memory. Figure 6-4 shows the internal data paths of the J11 microprocessor.

2. **Internal Register Layout**
   The J11 contains two groups of 16-bit per internal registers that are used for temporary data storage: general purpose and special registers. These registers are used as accumulators, index reference, autoincrement and autoexcrement, and stack pointers. Refer to Section 6.4 for descriptions of the Professional 380 register sets.

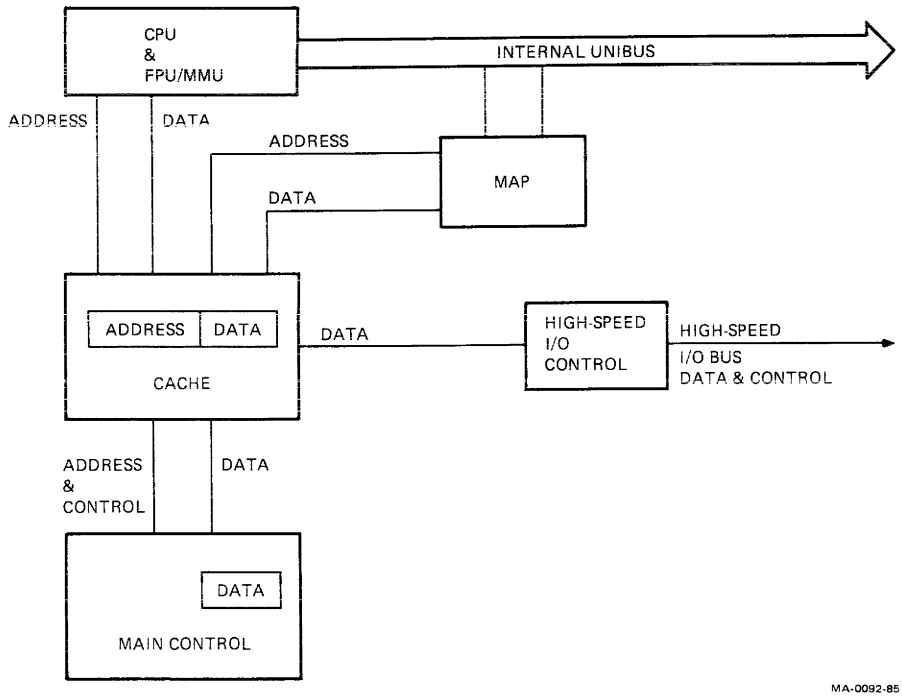


Figure 6-4 J11 Internal Data/Information Path

3. **Data Chip**
The data chip is composed of three integral logic units: an execution unit (EU), a memory management unit (MMU), and a prefetch mechanism. The EU contains the J11 register set and multiplexers. The MMU contains all memory management logic, floating point accumulators, and error status registers. The prefetch mechanism contains a prefetch buffer and status flagging logic.

The data chip performs all arithmetic and logic functions, handles all data transfers and address relocations, and operates all interchip communication and timing signals.

4. **Base Control Chip**
The base control chip contains the microprogram logic and local storage using programmable logic arrays (PLA) and ROM arrays. The control chip emulates the PDP-11 instructon set, the extended instruction set (EIS), the floating point instruction set, and the console microcode (ODT).

The control chip accesses the correct sequential instruction, during an instruction cycle, from internal cache memory and sends it to the data chip over the microinstruction bus (MIB). It will simultaneously generate the address for the next sequential instruction to be executed by the data chip.

6.3.1.1 Memory Management Unit – The J11 uses the PDP-11/70 memory management unit (MMU) integrated in the data chip. The MMU implements address relocation and protection logic to enable the J11 to execute internal and external instruction cycles simultaneously.

The J11 accesses 64 kilobytes of memory at a time which allows 64 kilobytes of program data per instruction fetch to be available to the microprocessor at any given time during program execution. To do this, a 16-bit program virtual address (VA) is converted to a 22-bit physical address (PA). The high order 256 kilobyte addresses are used by the J11 to address the internal microinstruction bus. The remaining 3,840 kilobyte addresses access a physical main memory. If an address is in the top 256 kilobytes of the 22-bit physical address, the lower 18 bits of the address are placed on the internal J11 bus. An internal J11 bus map converts that 18-bit address back to a 22-bit physical address. This structure enables the J11 to address up to 4 megabytes of memory.

Figure 6-5 shows how the MMU converts a 16-bit VA to a 22-bit PA. For detailed information on memory management techniques, refer to *Microcomputers and Memories.*

6.3.1.2 Floating Point Unit – The J11 implements the FP11-C floating point unit is an integral part of the base control chip. The FP11-C provides both single precision (32-bit) mode or double precision (64-bit) mode.

Figure 6-6 illustrates how the floating point interacts with the J11 microprocessor. For detailed information concerning the FP11-C floating point unit, refer to *Microcomputers and Memories.*

6.3.2 Instruction Cycle Timing

The J11 performs bus read and write transactions during each program instruction. Each transaction requires a minimum of four to eight clock cycles. An AIO (address I/O) code is used to identify the type of transaction. Any given read or write may be extended beyond its normal clock period in increments of two to four clock cycles. This allows a transaction to be extended as long as necessary, determined by the transaction taking place. Table 6-2 identifies all AIO codes generated by the J11.

This section describes only the microprocessor bus read and write transactions.

Table 6-2 J11 Transaction Identification Codes

AIO Codes				Transaction
3	2	1	0	
1	1	1	1	Non-I/O
1	1	1	0	General purpose read
1	1	0	1	Interrupt acknowledge
1	1	0	0	Instruction stream request read
1	0	1	1	Read-modify-write/no Bus lock
1	0	1	0	Read-modify-write/Bus lock
1	0	0	1	Data stream read
1	0	0	0	Instruction stream demand read
0	1	1	1/0	Reserved
0	1	0	1/0	General purpose word-write
0	0	1	1/0	DAL Bus byte-write
0	0	0	1/0	DAL Bus word-write

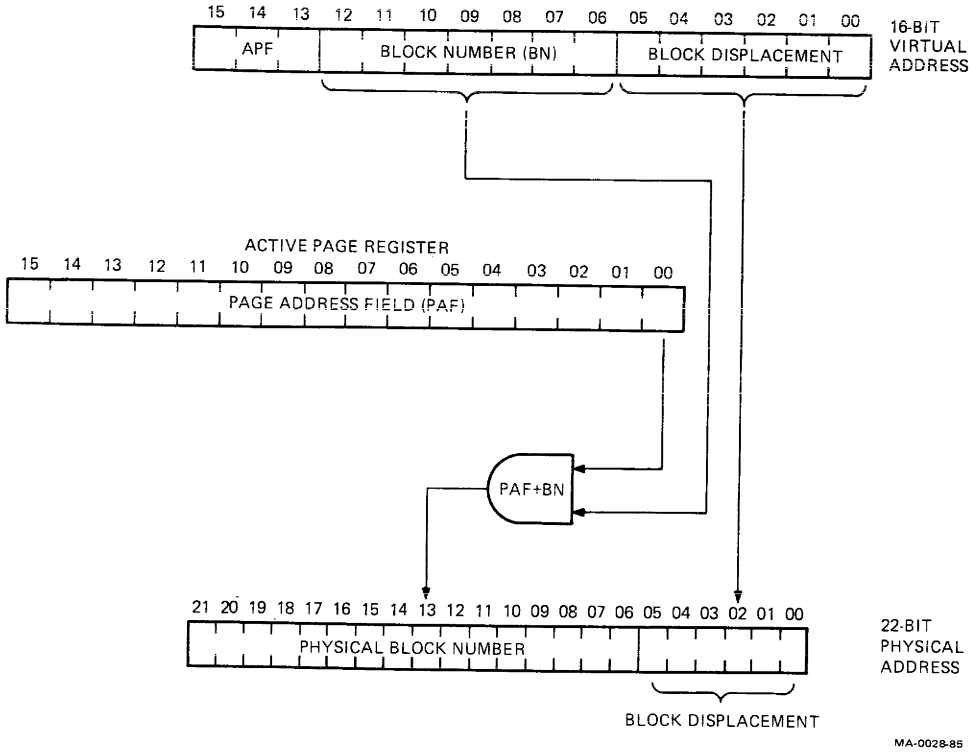


Figure 6-5 J11 Memory Management Data Flow

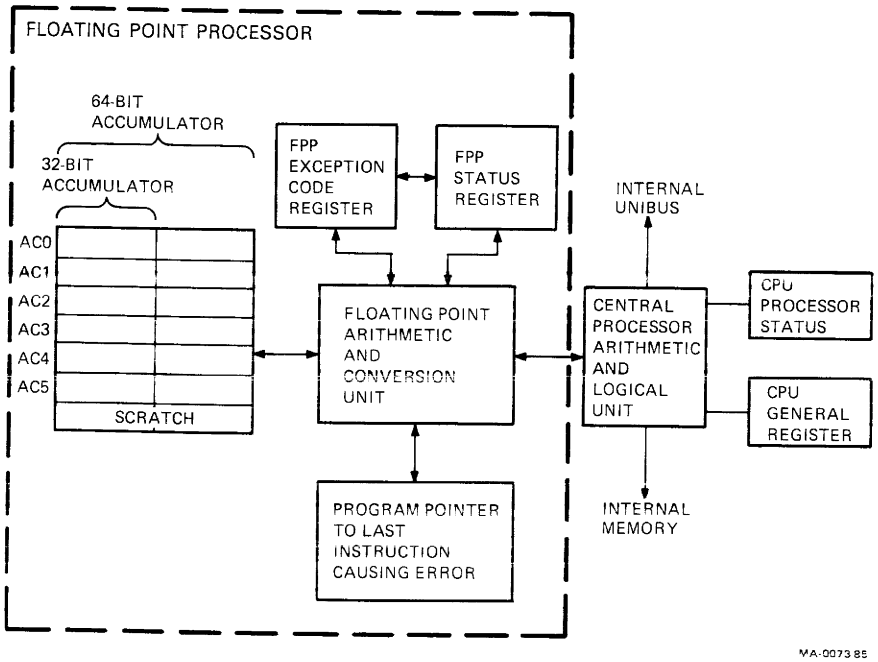


Figure 6-6 FP11-C Floating Point Interaction

6.3.2.1 Read Timing – The J11 uses the DC365 control gate array (Figure 6-2) to access data from memory, I/O, and other devices attached to the system module. The J11 initiates a read transaction by asserting ALE (address latch enable). ALE enables the J11 to generate the following codes to the control gate array.

1. AIO (address I/O – defines the type of read transaction)
2. The physical address of the device being read from
3. BS1,0 data (defines the type of device being read from)
4. MAP (I/O map enable)

The J11 reads the data on the rising edge of T3 during a non-stretched transaction. The J11 normally completes a bus read in four time periods.

During a stretched bus read, the BUFCTL (buffer control) and SCTL (stretch control) signals are asserted. The J11 will read the data when it receives a DV (data valid) signal. The stretched bus read will continue in increments of two time periods until the J11 receives a CONT (continue) from the control gate array ending the read transaction.

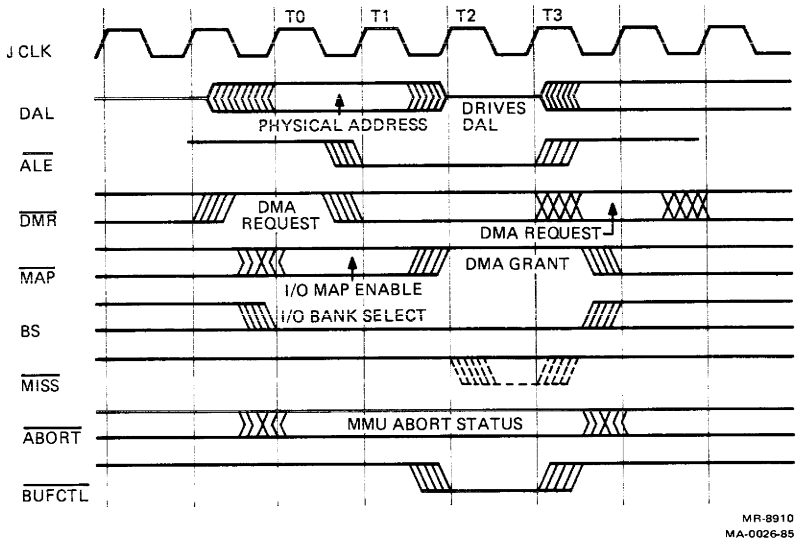
The J11 handles any memory management or addressing errors by stopping the bus transaction. It stops a bus read by asserting the signal ABORT to the control gate array. Bus parity errors also assert ABORT back to the J11.

Figure 6-7 shows the timing diagram for a bus read transaction.

6.3.2.1.1 General Purpose Read Timing – A general purpose read transaction is initiated when the J11 asserts STRB. STRB latches the address on the DAL Bus. This enables the J11 to latch the AIO code and a general purpose read code of the device being read.

The data is read during the assertion of SCTL and after the J11 has received DV (data valid) from the device being read. The transaction will continue until the control gate array sends a CONT to the J11 signifying the end of the general purpose read.

Figure 6-8 shows the timing diagram of a general purpose read transaction.



NOTE
T0, T1, T2, AND T3 ARE NOT EQUAL IN TIME.

Figure 6-7 Bus Read Transaction (600 ns)

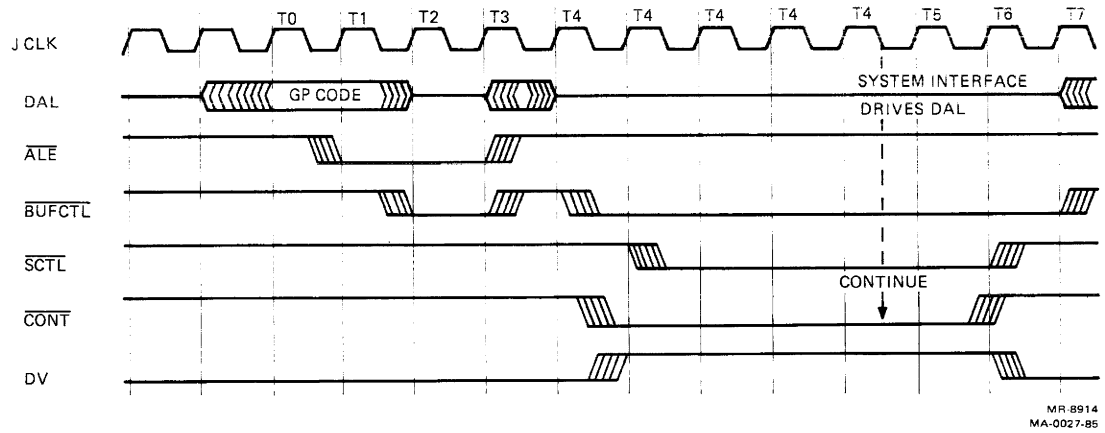


Figure 6-8 General Purpose Read Transaction (1000 ns)

6.3.2.2 Write Timing – The J11 initiates a write transaction by asserting ALE (address latch enable). ALE enables the J11 to generate the following codes to the control gate array.

1. AIO (address I/O – defines the type of write transaction)
2. The physical address of the device being written to
3. BS1,0 data (defines the type of device being written to)
4. MAP (I/O map enable)

During a stretched bus write, SCTL is asserted. The J11 will write the data to the chosen device between the leading and trailing edges of SCTL. The stretched bus write will continue in increments of two time periods until the J11 receives a CONT (continue) from the control gate array ending the write transaction.

The J11 handles any memory management or addressing errors by stopping the bus transaction. It stops a bus write by asserting ABORT to the control gate array.

Figure 6-9 shows the timing diagram of a bus write transaction.

6.3.2.2.1 General Purpose Write Timing – A general purpose write transaction is initiated when the J11 asserts ALE to the control gate array. This enables the J11 to latch the AIO code and a general purpose write code of the device being written to. The data is written during the assertion of SCTL. The transaction will continue until the controller gate array sends a CONT to the J11 signifying the end of the general purpose write.

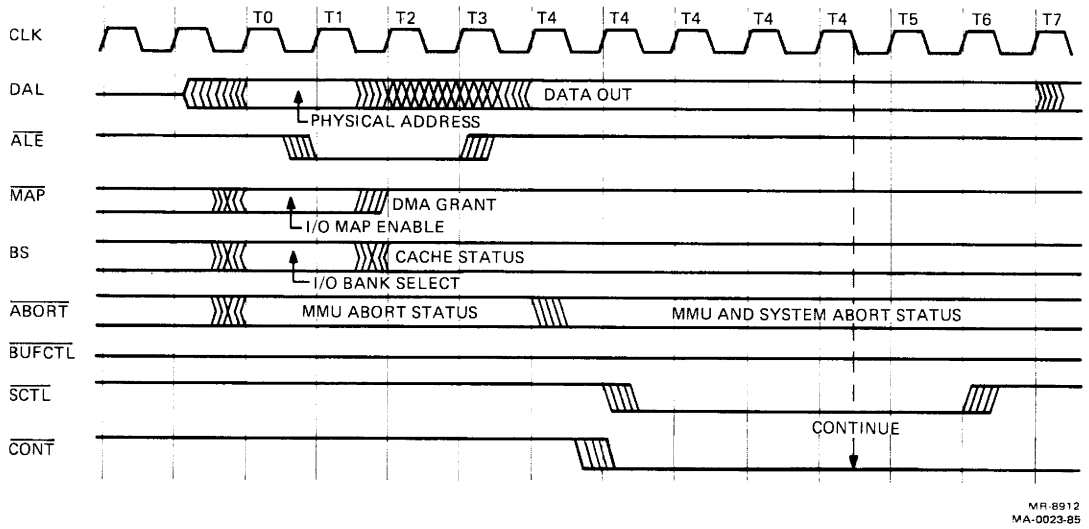


Figure 6-9 Bus Write Transaction

Figure 6-10 shows the timing diagram of a general purpose write transaction.

6.3.2.3 Interrupt Acknowledge Timing – The J11 initiates an interrupt acknowledge (on internal CTI Bus) transaction whenever it receives an interrupt request on its IRQ H interrupt input. It then branches to a vector address to service the interrupt. The AIO code and a decoded-interrupt-level-acknowledged signal is driven to the control gate array from the DAL 3–0 outputs.

The interrupt acknowledge transaction requires a minimum of eight time periods to complete and can be stretched by increments of two time periods until the control gate array generates CONT to the J11 completing the interrupt acknowledge transaction.

Figure 6-11 shows the timing diagram of an interrupt acknowledge transaction.

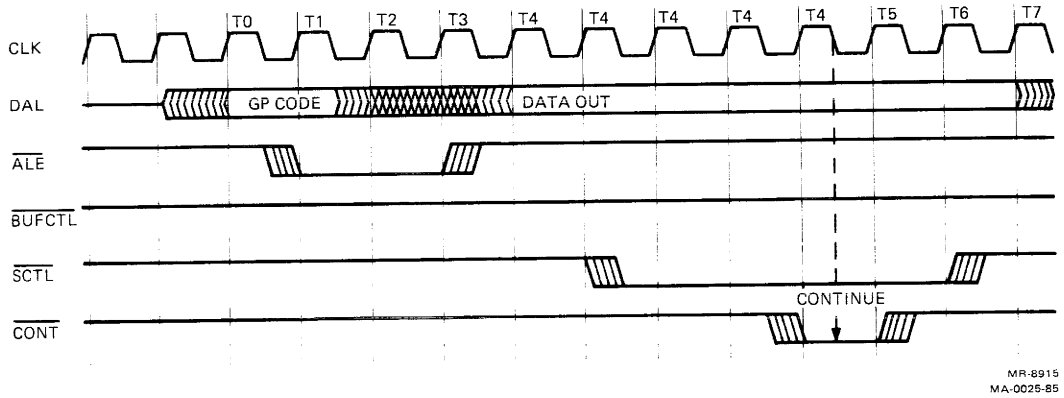


Figure 6-10 General Purpose Write Transaction

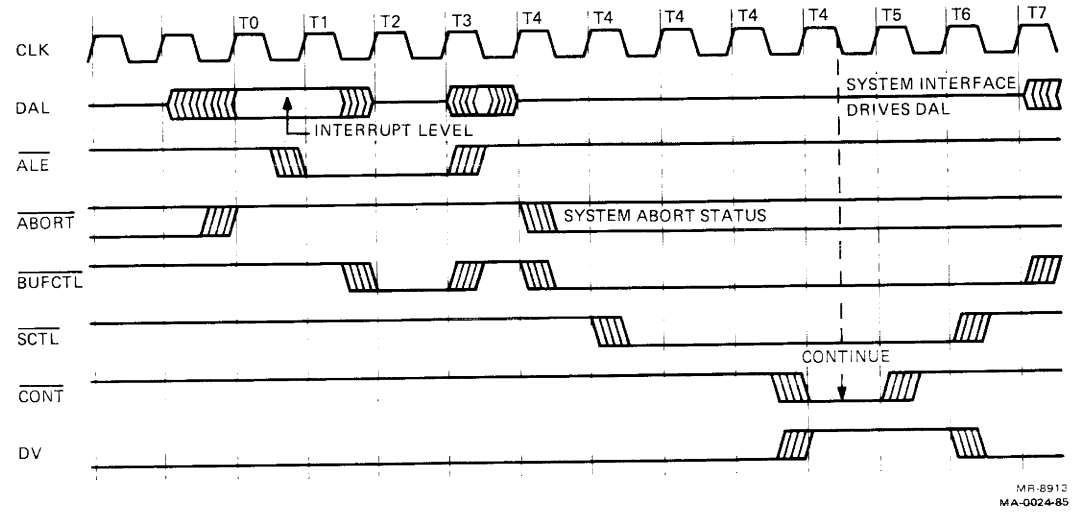


Figure 6-11 Interrupt Acknowledge Transaction

6.3.2.4 DMA (Direct Memory Access Timing) Request and Grant Timing – The CTI Bus and the system module allow for DMA option modules. A DMA device requests the bus from the J11 by asserting its DMA request line, DMR n L. The DMA device becomes the bus master when it receives a grant from the I/O gate array on its DMA grant line, DMG n L. DMA devices monitor the bus DMA priority lines, BP 0 L and BP 1 L, and are granted bus access only if they are at a higher priority level than the DMA device currently occupying the CTI Bus.

The DC365 control gate array arbitrates bus access between the DMA devices that are requesting the bus and the J11. DMA devices always have priority over the J11 and will be granted the bus as soon as the processor completes any bus cycle already in progress.

During a DMA cycle, the I/O gate array asserts a signal to reverse the direction of the control signals on the CTI Bus. When multiple DMA devices at a particular DMA priority level are simultaneously requesting the bus, the arbiter will grant bus access to the one in the lowest numbered slot (i.e., slot 1 before slot 3).

If a DMA device does not assert the BUS BUSY signal in response to its grant within the allowable time stated in the CTI Bus specification, the DC365 will remove the grant and continue. The control gate array arbitrates for the local memory between refresh cycles, DMA devices, and the J11 CPU (listed in highest to lowest priority). The J11 may access local memory in between any refresh or DMA bus access cycle. Refer to the *CTI Bus Technical Manual* for information on direct memory accessing.

6.3.3 J11 Microprocessor DC365 Control Gate Array

The DC365 control gate array is a 120-signal pin gate array contained in a 145-pin package and provides the interface between the J11 microprocessor and the rest of the Professional 380 system.

The DC365 is structured to respond to various sequences of input signal transitions provided by the J11 and other devices on the system module. The following sections describe the DC365 logic on a functional level and how it interacts with the Professional 380 computer system.

The DC365 contains logic to excute the following functions:

1. Handles accessing to local memory by the J11 microprocessor or any DMA devices
2. Generates bus timing signals when the J11 accesses devices on the CTI Bus
3. Arbitrates access to the CTI Bus between the J11 and DMA devices
4. Provides power-up information for the J11
5. Acts as the system CSR
6. Is the SSODT register for single stepping in ODT
7. Generates the following J11 service conditions:
   a. HALT on break detect from console terminal
   b. HALT from SSODT register
   c. PWRFL L (Power fail) interrupt
   d. PRITY L (Parity) abort from bus data
   e. ABORT L for bus time-out or in conjunction with PRITY L.
8. Responds to the following J11 transactions:
   a. Interrupt acknowledge
   b. Bus INIT assertion and deassertion.

6.3.3.1 DC365 Bus Cycle Interaction – The DC365 synchronizes data flow between the J11 and the rest of the Professional 380 system J11 during a bus cycle transaction.

The J11 starts a bus transaction by:

1. generating a valid physical address, general purpose code, or interrupt acknowledge level to the control gate array,

2. asserting BS1-0, and

3. asserting AIO3-0.

STRB L going high signals the beginning of a J11 transaction and initiates timing chains in the DC365 that handle each type of J11 cycle. STRB L asserting high causes a J11 machine state counter to start.

NOTE

The machine state counter generates internal J11 time periods associated with specific machine cycles designated as JSTATES.

When STRB L is asserted, The DC365 latches data from the J11 BS and AIO lines. A DC365 internal comparator uses the jumper data from the local memory modules (read during refresh cycles) to determine if the current J11 address accesses a local memory bank or other device. The results of the comparison combined with the BSx, AIOx, and MYSTRB codes cause one of the following states to occur:

1. generate an access request to the local memory,
2. generate an access request to the CTI Bus state machine,
3. wait for SCTL time to do a GP read or write, or
4. generate a NOP (a "no operation" cycle).

6.3.3.2 Memory Read/Write Transaction – Memory read requests are always asserted at the beginning of JSTATE4 (internal occurs at beginning of every cycle). The J11 clock is stalled by the DC365. This prohibits any other operation to execute when obtaining data from local memory. Write requests are always asserted at the beginning of JSTATE3 (internal).

The DV L input to the J11 controls its internal data latch. Whenever a read cycle starts, DV L is negated high. When the data arrives, DV L is asserted low to preserve the data.

The J11 generates BFCTL L when a read cycle is going to be initiated. Read cycles to local memory will cause BFCTL L to pulse once. Other read cycles will because BFCTL L to pulse twice. The DC365 asserts CONT L to the J11 ending the cycle.

Write cycles are stretched until the J11 is finished writing data to the selected device and CONT L is asserted to end the write cycle.

NOTE

CONT L is asynchronously cleared every time JSTATE4 (memory read request) is entered. GP internal cycles cause CONT L to be asserted as soon as SCTL L asserts. Aborted cycles also assert CONT L until the beginning of the next J11 machine cycle.

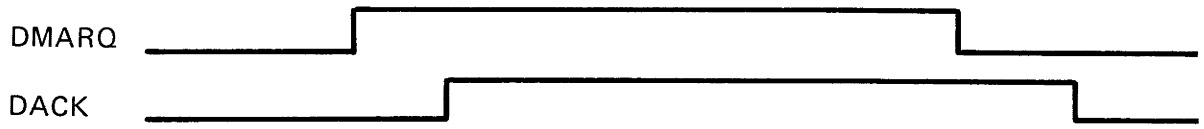
6.3.3.3 CTI Bus/DC365 Accessing – The J11 asserts WANTBUS at the beginning of JSTATE6 if the transaction is for a device on the CTI Bus or for a DC365 internal register. J11 cycles which access the CTI Bus or a DC365 internal register have bus priority to prevent delay in address comparison for other bus cycles.

6.3.3.4 General Purpose Read/Write Transaction – When the J11 does an internal or GP read/write, then CONT L is set asynchronously when SCTL is asserted. CONT L is cleared at the beginning of JSTATE4 on the next cycle. Only one GP read transaction must be accounted for. This occurs when the J11 does a GP 000 read to obtain the power-up status information. This data is gated to the inputs of the DAL output drivers with GFDIN2C. DV L is controlled asynchronously by SCTL during a GP read. GFDIN2C (internal) ensures that the required data set-up and hold times are met. The J11 DAL lines are only driven while BUFCTL from the J11 is asserted. A GP write is just like a GP read except that DV L is not asserted.

6.3.3.5 Interrupt Acknowledge Transaction – When an interrupt acknowledge cycle is initiated, the J11 assumes complete mastership of the DAL bus and generates IAKCYC. This signal is similar to WANTBUS (internal) and is generated when the J11 wants the DAL Bus. IAKCYC remains asserted until the vector reading starts. DS is asserted without AS to signal an interrupt acknowledge cycle to the DC362. The DC362 I/O interface gate array will reply in time for the IAK cycle to complete within 1400 – 1600 nanoseconds.

6.3.3.6 DMA Device Bus Accessing – DMA devices request mastership of the bus by asserting DMRx. The DC362 I/O interface gate array prioritizes these requests while asserting DMARQ to the DC365 controller gate array. If the J11 is not using the bus, then DACK is asserted which allows the DC362 to assert the appropriate DMG (DMA grant) line.

The following diagram shows the timing relationship of DMARQ to DACK.



Once DMARQ is asserted by the DC362, it will not deassert until DACK asserts. If the DMA device removes its request on the DMRx line, the DC362 will ensure that DMARQ stays high until DACK is asserted. DACK will remain asserted as long as DMARQ is asserted.

6.3.4 DC362 I/O Interface Gate Array

The DC362 I/O interface gate array is a 3200-gate HCMOS technology gate array. It handles all system interrupts, arbitrates DMA activity, and provides an interface between the CPU and all I/O devices on the Professional 380 system module.

The I/O gate array performs the following functions.

1. Provides the data path to the local I/O devices
2. Decodes addresses to perform the following functions:
   a. select slots
   b. select local I/O devices
   c. select interrupt controllers
   d. select modem registers
   e. select baud rate register
   f. select console registers
3. Performs Boot ROM sequencing
4. Provides support logic for the communications port
5. Provides a baud rate clock to the printer and keyboard USARTs
6. Controls all interrupts
7. Controls all DMA arbitration by:
   a. prioritizing DMA requests
   b. arbitrating with the DC365 for the bus mastership
   c. and generating all DMA grants
8. Controls the direction of the CTI Bus buffers
9. Performs emulation of a standard DL interface on the printer port for the maintenance terminal
10. Provides a maintenance status register

6.3.4.1 DC362 Bus Cycle Interaction – The DC362 gate array outputs information onto the IDAL Bus and the MOS Bus. The IDAL Bus is 22-bits wide and channels addresses and data between the I/O interface and control gate arrays. The MOS Bus is 8-bits-wide and channels addresses and data to the local I/O devices.

The J11 microprocessor begins a bus cycle by driving a 22-bit address to the DC365 control gate array. The DC365 drives the 22-bit address onto the IDAL Bus and asserts the IOSEL L line. The I/O interface gate array decodes the address information to determine if local I/O devices or internal registers are being accessed. It then channels the decoded address on lines IDAL08–IDAL01 onto MOS Bus lines MOSB7–MOSB0.

During a read transaction from the DC362 or during an interrupt acknowledge cycle, the DC362 array drives 16 bits of data onto IDAL15–IDAL00.

The I/O gate array first receives the 8-bit high byte and then the 8-bit low byte. Both are assembled into a 16-bit word that is placed on IDAL15–IDAL00. If a local I/O device is being read, the device being read channels the 8-bit data to the DC362 over the MOS Bus.

During a write transaction to the I/O interface gate array, only the data on IDAL07–IDAL00 is used. If an internal register was addressed, the data on IDAL07–IDAL00 is written into the register. If a local I/O device was addressed, the data on IDAL07–IDAL00 is placed on the MOS Bus. Write cycles are write-word or write-low-byte cycles. Write-high-byte cycles are ignored.

6.3.4.2 Address Decoding – The DC362 decodes a bus address on every bus cycle to determine if a local I/O device or internal register is being accessed. If an internal register is addressed, the DC362 gate array will generate an internal strobe signal to the appropriate register. If a local I/O device is addressed, the DC362 will generate a 3-bit code which represents the local device selected. The 3-bit code is output on the SMOS2–SMOS0 lines to enable the selected I/O device.

The following TYPE code list defines the codes in the "TYPE" column in Table 6-3. These codes define the type of address associated with each device addressed by the DC362.

TYPE Code List
R/W=address may be read or written
R/T=address is read-only, writes cause a timeout trap
R/=address is read-only, writes are ignored
0/W=address is write-only, read as all 0s
0/=read as all 0s, writes are ignored

Table 6-3 shows the addresses that are recognized by the I/O interface gate array, the device associated with the address, what type of address as defined by the above TYPE code list, and the SMOS2–SMOS0 codes that are generated.

Table 6-3 DC362 Device Addressing Chart

Address	Device	SMOS2-0	Type
17700000–17767776	28 Kb of boot ROM space	7	R/T
17773000–17773176	TOD clock IC	0	R/W
–17773200	reserved	n/a*	0/
–17773202	CSR/interrupt controller 0	n/a*	0/W
–17773204	reserved	n/a*	0/
–17773206	CSR/interrupt controller 1	n/a*	0/W
–17773210	reserved	n/a*	0/
–17773212	CSR/interrupt controller 2	n/a*	0/W
17773300–17773306	comm USART	3	R/W
–17773310	modem control register 0	n/a*	R/W
–17773312	modem control register 1	n/a*	R/T
–17773314	baud rate register	n/a*	0/W
17773400–17773406	printer USART	4	R/W
17773500–17773506	keyboard USART	5	R/W
17773600–17773676	ID PROM	6	R/T
–17773702	option present register	1	R/T
–17773704	LED display register and maintenance status register	2	R/W
–17777560	console RCSR/TERM L low	n/a*	R/
–17777562	console RBUF/TERM L low	4	R/
–17777564	console TCSR/TERM L low	n/a*	R/
–17777566	console TBUF/TERM L low	4	0/W
17777560–17777566	console registers/TERM L high	n/a*	0/

* These addresses are for the DC362 internal registers.

Address 17774000–17775776 is the address range within which opton modules on the CTI Bus are detected. The DC362 I/O interface gate array asserts ENASS L when this range is decoded. Address lines 9–7 combined with ENASS L are used to generate the slot select lines on the CTI Bus.

An external address latch provides address lines for the communication USART, keyboard USART, ID PROM, and boot ROM. The TOD clock receives address information from the MOS Bus. The printer USART receives address information from the IOA1–IOA0 lines.

6.3.4.3 Boot ROM Sequencing – When the I/O gate array detects a boot ROM address, it starts an internal sequencer and asserts ROM address line 0. The ROM is enabled when the DC362 outputs ROM code 7 on SMOS2–SMOS0 and asserts the ENAMOS L line. The ROM drives the high byte onto the MOS Bus.

NOTE

The DC362 does two 8-bit byte-wide reads from the boot ROM and outputs a 16-bit word to the J11. This accomodates the 8-bit ROM and 8-bit-wide MOS Bus. The ROM contains alternating low bytes and high bytes. A sequencer in the DC362 is used to control the ROM read.

When ROM access time has elapsed, the DC32 sequencer inputs the high byte on the MOS Bus to an internal register. ROMA0 is cleared after this sequence to allow access to the low byte. The same process is done for the low byte.

When ROM access time has elapsed again, the DC362 sequencer passes the latched high byte onto IDAL15–IDAL08 and the low byte from MOSB7–MOSB0 to IDAL07–IDAL00. It also generates a bus REPLY signal to the J11. At the completion of the bus cycle, the DC362 sequencer is reset.

6.3.4.4 Communication Port Support Logic – The DC362 I/O interface gate array contains logic to support modem controls for the kernal communication port. It also contains logic to select the communication USART clocks and maintenance loopback mode. There are two internal registers for handling the modem control signals and selecting the mode of operation. A third register selects the baud rates of the internal baud rate generators. Detection logic samples signal transitions on four modem lines and generates an interrupt (IRQ4 L) to the first interrupt controller.

6.3.4.5 Baud Rate Generators – The DC362 I/O interface gate array contains two baud rate generators used for the communication port. One is used for the communication port USART receiver and one for the communication port USART transmitter. The two generators are identical in their operation.

The internal generators supply one of 16 baud rates under program control. A 4-bit code in a baud rate generator register selects the desired frequency. All frequencies are derived by dividing the 20.16 MHz CLKI (clock in) signal. This signal is divided by two and the derived 10.08 MHz signal is used to clock a counter to generate the selected baud rate frequency.

The I/O gate array also outputs a clock signal (CLKO) that is used as the baud rate for the printer and keyboard USARTs. CLKO is derived by dividing 20.16 MHz by 4 to yield a clock rate of 5.04 MHz.

6.3.4.6 Interrupt Controller Logic – The DC362 I/O interface gate array uses three interrupt controllers to handle the 21 system interrupts. The first interrupt controller handles all interrupts generated by devices not on the CTI Bus. The second interrupt controller handles all the "A" interrupts from the CTI Bus modules. The third controller handles all CTI Bus module "B" interrupts.

The interrupt controllers latch the interrupt requests, provide the interrupt enables for each request, prioritize all pending interrupts, and generate the proper vectors. The I/O gate array interrupts the J11 microprocessor at processor status level 4 via the IRQ H signal.

The interrupt controllers can handle a total of seven interrupts requests at any given time. Interrupt controller 0 commands the highest priority and interrupt controller 2 commands the lowest.

The interrupt requests are received at request levels 0–6 (1 to 7 for interrupt controller 0). Request level 0 is the highest priority and request level 7 is the lowest priority.

Table 6-4 shows the interrupts that are handled by each controller. The table presents each interrupt vector, description, and interrupt name for each of interrupt controller in the DC362 I/O interface gate array.

Table 6-4 DC362 Interrupt Listing

Controller	Request Level		Vector*	Interrupt Description	Name
	0	0	234	TOD clock	IRQ7 L
	0	1	200	keyboard receiver	IRQ1 L
highest	0	2	204	keyboard transmitter	IRQ2 L
priority	0	3	210	communication port	IRQ3 L
	0	4	214	modem controls change	N/A**
	0	5	220	printer receiver	IRQ5 L
	0	6	224	printer transmitter	IRQ6 L
	0	7	230	TOD clock	IRQ7 L
	1	0	300	slot 0/IRQA	IRQA0 L
	1	1	310	slot 1/IRQA	IRQA1 L
	1	2	320	slot 2/IRQA	IRQA2 L
	1	3	330	slot 3/IRQA	IRQA3 L
	1	4	340	slot 4/IRQA	IRQA4 L
	1	5	350	slot 5/IRQA	IRQA5 L
	1	6	360	slot 6/IRQA	IRQA6 L
	2	0	304	slot 0/IRQB	IRQB0 L
	2	1	314	slot 1/IRQB	IRQB1 L
lowest	2	2	324	slot 2/IRQB	IRQB2 L
priority	2	3	334	slot 3/IRQB	IRQB3 L
	2	4	344	slot 4/IRQB	IRQB4 L
	2	5	354	slot 5/IRQB	IRQB5 L
	2	6	364	slot 6/IRQB	IRQB6 L

* These vectors are fixed in hardware.
** This interrupt is generated internally in the gate array.

6.3.4.7 Direct Memory Access (DMA) Arbitration – The I/O interface gate array arbitrates bus mastership between the J11 microprocessor and all DMA devices. The DMA logic consists of a state machine, a 6-bit latch, a 6- to 3-bit priority encoder, and a 3-bit latch.

A DMA device requests bus mastership by asserting a DMA request signal, DMRn L. Any number of DMA request signals may be asserted at the same time. The DMRn L signals go through the open six bit latch to the priority encoder.

The priority encoder sends a signal to the DMA state machine to indicate that a DMA device is requesting the bus and to start the appropriate timing sequence.

The state machine begins by asserting a master DMA request to the DC365 control gate array on the DMARQ line. This causes the J11 microprocessor to complete any active bus cycle and relinquish bus mastership to the requesting DMA device(s).

When the DC365 returns DACK H (DMA acknowledge signal) to the DC362, the state machine ensures that the priority encoder has generated the 3-bit code representing the number of the pending highest priority DMA request. This 3-bit code is latched onto the DMG2–0 L lines.

The state machine then generates ENAGR L. This enables the DC362 external logic to assert a DMA grant signal to the requesting device in the slot indicated by the code present on the DMG2–0 L lines. During the grant pulse, the state machine opens the 6-bit latch to allow the next DMA arbitration cycle to begin.

The DMA device that received the grant must assert the BUSY L signal to inform the state machine that it has become the bus master. If BUSY L is received, the state machine waits for the DMA device to drop BUSY L before proceeding. If BUSY L is not received within a specific time, the state machine will end that grant and proceed to the next DMA device.

The state machine will continue granting and monitoring the BUSY L line until there are no more pending DMA requests. It then deasserts DMAMAS L and DMARQ signal to the J11. Once DMARQ has been deasserted, it will not be asserted again until the DC365 has deasserted DACK H.

6.3.4.8 Buffer Direction Control – The I/O gate array generates three signals for controlling the direction of the CTI Bus buffers: XMIT L, RCV L, and DMAMAS L.

The DC362 requires the input signal INTERNAL L to be asserted before it can control the buffer directions. INTERNAL L is asserted by any device on the system module that is being addressed. This informs the DC362 whether a system module device or a CTI Bus device is being accessed.

XMIT L is asserted to cause the IDAL Bus to be driven onto the BDAL Bus. This is done when one of the following conditions is present:

1. the J11 microprocessor is bus master and MDEN L is asserted, or

2. a DMA device is bus master and SDEN L is asserted and INTERNAL L is asserted.

RCV L is asserted causing the BDAL Bus to be driven onto the IDAL bus. This is done when one of the following conditions is present:

1. the J11 microprocessor is bus master and SDEN L is asserted and INTERNAL L is not asserted and it is not an IAK cycle, or

2. a DMA device is bus master and MDEN L is asserted.

When the J11 microprocessor is the bus master, the J11 microprocessor generates the bus control signals and are driven out to the CTI Bus. When a DMA device is the bus master, that device must generate the bus control signals. DMAMAS L is asserted by the DC362 during DMA transactions so the system module will receive the bus control signals. The DC362 gate array does not assert DMAMAS L when the J11 microprocessor is bus master. In this case, the Professional 380 system module generates all bus control signals.

6.3.4.9 Maintenance Terminal Logic – The DC362 I/O interface gate array contains circuitry to enable the printer port program to emulate a standard PDP-11 DL interface.

When TERM L is high, the gate array responds to the maintenance terminal addresses 17777560–17777566. All the registers are read as 0s and writes to the registers have no effect. When TERM L is low, the gate array responds to the maintenance terminal addresses like a DL serial device.

6.3.5 System Memory

The following sections describe the system memory components of the Professional 380 System Module.

6.3.5.1 Random Access Memory (RAM) – The system module implements two groups of local RAM memory.

1. System Module-Resident RAM
   The system module contains 512 kilobytes of RAM. This consists of sixty-four 64K × 1 dynamic RAM integrated circuit chips.

2. RAM Daughter Module
   The daughter module provides up to 512 kilobytes using 256K × 1 RAM integrated circuit chips. The RAM daughter module plugs into a 48-pin connector on the system module. The daughter module uses 40 pins on the connector. The remaining 8 pins may be used for future memory expansion daughter modules.

A private address/data bus channels data between the DC365 controller gate array and RAM. This allows the J11 to continue executing out of main memory while an external DMA device is using the IDAL Bus. The DC365 controller gate array can support up to 2 megabytes on the system module and up to 2 megabytes on a daughter board, with a maximum of 3 megabytes total.

Table 6-5 shows the varying address ranges and memory sizes of the system module when using either system module-resident RAM, the daughter board module, or both.

NOTE

Whichever memory (system module or daughter board) contains more space will have an address range beginning with address 00000000. If the memory sizes are equal, the system module memory space will begin with address 00000000.

The DC365 controller gate array provides the circuitry for address decoding and multiplexing, for timing, and for cycle refresh.

Table 6-5 Professional 380 Memory Configuration

Memory Size/Board	Total Memory	Address Range/Board
512 Kb on system module 0 Kb on daughter board	512 Kb	00000000–01777777 none
512 Kb on system module 128 Kb on daughter board	640 Kb	00000000–01777777 02000000–02377777
512 Kb on system module *256 Kb on daughter board	768 Kb	00000000–01777777 02000000–02777777
512 Kb on system module 512 Kb on daughter board	1.24 Mb	00000000–01777777 02000000–03777777
*512 Kb on system module 1 Mb on daughter board	1.54 Mb	04000000–05777777 00000000–03777777
*512 Kb on system module 2 Mb on daughter board	2.56 Mb	10000000–11777777 00000000–07777777

* These configurations are not available from Digital.

6.3.5.2 Read Only Memory (ROM) – The system module contains one 16K × 8 ROM chip that provides 16 kilobytes of read only memory. It contains the power-up self-test code, configuration and initialization code, and the boot code. The ROM address space is distributed through two areas as shown in the list below.

Address Range	Size	Location
17730000–17757777	12 kilobytes	memory space
17760000–17767777	4 kilobytes	I/O page

Figure 6-12 shows the relationship of the ROM address mapping scheme to the 22-bit system addressing scheme.

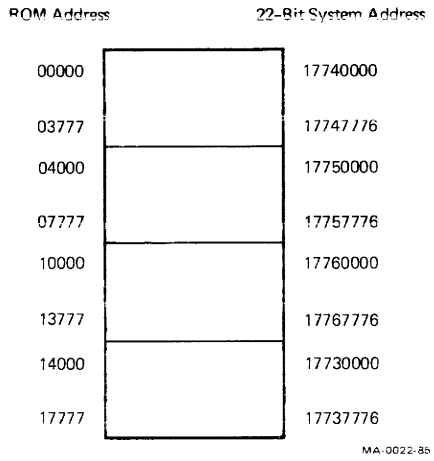


Figure 6-12 ROM Address Mapping Scheme

A memory read to the boot ROM is controlled by the I/O interface gate array. A word read is done by doing by two consecutive byte reads to the ROM over the MOS Bus. The resulting word is output onto the IDAL Bus by the I/O gate array.

6.3.5.3 Identification Programmable Read Only Memory (PROM) – The system module contains a 32-byte ID PROM. Each individual system module has a unique ID PROM. The ID code is a 12 BCD digit (6 byte) random number.

6.3.6 Printer Port Interface

The printer I/O interface is a serial port on the system module that performs asynchronous serial communication to and from a serial printer. The printer interface uses a 2661 enhanced programmable communication interface (EPCI). The EPCI is an enhanced USART containing its own I/O buffers and shift registers for controlling asynchronous character protocol.

Parallel data is taken from the IDAL Bus and converted into serial data to transmit to the printer. Simultaneously, it converts serial data from the printer into parallel data for processing by the J11 microprocessor.

The printer port logic uses a 5.0688 MHz clock for baud rate generation. The transmit and receive baud rates are programmable by the J11. The printer port is capable of performing asynchronous serial communications at programmable baud rates up to 19.2 kilobaud.

The printer port interface is also used as an input for a maintenance terminal console. The normal printer cable connector does not short these pins. The short pulls the line low, enabling break detection by the CPU. A received break asserts the J11 halt line (HALT H) to the J11 via the service register. This makes the J11 enter micro-ODT (octal debugging technique) for maintenance and system level troubleshooting.

Connection is made on the rear of the system module via a 9-pin male D-subminiature connector, J6.

6.3.7 Keyboard Port Interface

The keyboard port interface is a serial port on the system module that performs asynchronous serial communication to and from a serial keyboard. The keyboard interface uses a 2661 enhanced programmable communication interface (EPCI). The EPCI is an enhanced universal synchronous/asynchronous receiver/transmitter (USART) containing its own I/O buffers and shift registers for controlling asynchronous character protocol.

The EPCI converts parallel data characters from the IDAL Bus into serial data for transmission to the keyboard. At the same time, it converts serial data from the keyboard into parallel data for J11 processing.

The I/O signals to the keyboard are sent and received through the video/keyboard connector, J5. The EPCI uses a 5.0688 MHz clock for a 4800 baud rate generation. The transmit and receive baud rates are programmable by the J11.

The following signal lines are used to channel data to and from the keyboard.

1. KBD XDATA – Keyboard Transmit Data
2. KBD RDATA – Keyboard Receive Data

The EPCI requires standard EIA RS-423 signal levels and uses standard receivers and drivers for input and output. Keyboard connection to the system board is via a 15-pin male D-subminiature connector, J5.

6.3.8 Communication Port Interface

The communication port interface is a serial communication port that implements a 7201 USART containing its own I/O buffers and shift registers. It is capable of operating in asynchronous mode at split programmable baud rates up to 19.2 kilobaud and in synchronous mode up to 740 kilobaud.

The communication port interface can operate with asynchronous and synchronous (bit or byte) protocols. It also contains a full set of modem controls for asynchronous communication. The J11 selects transmit and receive baud rate clocks. Transmitted data feeds back into the received data line but is ignored except when in maintenance mode. When this happens, received data is ignored until the modem control register is cleared (at power up or by a reset instruction) or written with new data.

The communications port interface asserts two interrupts.

1. The first interrupts the J11 if the USART chip requires receiver or transmitter service.

2. The second interrupt indicates that a state change has occurred on one of four modem control signals: ring indicator, data set ready, clear to send, and carrier detect.

   A baud rate generator selects the clock speed for the USART. The modem controls used for asynchronous communication are also used to monitor all modem status signals.

3. Baud Rate Generator – A programmable baud rate generator (BRG) generates a 5.0688 MHz clock signal for the USART. The I/O page address decoder selects the BRG. Refer to Section 6.4 for a definition of the communication port registers that control the selection of the the clock and transmit/receive baud rates.

4. Modem Controls – The modem control signals connect directly to the IDAL. Bus through a buffer enabled by the I/O page address decoder. A exclusive-or circuit compares the modem signals' states clocked in on PHASE time with their status on the previous PHASE time. If any of the states change, an interuppt is generated. The J11 reads the interrupt from the IDAL Bus by addressing the modem control registers through the I/O page address decoder.

   All the port signals are EIA RS-423 levels. Connection is made on the rear of the unit via a 25-pin male D-subminiature connector, J7.

6.3.9 Video Generation Integrated Logic

The video generation integrated logic consists of the video gate array, sixteen 64K × 1 dynamic RAMs, video generator, and connector circuitry for the extended bit map option (a 64-pin connector).

Video memory appears as 64K words (128 kilobytes) in the J11 address space and provides one plane of displayable data. The analog-to-digital converters for all three planes. One plane resides on the system board and two reside on the EBO the module.

Video logic registers appear to the J11 microprocessor as "logical" slot six in the backplane. When the video gate array ROM address register is written to (address 17775402), the data resident in the identification register (ID0–ID7 lines) is transferred to the low byte of the J11 IDAL inputs.

The following list shows the three identification codes for the video generation integrated logic configurations.

1. ID 50 (octal) – EBO is not present.
2. ID 10050 (octal) – EBO is present.

6.3.10 Battery Backed-Up RAM

The battery backed-up RAM stores 50 bytes of data. The RAM is implemented in the MC146818 real-time system clock integrated circuit. The back-up is achieved with the use of a rechargeable NiCD battery. Battery power is supplied to the system module via connector J3.

The battery is continuously charging when the system is powered on. When power is shut off, the battery supplies power to RAM to maintain data integrity. A charged battery will maintain RAM data for a minimum of 10 days while the system is powered off. The battery will be completely charged after 48 hours of continuous system power-on time.

6.3.11 Real-Time System Clock

The real-time system clock keeps track of the date and time even when the system is powered off. The clock is implemented with an MC146818 CMOS integrated circuit. Power off back-up is achieved with the use of a rechargeable NiCD battery. Battery power is supplied to the system module via connector J3.

The battery is continuously charging when the system is powered on. When power is shut off, the battery supplies power to the clock to continuously update time and date.

A completely charged battery will maintain clock operation for a minimum of 10 days while the system is powered off. The battery will be completely charged after 48 hours of continuous system power-on time.

The clock IC can be programmed to interrupt the J11 at a specified alarm time or at a periodic rate. The periodic rate can be programmed to one of 13 frequencies from 2 Hz to 8.192 kHz. There is no line time clock. The clock will keep accurate time to within one minute per month.

6.3.12 LED Display Circuit

The LED display is located on the back edge of the system module and is used by the system to display various system messages. Figure 6-13 shows the arrangement of the LEDs as viewed from the back of the unit.

There are five LEDs on the back of the system module. The green one is lit to indicate the assertion of the DCOK signal from the power supply.

The four red LEDs are used as error indicators by the power-up self test. At power-up, all four red LEDs are lit. The LEDs will flash slowly in different patterns while executing self-test. When self-test has passed successfully, all LEDs are not lit. If any LEDs remain lit, there is an error. Table 6-6 indicates the error condition for each LED code.

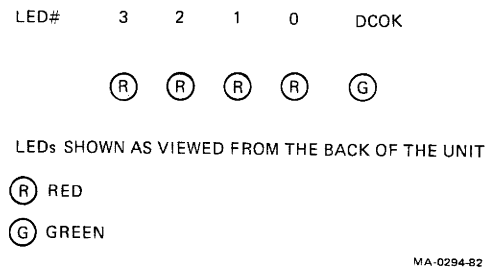


Figure 6-13 LED Display

Table 6-6 LED Error Codes

LED 3	LED 2	LED 1	LED 0	System Status
off	off	off	off	System module passed self-test
off	off	off	on	Error: Option module slot 1
off	off	on	off	Error: Option module slot 2
off	off	on	on	Error: Option module slot 3
off	on	off	off	Error: Option module slot 4
off	on	off	on	Error: Option module slot 5
off	on	on	off	Error: Option module slot 6
off	on	on	on	Invalid: Reserved
on	off	off	off	Invalid: Reserved
on	off	off	on	Keyboard failure
on	off	on	off	No bootable device found
on	off	on	on	Monitor not present
on	on	off	off	Memory modules slots 0 and 1 failed
on	on	off	on	Memory slot 1 failed self-test
on	on	on	off	Memory slot 0 failed self-test
on	on	on	on	System module failed self-test

6.3.13 CTI Bus Option Module Connectors

The CTI Bus backplane is part of the system module. The backplane is designed to accept option modules using a ZIF (zero insertion force) connector. Six option module slots are provided.

Each option slot has a 90-pin ZIF connector on the system module. The first 60 pins are used for the CTI Bus signals.

NOTE

Refer to the CTI Bus Technical Manual, EK-00CTI-TM-002, for a detailed description of how the CTI Bus operates. This manual can only be ordered by signing a license agreement.

Pins 61 through 90 are used to route signals from the option modules to connectors on the rear of the system module. An option module that only requires CTI Bus signals can use a 60-pin ZIF connector. An option module that uses the rear connectors on the system module must implement a 90-pin ZIF connector. All CTI Bus signals are bussed through all six option module slots with the exception of six signals.

The six non-bussed signals, listed below, provide slot dependent signals to the system module for handling address decoding, interrupts, and DMA.

Signal*	Definition
OPRES n L	Option present indicator
SS n L	Slot select from address decoder
IRQA n L	Interrupt request A from option
IRQB n L	Interrupt request B from option
DMR n L	DMA request from option
DMG n L	DMA grant from arbiter

* n = slot number (0–6)

Each option module has 128 bytes allocated in the I/O page. The system module decodes the addresses and asserts a slot select to the appropriate option module.

DMA devices may address the option modules. The system module decodes the address output by the DMA device and asserts a slot select to the appropriate option module.

6.4 PROGRAMMING INFORMATION

This section describes the register programming for the Professional 380 system module. It contains information on how to access internally programmed J11 functions and support devices on the system module. It does not contain information on high level application programming.

6.4.1 J11 Register Set Overview

The J11 microprocessor implements PDP11 architecture for high speed efficient real-time applications. The J11 uses a 22-bit address path and resident memory management to address up to 4 megabytes of memory. A 32-bit-wide internal data path and a four-level deep internal prefetch pipeline enables instruction stream references to be overlapped with internal operations.

This section provides a general description of the J11 register set. Section 6.4.6.6 provides detailed descriptions of the J11 register set.

General Purpose

There are two groups of 16-bit general purpose registers, R0–R5 and R0′–R5′ (Figure 6-14, J11 Register Architecture). These are used as accumulators, index reference, auto increment, auto decrement, and stack pointers for temporary data storage.

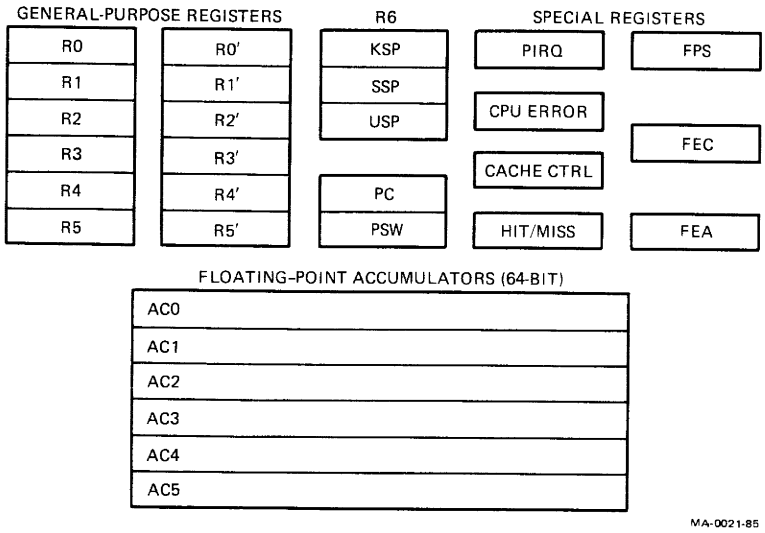


Figure 6-14 J11 Register Architecture

Special Purpose
A group of special purpose registers are used for specific functions. Refer to Section 6.4.1.6 for individual detailed register definitions.

1. CPU error register (CPU ERROR)
2. Program interrupt request register (PIRQ)
3. Cache control register (CCR)
4. Hit/miss register (HMR)
5. Processor maintenance register
6. Processor status word (PSW)

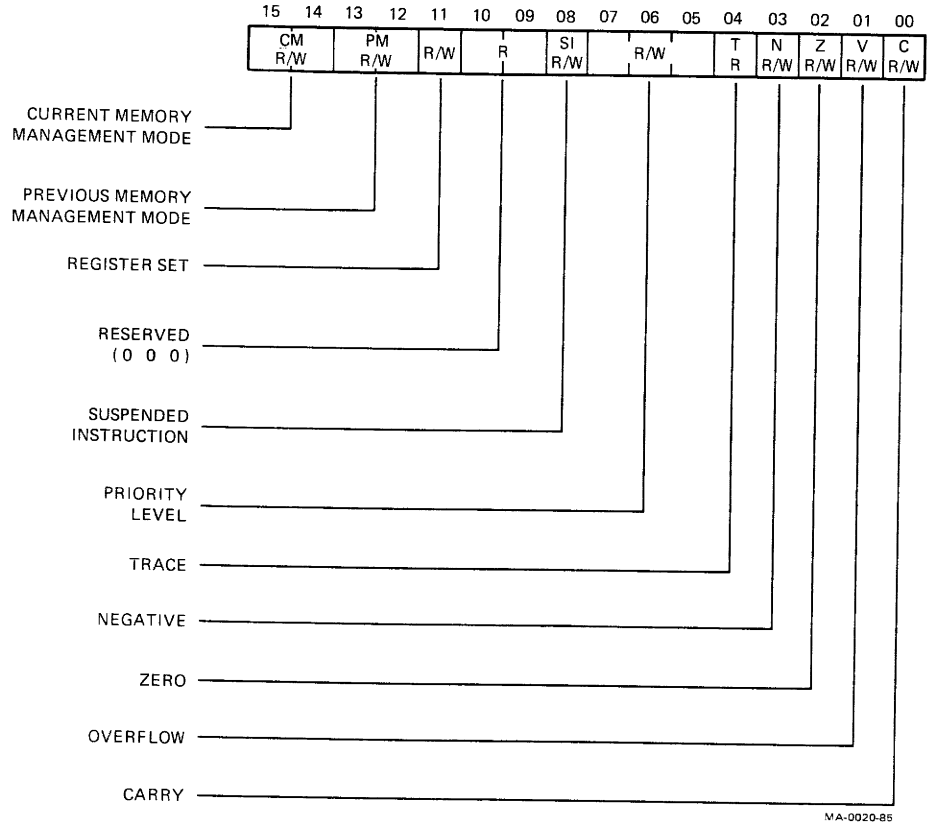
Stack Pointers
The J11 microprocessor uses three dedicated 16-bit stack pointers designated as R6 (Figure 6-14, J11 Register Architecture) to control its three operating modes: kernel (KSP), supervisor (SSP), and user (USP). These are used to store the current processor status information during a hardware interrupt or trap. Refer to Section 6.4.1.1 for individual detailed register definitions.

6.4.1.1 J11 Register Set – Addresses are as follows.

17777746	Cache control register
17777750	Processor maintenance register
17777752	Hit/miss register
(R0)	General register 0
(R1)	General register 1
(R2)	General register 2
(R3)	General register 3
(R4)	General register 4
(R5)	General register 5
(R6 or SP)	General register 6 or stack pointer
(R7 or PC)	General register 7 or program counter
17777766	CPU error
17777772	Program interrupt request
(RS)17777776	Processor status word

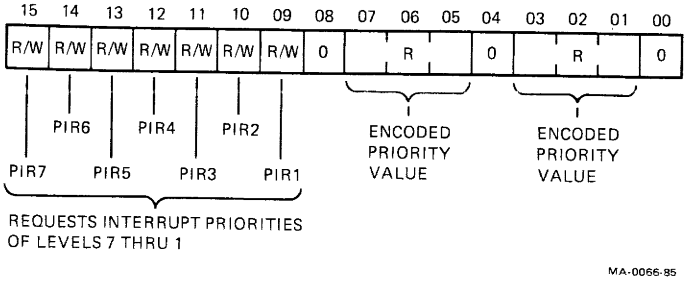
Processor Status Word – Address 17777776

The processor status word (PSW) contains information on the current status of the processor. This information includes the current processor priority, current and previous operational modes, the condition codes describing the results of the last instruction, an indicator for detecting the execution of an instruction to be trapped during program debugging, an indicator describing which register set (R0–R5 or R0'–R5') is in use, and an indicator for detecting the presence of a suspended instruction.



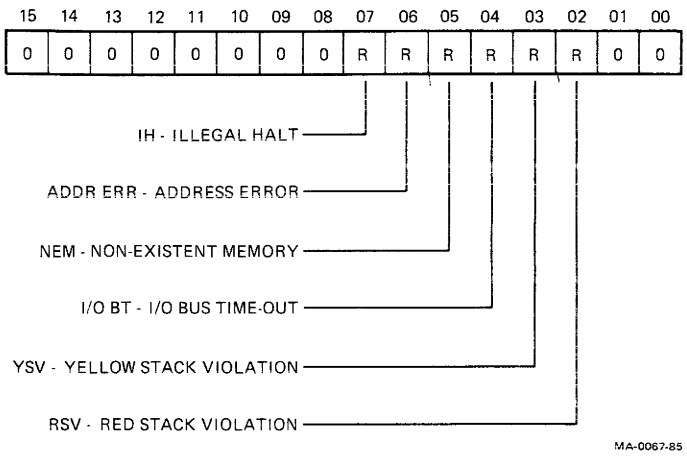
Program Interrupt Request – Address 17777772

Bits 7–5 represent the encoded value of the highest priority set in bits 15–9. Bits 3–1 are the same as bits 7–5.



CPU Error Register – Address 17777766

The CPU error register is used by the J11 to report any CPU errors detected to the system software. Six separate error conditions that cause the microprocessor to trap through location 4 are identified in above and described below.



Bits 15–8	They are not used.
Bit 7	Illegal halt, it is set when execution of a halt instruction is attempted in user or supervisor mode.
Bit 6	Address error, it is set when word access to an odd byte address or an instruction fetch from an internal register is attempted.
Bit 5	Non-existent memory, it is set when a reference to the main memory times out.
Bit 4	I/O bus time-out, it is set when a reference to the I/O page times out.
Bit 3	Yellow stack violation, it is set on a yellow zone stack overflow trap (kernel mode stack reference less than 400 octal).
Bit 2	Red stack violation, it is set on a red stack trap – a kernel stack push abort during an interrupt, abort, or trap sequence.
Bits 1–0	They are not used.

General Registers – Address R0–R7

There two groups of 16-bit general purpose registers, R0–R5 and R0'–R5' (Figure 6-14, J11 Register Architecture). These are used as accumulators, index reference, autoincrement, auto decrement, and stack pointers for temporary data storage. The register set information in the PS (bit<11>) defines which set is selected. PS<11> 0 selects R0–R5; PS<11>=1 selects R0'–R5'. The microcode can access only the selected register set. The state of the PDP-11 general registers at power up is undefined. They are accessible via software reference using the appropriate addressing modes or via $ and R commands in ODT.

Stack Pointer - Address R6 or SP
General register R6 is used as a hardware stack pointer (SP).This register is used to save and restore processor status word (PSW) information during hardware traps and interrupts. There are three stack pointer registers: one for kernel mode, one for supervisor mode and one for user mode.

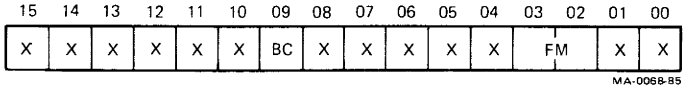
Program Counter - Address R7 or PC
General register R7 is used as the program counter (PC) and contains the address of the next instruction to be executed. It is used for addressing purposes and not as an accumulator for arithmetic operations.

Hit/Miss Register - Address 17777752
The hit/miss register (HMR) records the status of the MISS input from the system interface. The HMR is a shift register that records a hit as a 1 and a miss as a 0 for the most recent memory reads. A hit represents data located in the local memory and a miss means that data is located in the CTI Bus option memory. Bit 0 represents the most recent memory read and is shifted to the left on successive memory reads. The HMR is a read-only register.

Although the PC380 does NOT implement cache, the J11 clock is stalled by the J11 control gate array to simulate a cache read when obtaining data from local memory (local memory is the 512 Kbytes on the system module OR any memory residing on a daughter module).

Processor Maintenance Register - Address 17777750
The processor maintenance register is a 16-bit register used to identify the system architecture. It is always read as all 0s. All 0s in bits <7:4> indicate a CTI Bus module. Writes to the register have no effect but will not cause a nonexistent memory trap.

Cache Control Register - Address 17777746
The cache control register controls the operation of the cache memory. Cache bypass and force miss signals can be controlled by software via this register.



Bit 9 is the bypass cache bit and causes the J11 to assert BS1 during the second half of the read and write transactions.

Bits 3–2 are the force miss bits. When either of these bits are set, BS0 is asserted during the second half of read and write transactions.

On power up these bits are 0. These bits may be changed by software but should not be. Setting these bits would cause longer memory cycles to local memory, resulting in a decrease in performance. These bits should remain clear so that the J11 will recognize the MISS signal from the J11 control gate array and not stretch the cycle to local memory.

All other bits are not interpreted by the J11.

6.4.1.2 J11 Processor Traps – A variety of instructions and conditions will cause the processor to trap through vectors to service routines. The following list indicates the vectors and conditions.

Vectors	Conditions
004	Bus timeout, illegal halt, stack overflow trap
010	Illegal and reserved instruction traps
014	Breakpoint and trace trap
020	IOT instruction trap
024	Power fail trap
030	Emulator trap
034	Trap instruction trap
114	Memory error
240	PIRQ trap
244	Floating point error
250	Memory management abort

A bus timeout is provided so that the bus will not hang when a non-existent memory location access is attempted. If the processor does not receive a REPLY signal from a slave device a timeout will occur. The timeout will cause the bus cycle to terminate and the processor to trap through to location 4.

A power fail trap is provided to allow the processor to gracefully power down when ac power is lost. The POK signal is unasserted by the power supply when the AC power loss is detected. When the POK signal is unasserted, the processor will trap through location 24 to allow for the execution of a power fail routine.

6.4.1.3 Memory Management Unit Registers – The following is a listing of all memory management registers and their locations.

Addresses	
17772200–17772216	Supervisor instruction PDRs
17772220–17772236	Supervisor data PDRs
17772240–17772256	Supervisor instruction PARs
17772260–17772276	Supervisor data PARs
17772300–17772316	Kernel instruction PDRs
17772320–17772336	Kernel data PDRs
17772340–17772356	Kernel instruction PARs
17772360–17772376	Kernel data PARs
17777600–17777616	User instruction PDRs
17777620–17777636	User data PDRs
17777640–17777656	User instruction PARs
17777660–17777676	User data PARs
17777572	Status register 0
17777574	Status register 1
17777576	Status register 2
17777516	Status register 3

Vector	
250	MMU abort

At the completion of the power-up self-test, the MMU is disabled by clearing bit 00 in status register 0. Also, bit 04 in status register 3 is cleared so 22-bit mapping is not selected.

Tables 6-7, 6-8, and 6-9 show the memory mangement page address registers (PAR) and page descriptor registers (PDR) and their locations for the supervisor, kernel, and user page registers.

Table 6-7 Supervisor Active Page Registers

Instruction Space			Data Space		
No.	**PAR**	**PDR**	**No.**	**PAR**	**PDR**
0	17772240	17772200	0	17772260	17772220
1	17772242	17772202	1	17772262	17772222
2	17772244	17772204	2	17772264	17772224
3	17772246	17772206	3	17772266	17772226
4	17772250	17772210	4	17772270	17772230
5	17772252	17772212	5	17772272	17772232
6	17772254	17772214	6	17772274	17772234
7	17772256	17772216	7	17772276	17772236

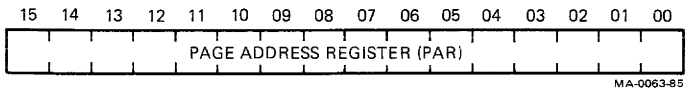
Table 6-8 Kernel Active Page Registers

Instruction Space			Data Space		
No.	**PAR**	**PDR**	**No.**	**PAR**	**PDR**
0	17772340	17772300	0	17772360	17772320
1	17772342	17772302	1	17772362	17772322
2	17772344	17772304	2	17772364	17772324
3	17772346	17772306	3	17772366	17772326
4	17772350	17772310	4	17772370	17772330
5	17772352	17772312	5	17772372	17772332
6	17772354	17772314	6	17772374	17772334
7	17772356	17772316	7	17772376	17772336

Table 6-9 User Active Page Registers

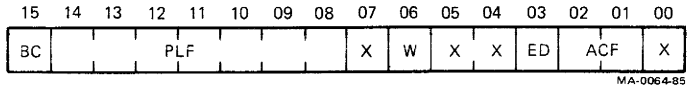
Instruction Space			Data Space		
No.	**PAR**	**PDR**	**No.**	**PAR**	**PDR**
0	17777640	17777600	0	17777660	17777620
1	17777642	17777602	1	17777662	17777622
2	17777644	17777604	2	17777664	17777624
3	17777646	17777606	3	17777666	17777626
4	17777650	17777610	4	17777670	17777630
5	17777652	17777612	5	17777672	17777632
6	17777654	17777614	6	17777674	17777634
7	17777656	17777616	7	17777676	17777636

Page Address Registers (PAR)
The page address registers (PAR) contain the 16-bit page address field (PAF) that specifies the base address of the page.



The page address register may be thought of alternatively as a relocation constant, or a base register containing a base address. Either interpretation indicates the basic function of the page address register (PAR) in the relocation scheme.

Page Descriptor Registers (PDR)
The page descriptor registers (PDR) contain information relative to page expansion, page length, and access control.



Bit 15 — BC – Bypass Cache. It is a read/write bit that implements a conditional cache bypass mechanism. If the PDR accessed during a relocation operation has this bit set, the time-multiplexed signal BS 1 H is asserted during the subsequent I/O cycle. This bit should not be changed by the software since it would degrade local memory performance.

Bits 14–08 — PLF – Page Length Field. They are read/write bits. This seven-bit field specifies the block number which defines the boundary of that page. The block number of the virtual address is compared against the Page Length Field to detect length errors. An error occurs when expanding upwards if the block number is greater than the Page Length Field, and when expanding downwards if the block number is less than the Page Length Field.

Bit 07 — It is not used and is always read as 0.

Bit 06 — W – Write Access. It is a read-only bit that indicates whether this page has been modified (i.e., written into) since either the PAR or PDR was loaded (W=1 is affirmative). The W bit is useful in applications which involve disk swapping and memory overlays. It is used to determine which pages have been modified and hence must be saved in their new form and which pages have not been modified and can be simply overlaid. The W bit is reset to 0 whenever either the PAR or PDR is modified (written into).

Bits 05–04 — They are not used and are always read as 0s.

Bit 03

ED – Expansion Direction. It is a read/write bit that specifies in which direction the page expands. If ED=0, the page expands upwards from block number 0 to include blocks with higher addresses; if ED=1, the page expands downwards from block number 127 to include blocks with lower addresses. Upward expansion is usually used for program space while downward expansion is used for stack space.

Bits 02–01

ACF – Access Control Field. They are read/write bits. This 2 bit field describes the access rights of this particular page. The access codes or keys specify the manner in which a page may be accessed and whether a given access should result in an abort of the current operation. A memory reference that causes an abort is not completed, but terminated immediately. Aborts are caused by attempts to access nonresident pages, by page length errors, or by access violations, such as attempting to write into a read-only page. Traps are used as an aid in gathering memory management information. The following list shows the ACF keys and their functions. The ACF is written into the PDR under program control.

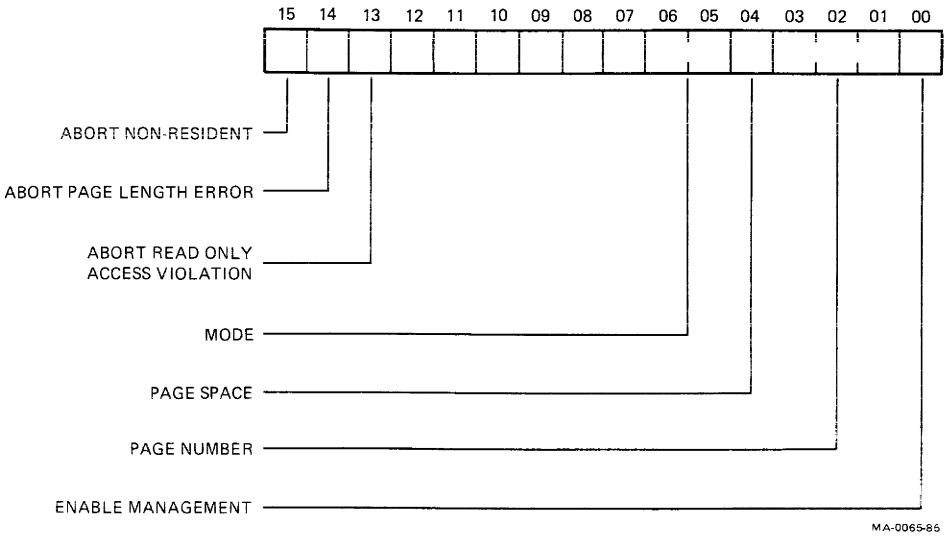
ACF	**Key**	**Description**	**Function**
00	0	Nonresident	Abort any attempt to access this nonresident page.
01	2	Resident, read-only	Abort any attempt to write to this page.
10	4	(unused)	Abort all accesses.
11	6	Resident, read/write	Read or write is allowed. No trap or abort is allowed.

Bit 00

It is not used and is always read as 0.

Status Register 0 (SR0) – Address 17777572

The SR0 contains abort error flags, memory management enable, plus other essential information required by an operating system to recover from an abort or service a memory management trap. SR0<15:13,0> is cleared at power up, by a console start, and by a RESET instruction. SR0<6:1> is UNDEFINED at power-up.



Bit 15 — Abort Non-Resident. It is a read/write bit that is automatically set by attempting to access a page with an access control field (ACF) key equal to 0 or 4, or by enabling relocation with an illegal mode in the PS. When this occurs, the processor will trap through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit as a result of hardware action is useful as a monitor of the status of the memory management unit. Setting this bit under program control will not cause a trap to occur. This bit should be reset to 0 by the program after an abort or trap has occurred in order to resume monitoring memory management.

Bit 14 — Abort Page Length. It is a read/write bit that is automatically set by attempting to access a location in a page with a block number (virtual address bits 12–6) that is outside the area authorized by the page length field (PLF) of the PDR for that page. When this occurs, the processor will trap through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit as a result of hardware action is useful as a monitor of the status of the memory management unit. Setting this bit under program control will not cause a trap to occur. This bit should be reset to 0 by the program after an abort or trap has occurred in order to resume monitoring memory management.

Bit 13 — Abort Read-Only. It is a read/write bit that is automatically set by attempting to write into a read-only page. When this occurs, the processor will trap through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit as a result of hardware action is useful as a monitor of the status of the memory management unit. Setting this bit under program control will not cause a trap to occur. This bit should be reset to 0 by the program after an abort or trap has occurred in order to resume monitoring memory management.

Bits 12–07 — These bits are not used.

Bits 06–05 — Mode of Operation. They are read/write bits that indicate the CPU mode (kernel, supervisor, user, illegal) associated with the page causing the abort. (Kernel=00, Supervisor=01, User=11, illegal=10.) They are automatically written at the time of the abort. These bits can also be written under program control. However, only that information which is automatically written in these bits as a result of hardware action, is useful as a monitor of the status of the memory management unit.

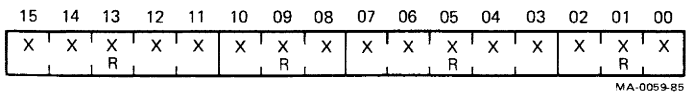
Bit 04 — Page Space. It is a read-only bit that indicates the current address space (instruction or data) of the current relocation operation causing the abort: 0=instruction space, 1=data space.

Bits 03–01 — Page Number. They are read/write bits that are used to identify the page being accessed when an abort occurs. They are automatically written at the time of the abort. (Pages, like blocks, are numbered from 0 upwards.) These bits can also be written under program control. However, only that information which is automatically written in these bits as a result of hardware action, is useful as a monitor of the status of the memory management unit.

Bit 00 — Enable Relocation and Protection. It is a read/write bit that is the memory management enable bit and is set and cleared under program control. When it is set to 1, all addresses are relocated and protected by the memory management unit. When cleared to 0, the memory management unit is disabled and addresses are neither relocated nor protected.

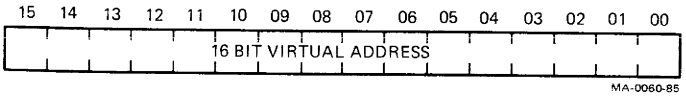
Status Register 1 (SR1) – Address 17777574

The SR1 register records any autoincrement or autodecrement of a general purpose register, including explicit references through the PC. The increment or decrement by which the register was modified is stored in 2's complement notation. This is necessary in order to accomplish an effective recovery from an error resulting in an abort. The lower byte is used for all source operand instructions and the destination operand may be stored in either byte dependent on the mode and instruction type. The register is cleared at the beginning of each instruction fetch.

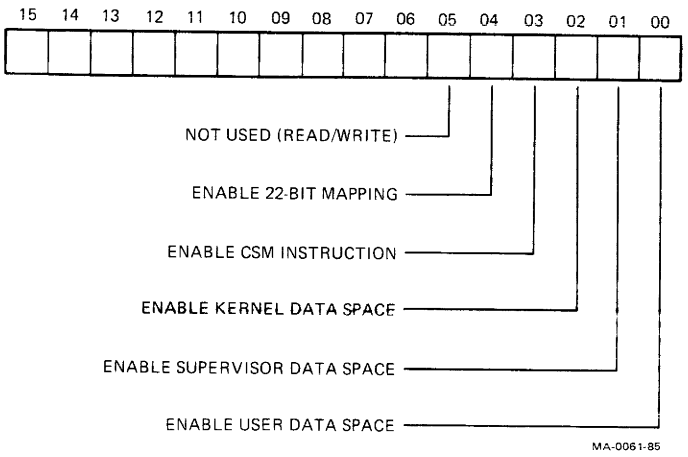


Bits 15–11	Amount changed, they represent the amount of autoincrement or autodecrement in the 2's complement notation for the register defined in bits 10–8.
Bits 10–8	Register, they identify one of the eight general purpose registers.
Bits 7–3	Amount changed, they represent the amount of autoincrement or autodecrement in the 2's complement notation for the register defined in bits 2–0.
Bits 2–0	Register, they identify one of the eight general purpose registers.

Status Register 2 (SR2) – Address 17777576
SR2 is loaded with the 16-bit virtual address (VA) at the beginning of each instruction fetch, but is not updated if the instruction fetch fails. SR2 is read-only; a write attempt will not modify its contents. SR2 is the virtual address program counter. Upon an abort, the result of SR0 bit 15, 14, or 13 being set will freeze SR2 until the SR0 abort flags are cleared.



Status Register 3 (SR3) – Address 17777516
SR3 is cleared at power up, by a console start, and by a RESET instruction.



Bits 15–06	They are not used.
Bit 05	Reserved. It is a read/write bit that has no effect on PC352 system module operation.

Bit 04 — Enable 22-Bit Mapping. It is a read/write bit that enables or disables the memory management 22-bit mapping. If memory management is not enabled, (SR0 bit 0 is clear), this bit is ignored and the 16-bit address is not relocated. If memory management is enabled, (SR0 bit 0 is set) and this bit is clear, the computer uses 18-bit mapping. If memory management is enabled, and this bit is set, the computer uses 22-bit mapping.

NOTE

A 22-bit mapping scheme should always be used. If 18-bit mapping is used, address bits <21:18> will always be 0s and the I/O page will be selected when bits <17:13> are all ones. In 18-bit mode, 12 kilobytes of the 16 kilobytes of ROM will not be accessible (along with any other memory devices beyond the 18-bit address range).

Bit 3 — Enable CSM instruction. (1=enable, 0=disable) This bit enables recognition of the call supervisor mode instruction.

Bit 2 — Enable kernel data space. (1=enable, 0=disable) Enables the data space mapping for the kernel mode.

Bit 1 — Enable supervisor data space. (1=enable, 0=disable) Enables the data space mapping for the supervisor mode.

Bit 0 — Enable user data space. (1=enable, 0=disable) Enables the data space mapping for the user mode.

6.4.1.4 Memory Space Relocation and Mapping – The J11 can implement instruction and data space (I/D space) relocation as a technique to expand the direct addressing range a J11 program or to facilitate efficient code sharing in a multiuser environment. If I/D space is enabled the J11 classifies memory references as instructions or data and independently relocates them via the corresponding PAR/PDR pair. The instruction space information below identifies the memory references classified by the J11 as D space. If I/D space is not enabled all memory references are relocated via the I space for that mode.

Instruction Space Information
Instruction fetches
Immediate operands (mode 27)
Absolute addresses (mode 37)
Index words
First references in modes 17, 47, and 57

Memory references (first, second and third) by addressing modes for normal instructions are as follows.

Mode	Register	
0–6	7	
0	–	–
1	D	I
2	D	I
3	D/D	I/D
4	D	I
5	D/D	I/D
6	I/D	I/D
7	I/D/D	I/D/D

The following is a memory map of addresses specific to the Professional 380 hardware. Words and bits of I/O registers are listed with a code specifying how they may be accessed. Access codes (AC) are listed below:

Word/Bit	Access Code (AC)
R/W	Address may be read or written.
R/t	Address is read-only, writes cause a timeout trap.
R/	Address is read-only, writes are ignored.
0/W	Address is write-only, reads as all 0s.
0/	Reads from address obtain all 0s.
1/W	Address is write-only, reads as all 1s.
1/	Reads from address obtain all 1s.
x/	Reads from address (bit) are undefined.
/W	Write conditions for this bit.
R/W once	The bit is cleared after reading. Writes have no effect y/W once read condition "y" from above. Used for bits/addresses where the first write causes some status to change. Successive writes do nothing more unless other events change the status again.

Address	Function
14000000–14377777	R/W; typical location for video memory
17700000–17727777	R/t, reserved for future expansion
17730000–17757777	R/t, base system ROM (in memory space)
17760000–17767777	R/t Base system ROM (in I/O page)
17767700	Continue boot address
17767730	Crash address
17770000–17770037	Reserved for manufacturing

Page Address Register/Page Descriptor Register Addresses:

Address		Description
17772200–17772216		R/W supervisor I space PDRs
17772220–17772236		R/W supervisor D space PDRs
17772240–17772256		R/W supervisor I space PDRs
17772260–17772276		R/W supervisor D space PDRs
17772300–17772316		R/W kernel I space PDRs
17772320–17772336		R/W kernel D space PDRs
17772340–17772356		R/W kernel I space PDRs
17772360–17772376		R/W kernel D space PDRs
Virtual address	15–13	APF – active page field selects PAR
	12–06	BN – block number
	05–00	DIB – displacement in block
Physical address	21–06	Obtained from adding BN to the PAR
	05–00	Value is obtained from DIB bits

Page Descriptor Register

Address	AC	Bits	Description
See List Above	–	–	PDR – page descriptor register
	R/W	15	Bypass cache when set
	R/W	14–08	PLF – page length field compared to virtual BN, error if ED=0 and BN>PLF, or ED=1 and BN<PLF
	R/W	07	Not used, always read as 0s
	R/W	06	W – page written; W=1 if page is modified
	R/W	05–04	Not used, always read as 0s
	R/W	03	ED – expansion direction; ED=0 means upwards
	R/W	02–01	ACF – access control field
		00	Non-resident – abort all accesses
		01	Read-only – abort on write attempt
		10	Not used – abort all accesses
		11	Read/write – access allowed
	R/W	00	Not used, always read as 0s.

Memory Management Register #3

Address	AC	Bits	Description
17772516	–	–	MMR3 – Memory management register #3
	R/	15–06	Reserved bits currently always read as 0
	R/W	05	Enable I/O map, a 1 enables MAP output of the J11
	R/W	04	Enable 22-bit mapping if set=1
	R/W	03	Enable CSM instruction if =1
	R/W	02–00	Mode bits; when D space disabled, all memory references use the I space registers or both I and D space are used.

Address	AC	Bits	Description
	R/W	02	Kernel D space enabled if =1
	R/W	01	Supervisor D space
	R/W	00	User D space

System Clock Registers

Address	Description
17773000–17773032	ROD clock registers

Address	AC	Description	Octal Range
17773000	R/W	Seconds	000–073
17773002	R/W	Seconds alarm	000–073
17773004	R/W	Minutes	000–073
17773006	R/W	Minutes alarm	000–073
17773010	R/W	Hours – 12 hour AM	001–014
		Hours – 12 hour PM	201–214
		Hours – 24 hour	000–027
17773012	R/W	Hours alarm	same as hours
17773014	R/W	Day of week	001–007
17773016	R/W	Date of month	001–037
17773020	R/W	Month of year	001–014
17773022	R/W	Year of century	000–143

Control/Status Register #0

Address	AC	Bits	Description
17773024	–	–	CSR0 – Control/status register 0
	R/	7	UIP – update in progress
	R/W	6–4	DV2–0 divider control should be 010
	R/W	3–0	RS3–0 Rate select
			0000 256 Hz
			0001 128 Hz
			0010 8192 Hz, etc.

Control/Status Register #1

Address	AC	Bit	Description
17773026	–	–	CSR1 – Control/status register 1
	R/W	7	SET – bit=1 to halt update cycles
	R/W	6	PIE – periodic interrupt enable, set to enable
	R/W	5	AIE – alarm interrupt enable, set enables alarms
	R/W	4	UIE – update ended interrupt Enable, set enables
	R/W	3	N/U – not used
	R/W	2	DM – data mode, set for binary dates; 0 is BCD
	R/W	1	24/12 – hour mode, set for 24 hour format
	R/W	0	DSE – daylight savings enable, set enables switching from/to daylight savings time

Control/Status Register #2

Address	AC	Bit	Description
17773030	–	–	CSR2 – control/status register 2
	R/	7	IRQF – interrupt request flag, 1=interrupt
	R-once	6	PF – periodic interrupt flag
	R-once	5	AF – alarm interrupt flag
	R-once	4	UF – Update-ended interrupt flag
	0/	3–0	Not used

Control/Status Register #1

Address	AC	Bit	Description
17773032	–	–	CSR1 – control/status register 1
	R-once	7	VRT – valid RAM and time, 1=OK, 0=lost power
	0/	6–0	Not used

Battery Backed-Up RAM Registers

Address	AC	Description
17773034 – 17773176		Battery backed-up RAM
17773034	R/W	High byte boot device identification number
17773036	R/W	Low byte boot device identification number
17773040	R/W	Physical slot number of boot device on Professional 350 high byte of second identification number on Professional 380
17773042	R/W	Physical unit number of boot device on Professional 350 low byte of second identification number on Professional 380
17773044	R/W	High byte checksum value
17773046	R/W	Low byte checksum value
17773150	R/W	Low byte of pointer to configuration table
17773152	R/W	High byte of pointer to configuration table

Interrupt Controller CSR Registers

Address		Description
17773200 – 17773212	–	Interrupt controller CSR registers

Commands for all interrupt CSRs are:
000 – RESET, IMR=1, IRR=0 02x – clear all IRR and IMR bits

03b – clear IRR and IMR bit b
04x – clear all IMR bits
05b – clear IMR bit b
06x – set all IMR bits
07b – set IMR bit b
10x – clear all IRR bits
11b – clear IRR bit b
12x – set all IRR bits
13b – set IRR bit b

Reserved Address	AC	Description
17773200	0/	Reserved

Interrupt Controller #0 CSR Register

Address	AC	Description
17773202	0/W	Interrupt controller 0 CSR register

Level/Vector

0/234	TOD clock interrupt
1/200	keyboard receiver
2/204	keyboard transmitter
3/210	communications port
4/214	modem controls changed
5/220	printer receiver
6/224	printer transmitter
7/230	TOD clock

Reserved Address	AC	Description
17773204	0/	Reserved

Interrupt Controller #1 CSR Register

Address	AC	Description
17773206	0/W	Interrupt controller 1 CSR register

Level/Vector

b/3b0 – Slot b interrupt request A

Reserved Address	AC	Description
17773210	0/	Reserved
17773212	0/W	b/3b4 – Slot b interrupt request B

Communication Port Registers

Address		Description
17773300	–	Communications port registers
17773314		

Address	AC	Bits	Description
17773300	R/W	7–0	DBUF – data buffer register DAT7–00 – read RCV'd character and write character to XMIT
17773302	R/W	7–0	CSRA – control/status register A CSR A operates as a window to 11 internal registers.
17773304	0/	7–0	Reserved; always read as 0s
17773306	R/W	7–0	CSRB – control/status register B CSR B operates as a window to 11 internal registers
17773310	–	–	Modem control register 0
	R/W	7	MM – maintenance mode, set for loopback
	R/W	6–5	CS10 – clock source

CS1	CS0	URXC	UTXC	COTXC
0	0	RBRG	TBRG	none
0	1	CIRXC	CITXC	none
1	0	CIRXC	TBRG	TBRG
1	1	TBRG	TBRG	none

	R/W	4	DTR – data terminal ready, 1=set CDTR high
	R/W	3	RTS – request to send, 1=set CRTS high
	R/W	2	DSRS – data signaling rate select, sets CDSRD
	R/W	1	RL – remote loopback, sets CRL
	R/W	0	LL – local loopback, sets CLL @modem connector
17773312	R/t	7	MCR1 – modem control register 1 DSR – data set ready, 1=CDSR asserted
	R/t	6	RI – ring indicator, 1=CRI asserted
	R/t	5	CTS – clear to send, 1=CCTS asserted
	R/t	4	CD – carrier detect, 1=CCD asserted
	R/t	3	TI – test indicator, 1=CTI asserted
	R/t	2	SPDMI – speed mode indicator, 1=CSPDMI asserted
	0/t	1–0	Not used

Baud Rate Register

Address	AC	Bits	Description
17773314	0/W	3–0	Baud rate register

TBR3–0	16x clock baud rate
00 OCTAL	50
01	75
02	110
03	134.5
04	150
05	300
06	600
07	1200
10	1800
11	2000
12	2400
13	3600
14	4800
15	7200
16	9600
17	19200

Printer Port Registers

Address		Description
17773400 17773406	–	Printer port registers (see keyboard registers below). The status register and the MODEM 2 register are unique to the printer port register set.

Address	AC	Bits	Description
17773402	–	–	STAT – status register
	R/	7	DSR – data set ready if =1
	1/	6	Not used; always read as 1
17773404	–	–	MR2 – modem register 2
	R/W	7–4	1011 – These must be set for proper operation.

Keyboard Port Registers

Address			Description
17773500 17773506	–		Keyboard port registers

Address	AC	Bits	Description
17773500	–	–	DBUF – data buffer
	0/	15–8	Not used; read as 0s
	R/W	7–0	DAT7-0. Read received character or write character
17773502	–	–	STAT – Status register
	0/	15–8	Not used, read as 0s
	1/	7–6	Not used, read as 1s
	R/	5	FE – framing error detected if set =1
	R/	4	OE – overrun error detected if set =1
	R/	3	PE – parity error detected if set =1
	R/	2	Not used
	R/	1	RD – receiver done if set =1
	R/	0	TR – transmitter ready for next character if set =1
17773504	–	–	MR1 – mode register 1 – accessed after CMD or MR2 read
	0/	15–8	Not used, read as 0s [word typically 116]
	R/W	7–6	SBL10 – stop bit length. 00=invalid; 01=1 stop bit; 10=1.5 stop bits; 11=2 stop bits.
	R/W	5	PT – parity type. PT=1 selects even parity, else odd.
	R/W	4	PC – parity control. PC=0=no parity; =1 add PT parity
	R/W	3–2	CL10 – character length. 00=5 bits; 01=6 bits; 10=7 bits; 11=8 bits.
	R/W	1	ONE – must be set to 1 for valid operation.
	R/W	0	Not used

Address	AC	Bits	Description
17773504	–	–	MR2 – mode register 2, accessed next after MR1 [typically 74]
	0/	15–8	Not used, read as 0s
	R/W	7–4	0011 – these bits must be 0011 for correct operation.
	R/W	3–0	BRS30 – baud rate select (see communication port TBR3–0)
17773506	–	–	CMD – command register [typically 47]
	0/	15–8	Not used; read as 0s
	R/W	7–6	OM10 – Operating Mode. 00=normal; 01=auto echo mode; 10=local loopback; 11=remote loopback.
	R/W	5	RTS – request to send
	0/once	4	RE – reset error. Write RE=1 clears PE, OE, FE.
	R/W	3	FB – force break. 0=normal; 1=transmit space (break)
	R/W	2	RxEN – receiver enable if set =1.
	R/W	1	DTR – data terminal ready if =1.
	R/W	0	TxEN – transmitter enabled when =1, else mark state.

Identification PROM

Address	AC	Description
17773600–17773676	R/t	ID PROM – 32 bytes

System Control/Status Register

Address	AC	Bits	Description
17773700	–	–	CSR – system control status register
	0/	15–8	Not used; read as 0s
	R/W	7	BRKEN – break enable if set=1 and TERM L=0
	R/	6	NBD1 – number of banks on daughter module (bit 1)
	R/	5	NBM1 – number of banks on mother module (bit 1)
	R/	4	MNPRS – 1=video monitor present
	R/	3	P256KD – 0=64K parts; 1=25K parts (daughter board)

Address	AC	Bits	Description
	R/	2	NBD0 – number of banks on daughter module (bit 0)
	R/	1	P256KM – 0=64K parts; 1=25K part (mother board)
	R/	0	NBM0 – number of banks on mother module (bit 0)

NBx1	NBx0	P256Kx
0	0	x no memory on module x.
0	1	0 128 Kb in 1 bank 64K RAM
1	0	0 256 Kb in 2 banks 64K RAM
1	1	0 512 Kb in 4 banks 64K RAM
0	1	1 512 Kb in 1 bank 256K RAM
1	0	1 1 Mb in 2 banks 256K RAM
1	1	1 2 Mb in 4 banks 256K RAM

Option Module Present Register

Address	AC	Bits	Description
17773702	–	–	OMPR option module present register
	0/	15–7	Not used; always read as 0s
	R/	6–0	Bit b=1 if module present in slot b

LED/Mode Register

Address	AC	Bits	Description
17773704	–	–	LED and MODE register
	0/	15–2	read 0s
	/W	3–0	LED3 – 0/writing a 0 sets selected LED
	R/	1	LOST – loop on self test
	R/	0	TERM – terminal present
		1–0	00 – customer mode 01 – console mode 10 – service mode 11 – manufacturing mode

Single Stepping Micro ODT Register

Address	AC	Bits	Description
17773706	–	–	SSODT – single stepping μODT register
	R/	15	BCRAY – 0=ok. 1=error in the B-state machine
	R/	14	CRAY – 0=ok. 1=error in the M-state machine
	R/	13	JCRAY – 0=ok. 1=error in the J-state machine

Address	AC	Bits	Description
	0/	12–5	not used
	R/W	4	SSODT – 0=single stepping disabled. 1=single stepping enabled if TERM L is low.
	0/	3–0	not used.

μODT Address	μODT Address Destination
17774000–17774176	Slot 0 addresses
17774200–17774376	Slot 1 addresses
17774400–17774576	Slot 2 addresses
17774600–17774776	Slot 3 addresses
17775000–17775176	Slot 4 addresses
17775200–17775376	Slot 5 addresses
17775400–17775576	Slot 6 addresses

Video Generation Integrated Logic Registers

Address	Description
17775400–17775426	Professional 380 video registers Most video registers are NOT write byte addressable. Registers for which write byte operations are valid are indicated below.

Address	AC	Bits	Description
17775400	–	–	VIDR – video identification register
	0/	15–8	always 0
	R/	7–0	ID Data Byte ID=00050 octal ID=10050 octal (EBO)
17775402	–	–	VRAR – video ROM address register
	0/W	15–0	Writing any data resets ROM address
17775404	–	–	VCSR – video control status register (write byte addressable)
	R/	15	Transfer done (counter register=0)
	R/W	14	Done interrupt enable (init to 0)
	R/	13	EBO not present (0 when EBO connected)
	0/	12–11	Reserved (always 0)
	R/W	10	Color map enable (power up to 0=disabled)
	R/W	9–8	Operation mode (init to 0)
			00 bit transfer left → right
			01 bit transfer right → left
			10 word transfer left → right
			11 word transfer right → left

Address	AC	Bits	Description
	R/	7	End of frame (vertical retrace=1)
	R/W	6	Frame interrupt enable (init to 0=disabled)
	R/	5	Odd/even frame (1=even, interlaced only)
	R/W	4	Video amplifiers on (init to 0=off)
	R/	3	Externally synchronized (1=IVIS connected)
	R/W	2–0	Line mode (power up to 0)

2–0	#vis	#line	frames/sec
000	240	526	60, noninterlaced
001	256	626	50, noninterlaced
010	240	525	60, interlaced
011	256	625	50, interlaced
100	480	525	60, interlaced
101	512	625	50, interlaced

17775406	–	–	VPCR – video plane 1 control register (blue) (write byte addressable)
	0/	15–7	Reserved (always 0)
	R/W	6	Plane 1 scroll disable (power up 0=enabled)
	R/W	5	Plane 1 memory enable (init to 0=disabled)
	R/W	4–3	Plane 1 horizontal resolution

4–3	Resolution Factor
00	1024 resolution
01	512 resolution
10	256 resolution
11	plane off (black)

R/W 2–0 Plane 1 logic operation

Operation [if VCSR 9=0 (bitmode)]

2–0	Operation
000	No-op
001	XOR pattern register to video memory
010	Move pattern register to video memory
011	Move pattern register 'NOT' to video memory
100	Bit set pattern register to video memory
101	Bit clear pattern register to video memory
110	Clear bit in video memory
111	Set bit in video memory

Operation [if VCSR 9=1 (wordmode)]

2–0	Operation
000	No-op
001	Complement video memory
010	Move pattern register bit 0 to video memory
011	Move pattern register bit 1 'NOT' to video memory
100	Reserved
101	Shift screen 1 bit (horizontal)
110	Shift screen 2 bits (horizontal)
111	Shift screen 4 bits (horizontal)

Address	AC	Bits	Description
17775410	–	–	VOPC – video option plane control register (write byte addressable)
	0/	15	Reserved (always 0)
	R/W	14	Plane 3 scroll disable (power up 0=enabled)
	R/W	13	Plane 3 memory enable (init to 0=disabled)
	R/W	12–11	Plane 3 horizontal resolution

12–11	Resolution Factor
00	1024 resolution
01	512 resolution
10	256 resolution
11	plane off (black)

R/W	10–8	Plane 3 logic operation

Operation [if VCSR 9=0 (bitmode)]

10–8	Operation
000	No-op
001	XOR pattern register to video memory
010	Move pattern register to video memory
011	Move pattern register 'NOT' to video memory
100	Bit set pattern register to video memory
101	Bit clear pattern register to video memory
110	Clear bit in video memory
111	Set bit in video memory

Operation [if VCSR 9=1 (wordmode)]

10–8	Operation
000	No-op
001	Complement video memory
010	Move pattern register bit 0 to video memory
011	Move pattern register bit 1 'NOT' to video memory
100	Reserved
101	Shift screen 1 bit (horizontal)
110	Shift screen 2 bits (horizontal)
111	Shift screen 4 bits (horizontal)

Address

AC	Bits	Description
0/	7	Reserved (always 0)
R/W	6	Plane 2 scroll disable (power up 0=enabled)
R/W	5	Plane 2 memory enable (init to 0=disabled)
R/W	4–3	Plane 2 horizontal resolution

4–3	Resolution Factor
11	1024 resolution
10	512 resolution
01	256 resolution
00	plane off (black)

R/W	2–0	Plane 2 logic operation

Operation [if VCSR 9=0 (bitmode)]

2–0	Operation
000	No-op
001	XOR pattern register to video memory
010	Move pattern register to video memory
011	Move pattern register 'NOT' to video memory
100	Bit set pattern register to video memory
101	Bit clear pattern register to video memory
110	Clear bit in video memory
111	Set bit in video memory

Operation [if VCSR 9=1 (wordmode)]

2–0	Operation
000	No-op
001	Complement video memory
010	Move pattern register bit 0 to video memory
011	Move pattern register bit 1 'NOT' to video memory
100	Reserved
101	Shift screen 1 bit (horizontal)
110	Shift screen 2 bits (horizontal)
111	Shift screen 4 bits (horizontal)

Address	AC	Bits	Description
17775412	–	–	VCMR – video color map register
	0/W	15	Red intensity 0 (LSB)
	0/W	14	Green intensity 0 (LSB)
	0/W	13–12	Blue intensity 1–0 (0 LSB)
	0/	11	Reserved (always 0)
	0/W	10–8	Color address 2–0 (2 MSB, 0 LSB)
	0/W	7–5	Red intensity 3–1 (3 MSB)
	0/W	4–2	Green intensity 3–1 (3 MSB)
	0/W	1–0	Blue intensity 3–2 (3 MSB)
17775414	–	–	VSCR – video scroll register (write byte addressable)
	0/	15–10	Reserved (always 0)
	R/W	9–8	Current page if VCSR bit 2=0 (line mode)
	R/W	7–0	Scroll offset if VCSR bit 2=0
	R/W	9	Current page if VCSR bit 2=1 (line mode)
	R/W	8–0	Scroll offset if VCSR bit 2=1
17775416	–	–	VX – Video X register
	0/	15–10	Reserved (always 0)
	R/W	9–0	X (horizontal) address for start of operation
17775420	–	–	VY – Video Y register
	0/	15–10	Reserved (always 0)
	R/W	9–0	Y (vertical) address for start of operation
17775422	–	–	VCNT – video counter register
	R/W	15–0	Operation counter
17775424	–	–	VPAT – video pattern register
	R/W	15–0	Pattern register
17775426	–	–	VMBR – video memory base register. Specify 128 kilobyte boundary. On Professional 380, largest allowable value is 170 (i.e., 174 is illegal).
	0/	15–9	Reserved (always 0)
	R/W	8–2	Memory base (8–address bit 23, 2–address bit 17)
	0/	1–0	Reserved (always 0)
17775430 to 17775576	0/	–	Reserved registers in video slot; read 0 and writes are ignored

Maintenance Terminal DL Interface Registers

Address	AC	Bits	Description
17777560 to 17777566	0/	15-0	Maintenance terminal DL interface registers if TERM L is high; if TERM L=0, then see below
17777560	–	–	RCSR – receiver control and status register
	0/	15-8	Always read as 0s
	R/	7	RD – Receiver done=1
	R/	6-0	Not used; always read as 0s
17777562	–	–	RBUF – Receiver data buffer
	R/	7-0	DAT7-0 – contains the last received character
17777564	–	–	XCSR – Transmitter control/status register
	R/	7	TR – transmitter ready if=1
	R/	6-0	Not used; always read as 0s
17777566	–	–	XBUF – Transmitter data buffer
	x/W	7-0	DAT7-0 – Load this with byte to be transmitted.

Memory Management Registers

Address	AC	Bits	Description
17777572	–	–	MMR0 – memory management register #0
	R/	15	Abort non-resident; page fault with ACF=0 or 2
	R/	14	Abort page length error
	R/	13	Abort read-only access violation
	R/	12-07	reserved bits
	R/	06-05	Processor page mode; 00=K, 01=S, 10=illegal, 11=user
	R/	04	Page address space; 0=1 space, 1=D space.
	R/	03-01	Page number of reference causing an MMU abort
	R/W	00	Enable relocation if set to 1
17777574	–	–	MMR1 – memory management register #1 Records any autoincrement/autodecrement of registers
	R/	15-11	Amount second register changed (in 2's complement)

Address	AC	Bits	Description
	R/	10–08	Register number for second change
	R/	07–03	Amount first register changed (in 2's complement)
	R/	02–00	Register number for first change
17777576	–	–	MMR2 – memory management register #2
	R/	–	Loaded with virtual address at beginning of each fetch

Page Descriptor Registers

Address	Description
17777600–17777616	R/W User I space PDRs
17777620–17777636	R/W User D space PDRs
17777640–17777656	R/W User I space PDRs
17777660–17777676	R/W User D space PDRs

System Registers

Address	AC	Bits	Description
17777740 to 17777750	0/	–	System registers – all I/O registers in this address range are considered "system registers" by the J11 and DC365. Access to an address in this range will be similar to an access to the maintenance register at 17777750

J11 Prefetch Buffer Register (Cache Control Register)

Address	AC	Bits	Description
17777746	–	–	CCR – cache control register
	0/	15–11	Uninterpreted by J11, hardware always provides 0s
	R/W	10	Uninterpreted by J11
	R/W	9	BC – bypass cache if set
	R/W	8–4	Uninterpreted by J11
	R/W	3–2	FM – force cache miss if either bit set
	R/W	1–0	Uninterpreted by J11

Processor Maintenance Register

Address	AC	Bits	Description
17777750	0/	15–0	Processor maintenance register; always read as 0s; writes have no effect.

Hit/Miss Register

Address	AC	Bits	Description
17777752	–	–	HMR – hit/miss register
	0/	15–6	Always read as 0s; writes have no effect.
	R/	5–0	Bits flow from 0 to 5; logical 1=cache hit; 0=miss.

CPU Error Register

Address	AC	Bits	Description
17777766	–	–	CPU error register, it is cleared by any write reference
	0/W once	15–8	Not used
	R/W once	7	IH – it is an illegal halt when set
	R/W once	6	ADDR ERR – Addr error when it is set (odd or reg I fetch)
	R/W once	5	NEM – nonexistent memory
	R/W once	4	I/O BT – I/O bus timeout (no I/O page address)
	R/W once	3	YSV – yellow stack trap
	R/W once	2	RSV – red stack trap
	0/W once	1–0	Not used

Programmable Interrupt Register

Address	AC	Bits	Description	
17777772	–	–	PIRQ – programmed interrupt register	
	R/W	15	PIR7 – queue request for interrupt priority 7, if set	
	R/W	14	PIR6	Bits 14–9 are for interrupt levels 6–1. When the program interrupt request is granted, the processor traps through a vector at virtual location location 240. Interrupt service routines must clear the appropriate bit in this group before exiting.
	R/W	13	PIR5	
	R/W	12	PIR4	
	R/W	11	PIR3	
	R/W	10	PIR2	
	R/W	9	PIR1	
	0/	8	Always 0	
	R/	7–5	PEV – priority encoded value of bits 15–9 by J11	
	0/	4	Always 0	
	R/	3–1	PEV – like bits 7–5, they are also set by the J11	
	0/	0	Always 0.	

Processor Status Register

Address	AC	Bits	Description
17777776	–	–	PIR – processor status register (P means protected bit)
	R/W P	15–14	Current processor mode:

15–14	Processor Mode
00	Kernel
01	Supervisor
10	Illegal
11	User

R/W P	13–12	Previous mode
R/W P	11	Register set, 0=set R0–R5, 1=set R0'–R5'
0/	10–9	Not used; read as 0s
R/W	8	Reserved
R/W P	7–5	Processor interrupt priority level
R/W P	4	Trace trap (T–bit), 1=trap through vector 14
R/W	3–0	Processor condition codes NZVC

6.4.1.5 Floating Point Unit Registers – Refer to the *Microcomputers and Memories* for a description of floating point data formats and registers.

6.4.1.6 J11 Interrupt Signal Listing – The following is a listing of all J11 interrupts. Each interrupt begins with its vector address and provides its board signal name and signal description. The listing is arranged in order of priority level.

Vector Address	Interrupt Type	Priority Level	Board Signal	Description
4	Abort	*NM	–	Red stack violation (CPU error register bit 2)
4	Abort	*NM	–	Address error (CPU error register bit 6)
250	Abort	*NM	–	Memory management violation (MMR0 bits <15:13>)
4	Abort	*NM	ABORTL	Timeout/nonexistent memory (CPU error register bits <5:4>)
114	Interrupt or Abort	*NM	PRITYL ABORTL	Parity error/PRITYL asserted then DC365 also asserts ABORTL

Vector Address	Interrupt Type	Priority Level	Board Signal	Description
14	Trap	*NM	–	Trace (T bit) set; (PSW bit 4)
4	Trap	*NM	–	Yellow stack violation (CPU error register bit 3)
24	Trap	*NM	PWRFL	Power fail
244	Interrupt	*NM	FPE L	Floating point exception Never occurs on PC380 (No FPA)
240	Trap	7	–	PIR 7 (PIRQ bit 15)
UD	Interrupt	7	IRQ 7	Interrupt level 7; not on Professional 380
100	Interrupt	6	EVENT L	Event interrupt; never on Professional 380
240	Trap	6	–	PIR 6 (PIRQ bit 14)
UD	Interrupt	6	IRQ 6	Interrupt level 6; not on Professional 380
240	Trap	5	–	PIR 5 (PIRQ bit 13)
UD	Interrupt	5	IRQ 5	Interrupt level 5; not on Professional 380
240	Trap	4	–	PIR 4 (PIRQ bit 12)
UD	Interrupt	4	IRQ 4	Interrupt level 4 for device interrupts
240	Trap	3	–	PIR 3 (PIRQ bit 11)
240	Trap	2	–	PIR 2 (PIRQ bit 10)
240	Trap	1	–	PIR 1 (PIRQ bit 9)
–		–	HALT	Places system in console mode

* NM=non-maskable, UD=user defined, –=none

Synchronous Interrupts

34	Trap	–	–	TRAP/trap instruction
30	Trap	–	–	EMT/emulator trap instruction
20	Trap	–	–	IOT/I/O trap instruction
14	Trap	–	–	BPT/breakpoint trap instruction
10	Trap	–	–	Illegal instruction
10	Trap	–	–	CSM=call to supervisor mode; (see J11 user's guide for conditions)
4	Trap	–	–	HALT=halt processor instruction (CPU error register bit 7). Trap through 4 if user mode, HALTS in kernel mode enter μODT.
–	–	–	–	WAIT=wait for interrupt instruction. Does not trap but frees the bus when waiting for external interrupt.

6.4.2 J11 Microprocessor DC365 Controller Gate Array

The DC365 contains three registers that reside in the I/O page address space. J11 cycles which access registers internal to the DC365 gain control of the bus. DMA devices do not access the internal DC365 registers.

All DC365 registers and their addresses are listed below.

Register	Address	21	20	17	14	11	876	543	210
CSR	17773700	1	111	111	111	011	111	000	000
SSODT	17773706	1	111	111	111	011	111	000	110
MAINT	17777750	1	111	111	111	111	111	101	000
sysreg	1777770x	1	111	111	111	111	111	10b	bbb

The following list shows the access codes used for the DC365 registers.

Code	Meaning
R/W	Bit(s) may be read from or written to.
R/	Bit(s) is/are read-only, writes are ignored.
R/t	Bit(s) is/are read-only, writes time-out.
x/	Bit(s) is/are currently undefined. For now, reads obtain all 0s and writes are ignored.
0/W	Bit(s) is/are read as all 0s, write-only bit(s).
0/	Bit(s) is/are read as all 0s (writes are ignored).

CSR Register

This register uses only the lower byte. Writes to the "R/" bits have no effect and the high byte always reads as 0s. The system control and status register provides configuration information, allowing the selection of certain operation modes.

Bit	Name	Access	Meaning
15–8		x/	Always read as 0s
7	BRKEN	R/W	See below
6*	NBD1	R/	Number of banks on daughter module
5†	NBM1	R/	Number of banks on system module
4	MNPRS	R/	1=monitor present. See below.
3*	P256KD	R/	0=64K parts; 1=256K parts on daughter module
2*	NBD0	R/	Number of banks on daughter module (bit 0)
1†	P256KM	R/	0=64K parts; 1=256K parts for system module
0†	NBM0	R/	Number of banks on system module (bit 0)

The bits in the CSR are also used to determine the amount of local memory on either the system module (M for x) or daughter (D for x) module.

The memory size of a particular module is explained below.

NBx1	NBx0	P256Kx	Definition
0	0	x	No memory on module x
0	1	0	128 kilobytes in 1 bank of 64K parts
1	0	0	256 kilobytes in 2 banks of 64K parts
1	1	0	512 kilobytes in 4 banks of 64K parts
0	1	1	512 kilobytes in 1 bank of 256K parts
1	0	1	1 megabyte in 2 banks of 256K parts
1	1	1	2 megabytes in 4 banks of 256K parts

NOTE

There is no commitment by DIGITAL to produce memory in all of these sizes.

* Bits 6,3,2 indicate the configuration of local memory on the daughter module.

† Bits 5,1,0 indicate the configuration of local memory on the mother module.

Bit 7 — BRKEN – Break Enable
This bit is used to enable hardware break detect on the printer port when that port is being used with a terminal. Mode register 1 of the printer port must be initialized before this bit is set (just like the Professional 350). When BRKEN is set, hardware break detection is enabled. When cleared, break detection is disabled. If a printer is connected to the port, break detection is disabled regardless of the state of the BRKEN bit. BRKEN is cleared at power-up.

Bit 4 — MNPRS – Monitor Present
This is a status bit to indicate that a video monitor is connnected to the video interface. MNPRS set indicates a monitor is present and cleared indicates no monitor present.

SSODT Register
The SSODT register is used for system debugging. The following list defines the SSODT register.

Bit	Name	Access	Meaning	
15	BCRAY	R/	0=OK	1=error in the B-state machine
14	CRAY	R/	0=OK	1=error in the M-state machine
13	JCRAY	R/	0=OK	1=error in the J-state machine
12–5		x/	not used	
4	SSODT	R/W	0=single stepping disabled 1=single stepping enabled if TERM L is low	
3–0		x/	Not used	

Maintenance Register
This register is used to identify the type of CPU and hardware configuration. It is always read as 16 bits of 0s. All 0s in bits <7:4> indicate a CTI Bus architecture product. Other PDP-11-based systems either do not respond to this address or supply non-zero data in bits 7–4. The address decoder responds to the 17777750 address to generate a reply signal, though no physical register corresponds to this location.

The 0s in the read data result from the default state of the DAL bus. Writes to this register have no effect, but will not cause a nonexistent memory trap since the address decoder still recognizes the address.

System Registers
All I/O registers in the address range 17777740 to 17777750 are considered system registers (sysreg) by the J11 and DC365. Any access to an address in this range will execute as an access to the maintenance register at location 17777750.

6.4.3 DC362 I/O Interface Gate Array

The DC362 I/O interface gate array handles all system interrupt and all DMA activity. It also provides an interface between the J11 and all local I/O devices.

6.4.3.1 Interrupt Controller Registers – Each of the interrupt controllers has a pair of registers which are used to control all interrupts. The registers are 7 bits wide in all three controllers. These registers are manipulated under program control by writing commands into the DC362 I/O interface gate array CSR registers. All the interrupt controller registers are read as all 0s. Writes to the reserved registers or to the high bytes of the CSR registers have no effect.

The following list shows the locations of the DC362 I/O interface gate array interrupt controller CSR registers.

Addresses	
17773200	Reserved
17773202	Interrupt controller 0 CSR register
17773204	Reserved
17773206	Interrupt controller 1 CSR register
17773210	Reserved
17773212	Interrupt controller 2 CSR register

Interrupt requests are received at a request level from 0 to 6 (0 to 7 for interrupt controller 0). Request level 0 is the highest priority and request level 7 is the lowest priority. Certain bits within certain internal registers correspond to certain request levels.

For example, an 8-bit interrupt mask register is used to enable or disable the eight interrupts. Setting bit 02 in the mask register will disable the interrupt at request level 2; clearing bit 05 in the mask register will enable the interrupt at request level 5.

NOTE

The IRQ7 L signal for interrupt controller 0 can interrupt at level 0 as well as level 7.

This allows the lowest level interrupt in controller 0 (TOD clock) to become the highest level interrupt. There is still one request bit but it can be set or cleared under program control as a request at level 0 or at level 7. There are two separate interrupt mask bits, one for level 0 and one for level 7. If the request bit is set and the level 0 mask is cleared, the highest level interrupt in interrupt controller 0 will occur (level 0). The request bit will be cleared if the interrupt is acknowledged. This means that the level 7 interrupt will not occur even if the level 7 mask bit is cleared. To get the level 7 interrupt, the level 7 mask bit must be cleared and the level 0 mask bit must be set.

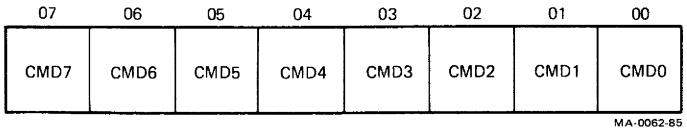
Interrupt Request Register (IRR)

The IRR stores the active transitions on the interrupt lines. A bit in the IRR is set whenever the corresponding interrupt request line makes a high to low transition. An IRR bit is cleared when the processor acknowledges the interrupt. IRR bits can be cleared or set by the processor by writing special commands into the controller CSR. The IRR bits are cleared at power up.

Interrupt Mask Register (IMR)

The IMR is used to enable or disable each of the individual interrupt requests. Setting an IMR bit disables the corresponding interrupt request, while clearing an IMR bit enables the corresponding interrupt request. Only unmasked IMR bits will cause a CPU interrupt. The state of an IMR bit has no effect on the operation of its IRR bit. IMR bits can be cleared by writing special commands into the controller CSR. The IMR bits are all set at power up.

Control/Status Register (CSR)
The CSR serves as a command register on writes and is all 0s on reads. Commands are written into the CSR to select specific controller operation.



Bits 7–0 CMD7–CMD0 – Command/write-only bits. These bits determine the command to the controller. The available commands are given below.

Reset – 0 0 0 0 0 0 0 0
The Reset command establishes a known state in the controller. The interrupt mask register is set to all 1s. The interrupt request register is cleared to all 0s.

Clear IRR and IMR – 0 0 0 1 0 X X X
All bits in the interrupt request register and the interrupt mask register are cleared.

Clear Single IRR and IMR – 0 0 0 1 1 B2 B1 B0
The bit specified by B2–B0 is cleared in both the interrupt request register and the interrupt mask register.

Clear IMR – 0 0 1 0 0 X X X
The interrupt mask register is cleared to all 0s.

Clear Single IMR Bit – 0 0 1 0 1 B2 B1 B0
The bit specified by B2–B0 is cleared in the interrupt mask register.

Set IMR – 0 0 1 1 0 X X X
The interrupt mask register is set to all 1s.

Set Single IMR Bit – 0 0 1 1 1 B2 B1 B0
The bit specified by B2–B0 is set in the interrupt mask register.

Clear IRR – 0 1 0 0 0 X X X
The interrupt request register is cleared to all 0s.

Clear Single IRR Bit – 0 1 0 0 1 B2 B1 B0
The bit specified by B2–B0 is cleared in the interrupt request register.

Set IRR – 0 1 0 1 0 X X X
The interrupt request register is set to all 1s.

Set Single IRR Bit - 0 1 0 1 1 B2 B1 B0
The bit specified by B2–B0 is set in the interrupt request register.

For the above commands that use B2–B0, the bit specified is as follows.

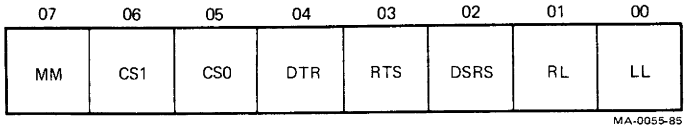
B2	B1	B0	Bit	
0	0	0	0	LSB
0	0	1	1	
0	1	0	2	
0	1	1	3	
1	0	0	4	
1	0	1	5	
1	1	0	6	
1	1	1	7	MSB

Some of these combinations do not exist (B2–B0=111 for interrupt controllers 2 and 3). Setting the IRR with these combinations will not cause an interrupt to the processor.

6.4.3.2 Modem Control and Baud Rate Registers – The following list shows the location of the DC362 I/O interface gate array modem and baud rate registers.

Addresses	
17773310	Modem Control Register 0
17773312	Modem Control Register 1
17773314	Baud Rate Register

Modem Control Register 0 - Address 17773310
The following list shows the location of the DC362 I/O interface gate array modem registers and baud rate register.



Bit 07 MM - Maintenance Mode. It is a read/write bit that is used to put the communication port in data loopback. When cleared, the receive data signal from the communication connector, CRXD, is passed onto the USART receive data signal, URXD. Also, the USART transmit data signal, UTXD, is passed onto the connector transmit data signal, CTXD. When set, UTXD is passed onto URXD providing data loopback on the USART. Also, CRXD is ignored and CTXD is held in the high state. Cleared at power up or by a RESET instruction.

Bit 06–05

CS1–CS0 – Clock Source. They are read/write bits that select the source of the transmit and receive baud rate clocks to the communication channel. The clock sources can be either the internal baud rate generators or the modem. The communication port is also capable of providing the transmit clock to the modem. The following list indicates how the selection is made.

		Sources for Clocks		
CS1	**CS0**	**URXC**	**UTXC**	**COTXC**
0	0	RBRG	TBRG	NONE
0	1	CIRXC	CITXC	NONE
1	0	CIRXC	TBRG	TBRG
1	1	TBRG	TBRG	NONE

URXC – receive clock output to communication USART

UTXC – transmit clock output to communication USART

COTXC – transmit clock output to modem connector

RBRG – internal receiver baud rate generator

TBRG – internal transmitter baud rate generator

CIRXC – receive clock input from the modem connector

CITXC – transmit clock input from the modem connector

NONE – no clock sent (signal is held high), cleared at power up or by a RESET instruction.

Bit 04

DTR – Data Terminal Ready. It is a read/write bit that, when set, the CDTR signal is asserted high to the modem connector. When cleared, the CDTR signal is unasserted to the modem connector. It is cleared at power up or by a RESET instruction.

Bit 03

RTS – Request To Send. It is a read/write bit that, when set, the CRTS signal is asserted high to the modem connector. When cleared, the CRTS signal is unasserted to the modem connector. It is cleared at power up or by a RESET instruction.

Bit 02

DSRS – Data Signaling Rate Select. It is a read/write bit that, when set, the CDSRS signal is asserted high to the modem connector. When cleared, the CDSRS signal is unasserted to the modem connector. It is cleared at power up or by a RESET instruction.

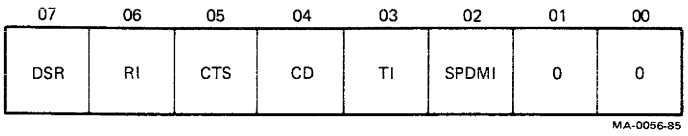
Bit 01

RL – Remote Loopback. It is a read/write bit that, when set, the CRL signal is asserted high to the modem connector. When cleared, the CRL signal is unasserted to the modem connector. It is cleared at power up or by a RESET instruction.

Bit 00

LL – Local Loopback. It is a read/write bit that, when set, the CLL signal is asserted high to the modem connector. When cleared, the CLL signal is unasserted to the modem connector. It is cleared at power up or by a RESET instruction.

Modem Control Register 1 – Address 17773312



Bit 07 — DSR – Data Set Ready. It is a read-only bit that reflects the state of the CDSR signal from the modem connector. A 1 indicates that CDSR is asserted and a 0 indicates that it is unasserted. A transition of this signal will generate a modem change interrupt, IRQ4 L, to the first interrupt controller.

Bit 06 — RI – Ring Indicator. It is a read-only bit that reflects the state of the CRI signal from the modem connector. A 1 indicates that CRI is asserted and a 0 indicates that it is unasserted. A transition of this signal will generate a modem change interrupt, IRQ4 L, to the first interrupt controller.

Bit 05 — CTS – Clear To Send. It is a read-only bit that reflects the state of the CCTS signal from the modem connector. A 1 indicates that CCTS is asserted and a 0 indicates that it is unasserted. A transition of this signal will generate a modem change interrupt, IRQ4 L, to the first interrupt controller.

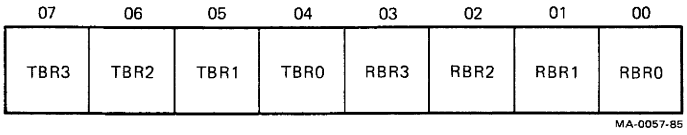
Bit 04 — CD – Carrier Detect. It is a read-only bit that reflects the state of the CCD signal from the modem connector. A 1 indicates that CCD is asserted and a 0 indicates that it is unasserted. A transition of this signal will generate a modem change interrupt, IRQ4 L, to the first interrupt controller.

Bit 03 — TI – Test Indicator. It is a read-only bit that reflects the state of the CTI signal from the modem connector. A 1 indicates that CTI is asserted and a 0 indicates that it is unasserted.

Bit 02 — SPDMI – Speed Mode Indicator. It is a read-only bit that reflects the state of the CSPDMI signal from the modem connector. A 1 indicates that CSPDMI is asserted and a 0 indicates that it is unasserted.

Bits 01–00 — N/U – not used. They are read-only bits and are always read as 0s.

Baud Rate Register – Address 17773314



Bits 07–04

TBR3–TBR0 – Transmitter Baud Rate Select. They are write-only bits and are used to program the internal transmitter baud rate generator.

TBR3	TBR2	TBR1	TBR0	16 X Clock Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19200

At power up these bits are set to 1110.

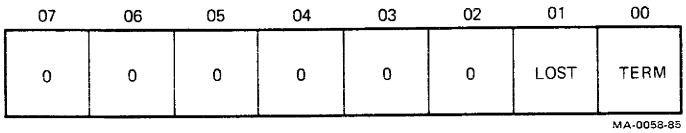
Bits 03–00

RBR3–RBR0 – Receiver Baud Rate Select. These bits are used to program the internal receiver baud rate generator.

RBR3	RBR2	RBR1	RBR0	16 X Clock Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19200

At power up these bits are set to 1110. Write-only bits.

6.4.3.3 Maintenance Status Register – This register is internal to the I/O gate array. It is accessed by reading the LED display register, 17773704.



Bits 07–02 They are not used and are read-only bits that are always read as 0s.

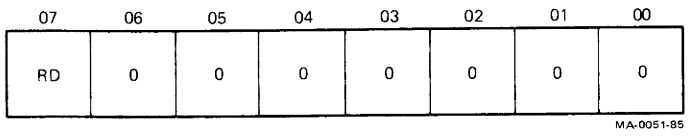
Bit 01 LOST – Loop On Self-Test. It is a read-only bit that reflects the state of the LOST L signal. When high, it indicates that LOST L is asserted low. When low, it indicates that LOST L is unasserted or high.

Bit 00 TERM – Terminal. It is a read-only bit that reflects the state of the TERM L signal. When high, it indicates that TERM L is asserted low. When low, it indicates that TERM L is unasserted or high.

6.4.3.4 Maintenance Terminal Registers – The following list shows the location of the maintenance terminal registers.

Address	
17777560	Receiver CSR
17777562	Receiver Data Buffer
17777564	Transmitter CSR
17777566	Transmitter Data Buffer

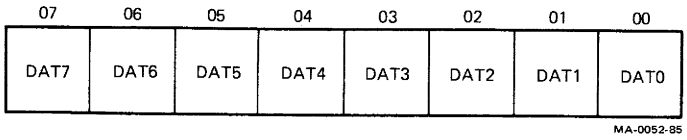
Receiver Control Status Register (RCSR) – Address 17777560



Bit 07 RD – Receiver Done. It is a read-only bit that is used to indicate that a character has been received by the interface receiver. Each time a new character is received, the RD bit is set. RD is cleared by reading the receiver data buffer register or by a RESET.

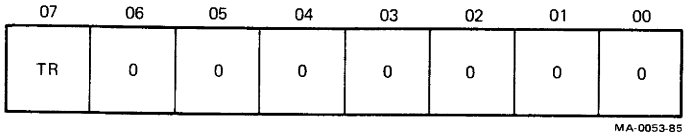
Bits 06–00 Not used. They are read-only bits and are always read as 0s.

Receiver Data Buffer Register (RBUF) – Address 17777562



Bits 07–00 — DAT7–DAT0 – Data. They are read-only bits. This register contains the last received character. Reading the register will clear RD. Writes to the register will have no effect on the data in the register nor the RD bit.

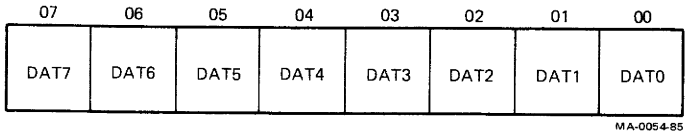
Transmitter Control Status Register (XCSR) – Address 17777564
The XCSR is a read-only register using only the low byte. A read of the high byte results in all 0s and writes have no effect.



Bit 07 — TR – Transmitter Ready. It is a read-only bit that is used to indicate that the transmitter data buffer register is ready to be loaded with another character. Each time the transmitter data buffer is loaded, the TR bit is cleared. TR is set by a RESET or when the transmitter data buffer becomes ready.

Bits 06–00 — Not used. They are read-only bits that are always read as 0s.

Transmitter Data Buffer Register (XBUF) – Address 17777566
This is a write-only register (low byte only).



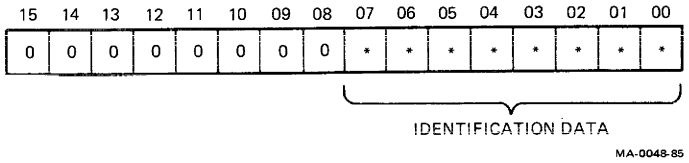
Bits 07–00 — DAT7–DAT0 – Data/Write-only bits. This register should be loaded with characters to be transmitted. Writing the register will clear TR. Reading the register will return unpredictable data and will have no effect on the TR bit.

6.4.4 Video Generation Integrated Logic

Video registers appear as "logical slot 6" (64K words/128K bytes) in the J11 address space.

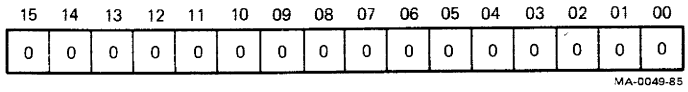
Identification Register (IDR) – Address 17775402

The IDR will show a 16-bit ID of 50(8) or 28(H) if no EBO option module is installed; 10050(8) or 1028(H) with an EBO option module that has a color map array device.



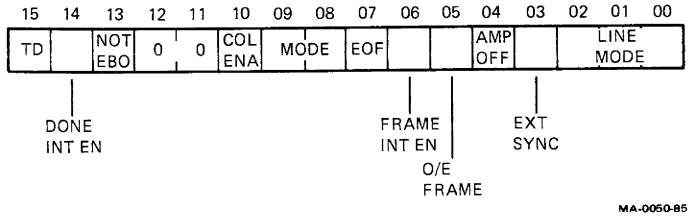
ROM Address Register (RAR)

The ROM address register provides CTI Bus compatibility. Refer to the *CTI Bus Technical Manual* for detailed information concerning the use of this register.



Control Status Register

The control status register address equals the slot base address plus 4.



(slot 6)
17775400 + 4 → 17775404

This register initializes the general operation and frame timing of the video generator and the EBO.

NOTE
"End of Frame" uses CTI interrupt line A. "Transfer Done" uses CTI interrupt line B. "A" interrupts are honored before "B" interrupts.

Registers should not be loaded unless the transfer done bit is set. X, Y and Pattern register are an exception. They may be loaded while an operation is in progress without effecting that operation.

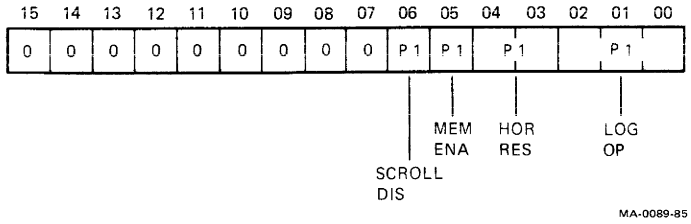
Bit 15	Transfer done. It is a read-only bit. Set if counter register=0. The logical AND of "done interrupt enable" and "transfer done" will generate a B interrupt for slot 6.
Bit 14	Done interrupt enable. It is a read/write bit. 1=allows B interrupt to occur. 0=B interrupt may not occur. Initialize to 0.
Bit 13	EBO is not connected. It is a read-only bit. 1=EBO not connected 0=EBO connected
Bits 12, 11	Reserved
Bit 10	Color map enable. It is a read/write bit. 1=enable color map 0=disable color map. Power up to 0.
Bit 09–08	Mode of operation. It is a read/write bit. Init to 0. See below. 0=bit transfer left → right 1=bit transfer top → bottom 2=word transfer left → right 3=word transfer right → left
Bit 07	End of frame. It is a read-only bit. 1 during vertical retrace time. The logical AND of "frame interrupt enable" and "end of frame" will generate an A interrupt for slot 6.
Bit 06	Frame interrupt enable. It is a read/write bit. 1=A interrupt is allowed. 0=A interrupt may not occur. Init to 0.
Bit 05	Odd/even frame. It is a read-only bit. It is set in interlaced mode when scanning the even frame. Cleared otherwise.
Bit 04	Video amplifiers off. It is a read/write bit. Set turns off all video amplifiers on the system board, leaving just the 75 ohm termination resistors. Power up to 0.

Bit 03 — Externally synchronized. It is a read only bit.
1=chip is in slave mode. Horizontal and vertical sync are inputs.
0=chip is in master mode. Horizontal and vertical sync are created internally and are outputs.

Bits 02–00 — Line mode. It is a read/write bit.
Power up to 0.
See below.

n	#Visible	#Lines	Interlace	Frames
0	240	263	no	60
1	256	313	no	50
2	240	525	yes	30
3	256	625	yes	25
4	480	525	yes	30
5	512	625	yes	25
6	reserved	–	–	–
7	reserved	–	–	–

Plane 1 Control Register (Blue)
The plane 1 control register address is equal to the slot base address +6.



(slot 6)
17775400 + 6 → 17775406
The CTI Bus writes to all planes that have the plane memory bit set. The bus reads from the first plane that has the bit set, in 1, 2, 3 order. If no plane has the bit set, any attempt to access the video memory will cause a CTI Bus time-out.

The shift screen operation shifts all bits in the words specified by the counter register either left or right. Bits shifted from the left or right side of the sceen are lost. The incoming bits are from the least significant bit of the pattern register.

Bits 15–8 — Reserved

Bit 7 — Reserved

Bit 6 — Plane 1 scroll disable
Power up to 0
1=scrolling of first page in plane 1 disabled.

Bit 5

Plane 1 memory enable.
Initialize to 0.
1=respond to processor memory cycles if within address range of video memory.
0=do not respond to processor memory cycles.

Bits 4–3

Plane 1 horizontal resolution.
Power up to 3.
0=1024 * 1 (2 intensity levels)
1= 512 * 2 (4 intensity levels)
2= 256 * 4 (16 intensity levels)
3=display off (black)

Bits 2–0

Plane logic operation.
Initialize to 0.
(if CSR[8,9] is bitmode)
0=No-op
1=XOR pattern to screen
2=Move pattern to screen
3=Move pattern "not" to screen
4=Bitset pattern to screen
5=Bitclear pattern to screen
6=Clear current bit on screen
7=Set current bit on screen

(if CSR[8,9] is wordmode)
0=No-op
1=Complement screen
2=Move pattern to screen
3=Move pattern "not" to screen
4=(reserved)
5=Shift screen 1 bit
6=Shift screen 2 bits
7=Shift screen 4 bits

(if CSR[8,9] is 2, shift is right)
(if CSR[8,9] is 3, shift is left)

Option Plane Control Register (Green and Red)

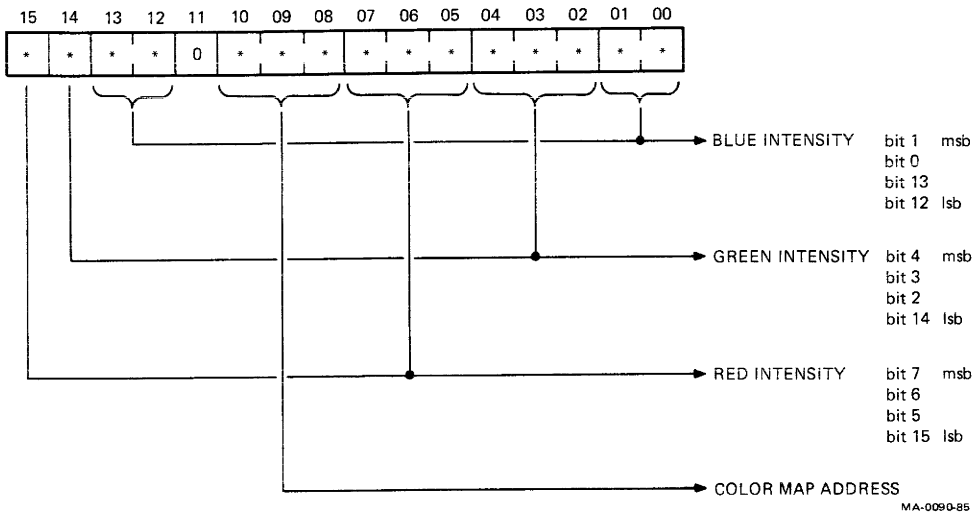
The option plane control register address is equal to the slot base address +10; 17775410.

This register is byte addressable. When the EBO is not installed, writes to this register have no effect and reads will always yield the initial value of 30_8 in each byte.

Bits 15–8 apply to plane 3 (red). Bits 7–0 apply to plane 2 (green). Refer to the plane 1 (blue) color register bits 7–0 description for bit definitions of option plane control register.

Color Map Control Register – Write-Only
The color map control register address is equal to the slot base address +12; 17775412.

Bits 8, 9, and 10 select one of eight map locations to receive color intensity information. The three color groups select values that are converted to analog levels to drive the three color guns in a color monitor.

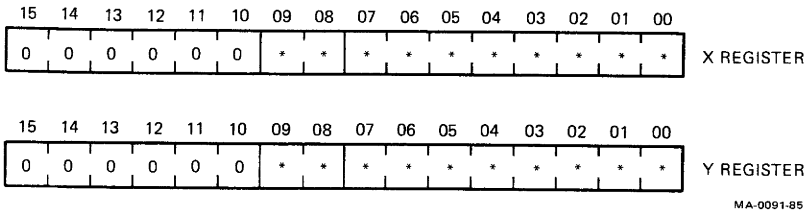


Scroll Register – Read/Write
The scroll register address is equal to the slot base address +14; 17775414.

Changing the contents of the scroll register causes a vertical scroll on the screen (increment scrolls up; decrement scrolls down). Operations with the scroll register can be absolute. However, the scroll register may have any value when your program starts. Therefore, you should increment/decrement, add/subtract to the contents of the register.

Bits 15–9	Reserved
Bits 8–0	In 240 line mode the content of the 8 least significant bits of the scroll register cause the first page (256 lines per screen) to scroll (in the planes that don't have the scroll disable bit set), and does not effect the three other pages. The content of the 2 most significant bits in the scroll register scroll the four pages. The scroll register is byte addressable for backward compatibility (INCB @#SCL has the same effect on the Professional 350 as the Professional 380). In 480 line mode the content of the 9 least significant bits of the scroll register cause the first page (512 lines per screen) to scroll (in the planes that do not have the scroll disable bit set), and does not effect the second page. The content of the most significant bit in the scroll register "swap" the 2 pages.

X and Y Registers - Read/Write
The X register address is equal to the slot base address plus 16; 17775416. The Y register address is equal to the slot base address +20; 17775420.



The X and Y registers hold the start coordinate of all transfers to the screen and are not the actual counters so they can be modified at any time during the transfer. The contents of the registers are loaded into counters when the transfer done bit is set. In word mode, the low 4 bits of X are ignored. In word mode right to left, X is the coordinate of the rightmost word. Y is still the coordinate of the top.

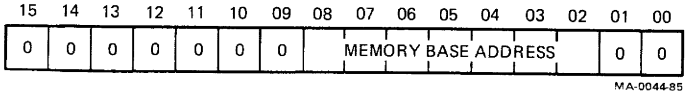
Counter Register - Read/Write
The counter register address is equal to the slot base address +22; 17775422.

When the counter is loaded with anything but 0, a transfer is started. The transfer decrements the counter until the counter is 0. When 0, the counter is stopped and the transfer done bit CSR[15] is set to "1". The counter can only be loaded if the transfer done bit is set. An attempt to load the counter while the transfer done bit is not will result in a no-op. Loading the counter register clears the transfer done bit. The counter register is a read/write register, however the counter is constantly changing states and the value read has a high probability of being incorrect. This feature is mainly there for diagnostic purpose.

Pattern Register - Read/Write
The pattern register address is equal to the slot base address plus 24; 17775424.

In word mode only, the least significant bit of the pattern register is used. The upper 15 bits are ignored. The pattern register is double buffered and can be loaded even when an operation is in progress. The content of the first buffer is transferred to the second buffer when the transfer done bit is set.

Memory Base Register - Read/Write
The memory base register address is equal to the slot base address plus 26; 17775426.



This register controls the address of the video memory in the processors address space. The memory addresses are programmable to any 128 kilobyte boundary with the register.

6.4.5 Printer Interface Port

The following list shows the location of the printer port registers.

Addresses

17773400	Data buffer register
17773402	Status register
17773404	Mode registers
17773406	Command register

All printer port registers use only the low byte. The high bytes are always read as 0s. After the power-up self-test is completed, the firmware initializes the printer port as below.

Mode Register 1

1 stop bit
parity disabled
8 bits per character

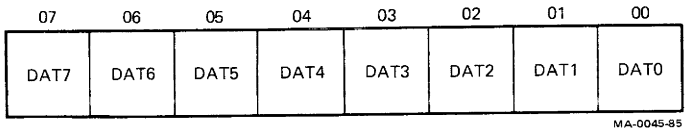
Mode Register 2

9600 baud if terminal cable is connected to J6
4800 baud if printer cable/no cable connected to J6

Command Register

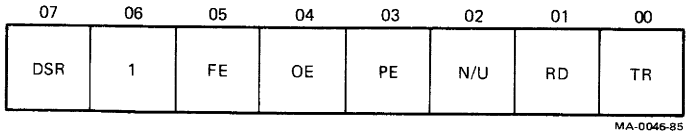
normal operation
RTS enabled
force break disabled
receiver enabled
DTR enabled
transmitter enabled

Data Buffer Register (DBUF) – Address 17773400



Bits 07–00 — DAT7–DAT0 – Data. They are read/write bits. On read operations, this register serves as the receiver holding register and contains the last received character. The character is right justified if the character length is less than eight. On write operations, this register serves as the transmitter holding register and should be loaded with the next character to be transmitted.

Status Register (STAT) – Address 17773402



Bit 07 — DSR – Data Set Ready. It is a read-only bit that reflects the state of the DSR signal input and can be used to determine that the printer is connected and ready. When DSR is set, it indicates that the DSR signal input is asserted and so the printer is present and ready. When DSR is cleared, it indicates that the DSR signal input is unasserted and so the printer is either not present or not ready.

Bit 06 — Not used. It is a read-only bit and is always read as a 0.

Bit 05 — FE – Framing Error. It is a read-only bit that, when set, indicates that the received character was not framed by the programmed number of stop bits. If the received character is all 0s and FE is set, a break condition was detected. When cleared, FE indicates that the received character was properly framed. FE can be cleared by disabling the receiver or by a reset error command in the command register.

Bit 04 — OE – Overrun Error. It is a read-only bit that, when set, indicates that the previous character loaded into the receiver holding register was not read by the processor by the time that a new received character was loaded into it. When cleared, no overrun condition occurred. OE can be cleared by disabling the receiver or by a reset error command in the command register.

Bit 03 — PE – Parity Error. It is a read-only bit that, when set, indicates that the received character had a parity error. When cleared, no parity error was detected. This bit will only function when parity is enabled. PE can be cleared by disabling the receiver or by a reset error command in the command register.

Bit 02 — Not used. It is a read-only bit.

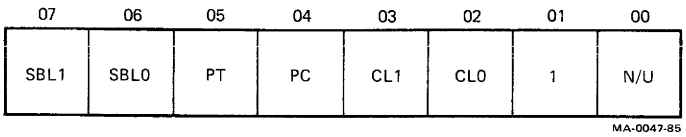
Bit 01 — RD – Receiver Done. It is a read-only bit that, when set, indicates that a character has been received and loaded into the receiver holding register for the processor to read. When cleared, it indicates that no new character has been loaded into the receiver holding register. RD can be cleared by reading the receiver holding register or by disabling the receiver in the command register. RD will not be set when characters are received if remote loopback mode is enabled in the command register.

Bit 00 — TR – Transmitter Ready. It is a read-only bit that is only valid when the transmitter is enabled in the command register. When TR is cleared, it indicates that the transmitter holding register is not ready to receive another character for transmission from the processor. When set, it indicates that the processor may load the next character for transmission into the transmitter holding register. TR will be cleared when operating in auto echo or remote loopback modes.

Mode Registers (MR1 and MR2) – Address 17773404

There are two mode registers used to select the operating mode of the printer port. Both registers reside at the same address. Operations (read or write) to a mode register will cause an internal pointer to point to the other mode register for the next operation. Reading the command register will always cause the internal pointer to point to mode register 1. Both mode registers will be cleared when system power is turned on. The processor will have to initialize both registers to the desired mode of operation. The two mode registers are described below.

Mode Register 1 (MR1)



Bits 07–06 SBL1–SBL0 – Stop Bit Length. They are read/write bits that select character framing of 1, 1.5, or 2 stop bits for both the transmitter and the receiver. The stop bits are selected as follows.

SBL1	SBL0	Stop Bit Length
0	0	invalid
0	1	1 stop bit
1	0	1.5 stop bits
1	1	2 stop bits

Bit 05 PT – Parity Type. It is a read/write bit that, when set, selects even parity. When cleared, PT selects odd parity. Parity type is the same for the transmitter and the receiver. This bit has no effect if parity is not enabled.

Bit 04 PC – Parity Control/Read/Write. When cleared, parity is disabled for the transmitter and the receiver. When set, the transmitter adds a parity bit to the transmitted character and the receiver performs a parity check on incoming characters. The PT bit selects odd or even parity.

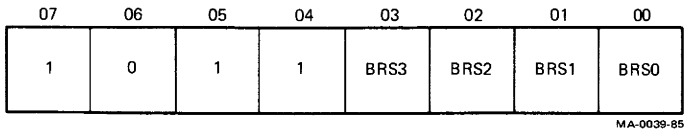
Bits 03–02 CL1–CL0 – Character Length. They are read/write bits that select the number of data bits per character for the transmitter and the receiver. (The character length does not include the parity bit if any, the start bit, or the stop bits.) Character length is selected as follows.

CL1	CL0	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 01 It is a read/write bit that must always be set to a 1 for proper operation. When the system power is turned on, this bit will be cleared. The processor must set it to a 1 before attempting to use the printer port.

Bit 00 Not used. It is a read/write bit.

Mode Register 2 (MR2)



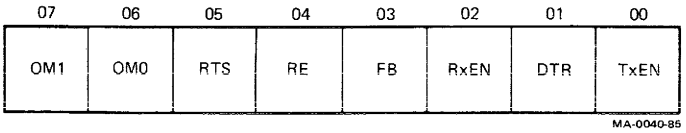
Bits 07–04 They are read/write 1011 bits. These bits must always be programmed to 1011 for proper operation. When the system power is turned on, these bits will be cleared. The processor must program them before attempting to use the printer port.

Bits 03–00 BRS3–BRS0 – Baud Rate Select. They are read/write bits that determine the frequency of the internal baud rate generator. The frequency is 16 times the selected baud rate. These bits select the clock for both the transmitter and receiver. The baud rate is selected as follows.

BRS3	BRS2	BRS1	BRS0	Baud Rate	Percent Error
0	0	0	0	50	–0.5682
0	0	0	1	75	–0.5682
0	0	1	0	110	–0.5682
0	0	1	1	134.5	–0.5517
0	1	0	0	150	–0.5682
0	1	0	1	300	–0.5682
0	1	1	0	600	–0.5682
0	1	1	1	1200	–0.5682
1	0	0	0	1800	–0.5682
1	0	0	1	2000	–0.3165
1	0	1	0	2400	–0.5682
1	0	1	1	3600	–0.5682
1	1	0	0	4800	–0.5682
1	1	0	1	7200	–0.5682
1	1	1	0	9600	–0.5682
1	1	1	1	19200	+2.5391

Command Register (CMD) - Address 17773406

The command register also controls the operation of the printer port. The command register will be cleared when system power is turned on. The processor will have to initialize the register to the desired mode of operation.



Bits 07–06 OM1–OM0 – Operating Mode/Read/Write. These bits select the operating mode of the port as follows.

OM1	OM0	Operating Mode
0	0	normal operation
0	1	automatic echo mode
1	0	local loopback
1	1	remote loopback

These modes are described below.

Normal – The transmitter and receiver operate independently in accordance with the mode and status registers.

Automatic Echo – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled. The receiver will continue to assert receiver done each time a character is received but the transmitter will no longer assert Transmitter Ready. Only the first character of a break condition is echoed. The transmitter will go to the mark state until the next valid start is detected.

Local Loopback – In this mode, the transmitter output is connected to the receiver input internally. The external transmitter output is held in the mark state. The transmitter must be enabled but the receiver need not be enabled (see RxEN and TxEN bits). The DTR and RTS bits must both be set for local loopback to function properly.

Remote Loopback – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver will no longer assert Receiver Done each time a character is received and the transmitter will no longer assert Transmitter Ready. Only the first character of a break condition is echoed. The transmitter will go to the mark state until the next valid start is detected. (The error status bits, PE, OE, and FE will still function in this mode.)

Bit 05 RTS – Request To Send. It is a read/write bit. There is no external hardware support for this signal. However, it must be set for local loopback mode to function properly (see OM1–OM0 bits).

Bit 04 RE – Reset Error. It is a write-once bit. Setting RE causes the error bits, PE, OE, and FE in the status register to be cleared. It is always read as a 0.

Bit 03	FB – Force Break. It is a read/write bit. When cleared, normal transmitter operation will occur. When set, the transmitter output signal will enter and hold the space condition at the end of the current transmitted character.
Bit 02	RxEN – Receiver Enable. It is a read/write bit. When set, the receiver is enabled for normal operation. When cleared, the receiver will immediately terminate operation and unassert receiver done. Disabling the receiver will clear the error bits, PE, OE, and FE in the status register.
Bit 01	DTR – Data Terminal Ready. It is a read/write bit. When set, the data terminal ready signal is asserted on the printer port connector. When cleared, the DTR signal is unasserted on the printer connector. This bit must be set for local loopback mode to function properly (see OM1–OM0 bits).
Bit 00	TxEN – Transmitter Enable. It is a read/write bit. When set, the transmitter is enabled for normal operation. When cleared, the transmitter will be disabled. If the transmitter is disabled, it will complete the transmission of any character that has already begun before terminating operation. (This does not mean a character pending in the transmitter holding register.) When disabled, the transmitter output will remain in the mark state and the transmitter ready bit will be unasserted.

6.4.6 Keyboard Interface Port

The following list shows the address locations of the keyboard interface port registers.

Addresses	
17773500	Data buffer register
17773502	Status register
17773504	Mode registers
17773506	Command register

Vectors	
200	Receiver
204	Transmitter

The mode of operation is completely programmable as described in the following sections. When using the port with the Professional computer system keyboard, the mode must be set to the following conditions.

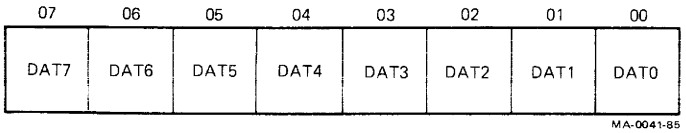
1. 8 bit character length
2. no parity
3. 1 stop bit
4. 4800 baud clock rate

After the power-up self-test is completed, the firmware initializes the keyboard port as shown below.

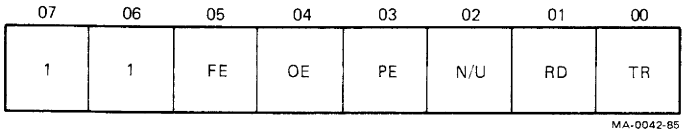
Mode Register 1
1 stop bit
parity disabled
8 bits per character

Mode Register 2
4800 baud

Command Register
normal operation
RTS enabled
force break disabled
receiver enabled
DTR enabled
transmitter enabled



Bits 07–00 — DAT7–DAT0 – Data. They are read/write bits. On read operations, this register serves as the receiver holding register and contains the last received character. The character is right justified if the character length is less than eight. On write operations, this register serves as the transmitter holding register and should be loaded with the next character to be transmitted.



Bits 07–06 — Not used. They are read-only bits and are always read as 1s.

Bit 05 — FE – Framing Error. It is a read-only bit that, when set, indicates that the received character was not framed by the programmed number of stop bits. If the received character is all 0s and FE is set, a break condition was detected. When cleared, FE indicates that the received character was properly framed. FE can be cleared by disabling the receiver or by a reset error command in the command register.

Bit 04 — OE – Overrun Error. It is a read-only bit that, when set, indicates that the previous character loaded into the receiver holding register was not read by the processor by the time that a new received character was loaded into it. When cleared, no overrun condition occurred. OE can be cleared by disabling the receiver or by a reset error command in the command register.

Bit 03 — PE – Parity Error. It is a read-only bit that, when set, indicates that the received character had a parity error. When cleared, no parity error was detected. This bit will only function when parity is enabled. PE can be cleared by disabling the receiver or by a reset error command in the command register.

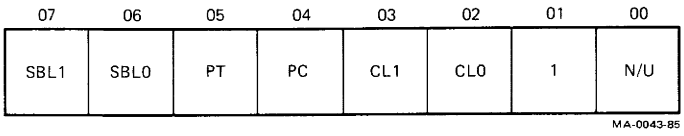
Bit 02 — N/U – Not used. It is a read-only bit.

Bit 01 — RD – Receiver Done. It is a read-only bit that, when set, indicates that a character has been received and loaded into the receiver holding register for the processor to read. When cleared, it indicates that no new character has been loaded into the receiver holding register. RD can be cleared by reading the receiver holding register or by disabling the receiver in the command register (see section on command register). RD will not be set when characters are received if remote loopback mode is enabled in the command register.

Bit 00 — TR – Transmitter Ready. It is a read-only bit that is only valid when the transmitter is enabled in the command register. When TR is cleared, it indicates that the transmitter holding register is not ready to receive another character for transmission from the processor. When set, it indicates that the processor may load the next character for transmission into the transmitter holding register. TR will be cleared when operating in auto echo or remote loopback modes.

Mode Registers (MR1 and MR2) – Address 17773504

There are two mode registers used to select the operating mode of the keyboard port. Both registers reside at the same address. Operations (read or write) to a mode register will cause an internal pointer to point to the other mode register for the next operation. Reading the command register will always cause the internal pointer to point to mode register 1. Both mode registers will be cleared when system power is turned on. The processor will have to initialize both registers to the desired mode of operation.



Bits 07–06 — SBL1–SBL0 – Stop Bit Length. They are read/write bits that select character framing of 1, 1.5, or 2 stop bits for both the transmitter and the receiver. The stop bits are selected as follows.

SBL1	SBL0	Stop Bit Length
0	0	Invalid
0	1	1 stop bit
1	0	1.5 stop bits
1	1	2 stop bits

Bit 05 — PT – Parity Type. It is a read/write bit that, when set, selects even parity. When cleared, it selects odd parity. Parity type is the same for the transmitter and the receiver. This bit has no effect if parity is not enabled.

Bit 04

PC – Parity Control. It is a read/write bit. When cleared, parity is disabled for the transmitter and the receiver. When set, the transmitter adds a parity bit to the transmitted character and the receiver performs a parity check on incoming characters. The PT bit selects odd or even parity.

Bits 03–02

CL1–CL0 – Character Length. They are read/write bits that select the number of data bits per character for the transmitter and the receiver. Character length is selected as follows.

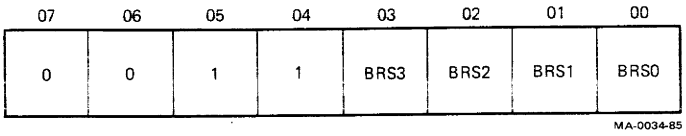
CL1	CL0	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 01

01. It is a read/write bit that must always be set to a 1 for proper operation. When the system power is turned on, this bit will be cleared. The processor must set it to a 1 before attempting to use the keyboard port.

Bit 00

N/U – Not used. It is a read/write bit.



Bits 07–04

0011. They are read/write bits that must always be programmed to 0011 for proper operation. When the system power is turned on, these bits will be cleared. The processor must program them before attempting to use the keyboard port.

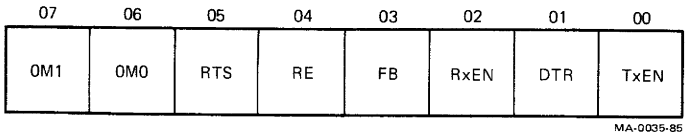
Bits 03–00

BRS3–BRS0 – Baud Rate Select. They are read/write bits that determine the frequency of the internal baud rate generator. The frequency is 16 times the selected baud rate. These bits select the clock for both the transmitter and receiver. The baud rate is selected as follows.

BRS3	BRS2	BRS1	BRS0	Baud Rate	Percent Error
0	0	0	0	50	–0.5682
0	0	0	1	75	–0.5682
0	0	1	0	110	–0.5682
0	0	1	1	134.5	–0.5517
0	1	0	0	150	–0.5682
0	1	0	1	300	–0.5682
0	1	1	0	600	–0.5682
0	1	1	1	1200	–0.5682
1	0	0	0	1800	–0.5682
1	0	0	1	2000	–0.3165
1	0	1	0	2400	–0.5682
1	0	1	1	3600	–0.5682
1	1	0	0	4800	–0.5682
1	1	0	1	7200	–0.5682
1	1	1	0	9600	–0.5682
1	1	1	1	19200	+2.5391

Command Register (CMD) – Address 17773506

The command register also controls the operation of the keyboard port. The command register will be cleared when system power is turned on. The processor will have to initialize the register to the desired mode of operation. The command register is described below.



Bits 07–06 OM1–OM0 – Operating Mode. They are read/write bits that select the operating mode of the port as follows.

OM1	OM0	Operating Mode
0	0	normal operation
0	1	automatic echo mode
1	0	local loopback
1	1	remote loopback

These modes are described below.

Normal – The transmitter and receiver operate independently in accordance with the mode and status registers.

Automatic Echo – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver will continue to assert receiver done each time a character is received but the transmitter will no longer assert transmitter ready. Only the first character of a break condition is echoed. The transmitter will go to the mark state until the next valid start is detected.

Local Loopback – In this mode, the transmitter output is connected to the receiver input internally. The external transmitter output is held in the mark state. The transmitter must be enabled but the receiver need not be enabled (see RxEN and TxEN bits). The DTR and RTS bits must both be set for local loopback to function properly.

Remote Loopback – Characters received in the receiver holding register are automatically loaded into the transmitter register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver will no longer assert receiver done each time a character is received and the transmitter will no longer assert transmitter ready. Only the first character of a break condition is echoed. The transmitter will go to the mark state until the next valid start is detected. (The error status bits, PE, OE, and FE will still function in this mode.)

Bit 05 RTS – Request To Send. It is a read/write bit. There is no external hardware support for this signal. However, it must be set for local loopback mode to function properly (see OM1–OM0 bits).

Bit 04 RE – Reset Error. It is a write-once bit. Setting RE causes the error bits, PE, OE, and FE in the status register to be cleared. It is always read as a 0.

Bit 03 FB – Force Break. It is a read/write bit. When cleared, normal transmitter operation will occur. When set, the transmitter output signal will enter and hold the space condition at the end of the current transmitted character.

Bit 02 — RxEN – Receiver Enable. It is a read/write bit. When set, the receiver is enabled for normal operation. When cleared, the receiver will immediately terminate operation and unassert receiver done. Disabling the receiver will clear the error bits, PE, OE, and FE in the status register.

Bit 01 — DTR – Data Terminal Ready. It is a read/write bit. There is no external hardware support for this signal. However, it must be set for local loopback mode to function properly (see OM1–OM0 bits).

Bit 00 — TxEN – Transmitter Enable. It is a read/write bit. When set, the transmitter is enabled for normal operation. When cleared, the transmitter will be disabled. If the transmitter is disabled, it will complete the transmission of any character that has already begun before terminating operation. (This does not mean a character pending in the transmitter holding register.) When disabled, the transmitter output will remain in the mark state and the transmitter ready bit will be unasserted.

6.4.7 Communication Interface Port

All the communication port registers use only the low byte. The high bytes are always read as all 0s and writes to the high bytes have no effects. The reserved register will respond to read and write accesses but reads will always produce all 0s and writes will have no effect.

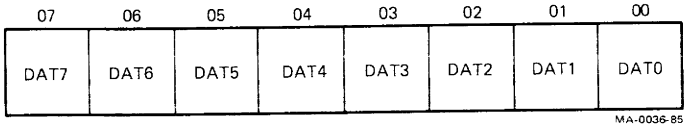
When the power-up self-test is completed, the firmware initializes the communication port. The firmware issues a channel reset command to both control/status register A and control/status register B. This will clear all the internal control registers in the communication USART. The firmware also loads the modem and baud rate registers as follows

modem control register 0=000
baud rate register=377

The following list shows the address location of the communication interface port registers.

Addresses	
17773300	Data buffer register
17773302	Control/status register A
17773304	Reserved
17773306	Control/status register B
17773310	Modem control register 0
17773312	Modem control register 1
17773314	Baud rate register

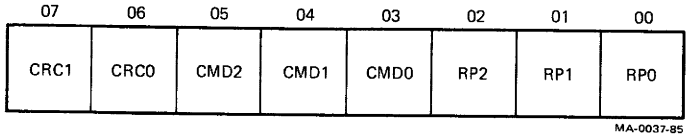
Vectors	
210	Receive/transmit
214	Modem change



Bits 07–00 — DAT7–DAT0 – Data. They are read/write bits. On read operations, this register contains data bytes received by the communication port. The receiver has a 3-byte buffer for holding received characters. On write operations, this register serves as a transmitter holding register and should be loaded with the next character to be transmitted.

Control/Status Register A – Address 17773302

This register serves as a window to 11 internal registers. The internal registers consist of 8 write registers and 3 read registers. The write registers are labeled WR0–WR7 and are used to control the various operating modes of the communication port. The read registers are labeled RR0–RR2 and provide status information. An internal pointer register selects which of the command or status registers will be read or written during an access to control/status register A. After reset, the contents of the pointer register are 0. The first write to the control/status register causes the data to be loaded into WR0. The 3 least significant bits of WR0 serve as the pointer register. The next access to the control/status register accesses the internal register selected by the pointer register. The pointer is reset after the read or write operation is completed.



Bits 07–06 CRC1–CRC0 – CRC Reset Code. They are write-only bits that, when written, have the following effect.

CRC1	CRC0	Effect
0	0	Null – it has no effect.
0	1	Reset receive CRC checker – it resets the CRC checker to 0s. If in SDLC mode, the CRC checker is set to all 1s.
1	0	Reset transmit CRC generator – it resets the CRC generator to 0s. If in SDLC mode, the CRC generator is set to all 1s.
1	1	Reset transmitter underrun/end of message latch.

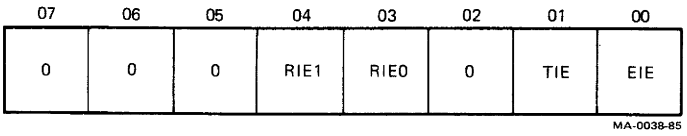
Bits 05–03

CMD2–CMD0 – Command Bits. They are write-only bits that determine which of seven commands will be performed.

Command	Effect
0	Null – it has no effect.
1	Send Abort – it causes the generation of eight to thirteen 1s when in SDLC mode.
2	Reset external/status interrupts – it resets the latched status bits of RR0 and reenables them, allowing interrupts to occur again.
3	Channel reset – it resets the latched status bits of RR0, the interrupt prioritization logic and all control registers in the channel. Two microseconds should be allowed for the channel reset time before any additional commands or controls are written into the channel.
4	Enable interrupt on next receive character – if the interrupt on first receive character mode is selected, this command reactivates that mode after each complete message is received to prepare for the next message.
5	Reset transmitter interrupt pending – if the transmit interrupt enable mode is selected the channel automatically interrupts when the transmit buffer becomes empty. When there are no more characters to be sent, issuing this command prevents further transmitter interrupts until the next character has been completely sent.
6	Error reset – error latches, parity, and overrun errors in RR1 are reset.
7	End of interrupt – resets the interrupt-in-service latch of the highest priority internal device under service and allows lower priority devices to interrupt.

Bits 02–00

RP2–RP0 – Register Pointer bits. They are write-only bits that determine which write register the next byte is to be written into or which read register the next byte is to be read from. After reset, the first byte written goes into WR0. Following a read or a write to any register (except WR0) the pointer will point to WR0.



Bits 07–05 N/U – Not used. They are write-only bits that must always be written as 0s.

Bits 04–03 RIE1–RIE0 – Receiver Interrupt Enable bits. They are write-only bits that enable receiver interrupts in the following modes.

RIE1	RIE0	Function
0	0	Disable receiver and special condition interrupts
0	1	Enable interrupt on first received character only or special condition
1	0	Enable interrupt on all receive characters or special condition (parity error is a special receive condition)
1	1	Enable interrupt on all receive characters or special condition (parity error is not a special receive condition)

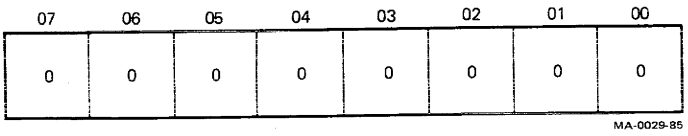
Bit 02 N/U – Not used. It is a write-only bit that must always be written as 0.

Bit 01 TIE – Transmitter Interrupt Enable. It is a write-only bit that, when set, allows transmitter interrupts to occur when the transmitter buffer becomes empty. When cleared, no transmitter interrupts will occur.

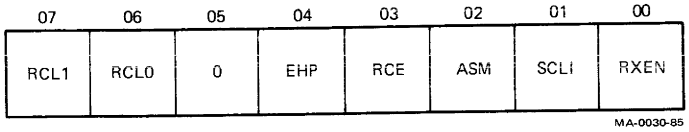
Bit 00 EIE – External Interrupt Enable. It is a write-only bit that, when set, allows interrupts when one of the following occur:

1. entering or leaving synchronous hunt phase
2. break detection or termination
3. SDLC abort detection or termination
4. idle/CRC latch becoming set (CRC being sent).

When cleared, no such interrupt will occur.



Bits 07–00 N/U – Not used. They are write-only bits. If this register is written, it must be written with all 0s.



Bits 07–06 RCL1–RCL0 – Receiver Character Length. They are write-only bits that determine the receiver character length as shown below.

RCL1	RCL0	Data Bits/Character
0	0	5
0	1	7
1	0	6
1	1	8

Bit 05 N/U – Not used. It is a write-only bit that must be written as 0.

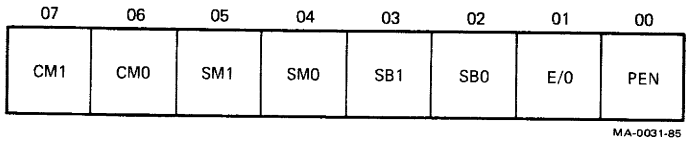
Bit 04 EHP – Enter Hunt Phase. It is a write-only bit. After initialization, the channel automatically enters the hunt mode. If synchronization is lost, the hunt phase may be reentered by writing a 1 to this bit.

Bit 03 RCE – Receiver CRC Enable. It is a write-only bit. Writing a 1 to this bit enables (or reenables) CRC calculation. CRC calculation starts with the last character placed in the receiver buffer. Writing a 0 to this bit disables, but does not reset, the receiver CRC generator.

Bit 02 ASM – Address Search Mode. It is a write-only bit. In SDLC mode, all frames will be received if this bit is 0. If this bit is a 1, frames will only be received with address bytes that match the global address (11111111) or the value loaded into WR6. This bit must be 0 in non-SDLC modes.

Bit 01 SCLH – Sync Character Load Inhibit. It is a write-only bit. Setting this bit prevents the receiver from loading sync characters into the receive buffer.

Bit 00 RXEN – Receiver Enable. It is a write-only bit. Setting this bit enables the receiver to begin. It should be set only after the receiver has been initialized.



Bits 07–06

CM1–CM0 – Clock Mode. They are write-only bits that select the clock rate multiplier for both the receiver and transmitter as follows.

CM1	CM0	Clock Rate
0	0	1 x
0	1	16 x
1	0	32 x
1	1	64 x

In synchronous modes, 1 x must be selected.

Bits 05–04

SM1–SMO – Synchronous Mode. They are write-only bits that select the synchronous protocol when synchronous operation has been chosen. These bits are ignored when asynchronous operation has been chosen.

SM1	SM0	Mode
0	0	8 bit internal sync character/monosync
0	1	16 bit internal sync character/bisync
1	0	SDLC
1	1	invalid

Bits 03–02

SB1–SB0 – Stop Bits. They are write-only bits that select the number of stop bits for asynchronous operation and also select whether the mode of operation will be asynchronous or synchronous.

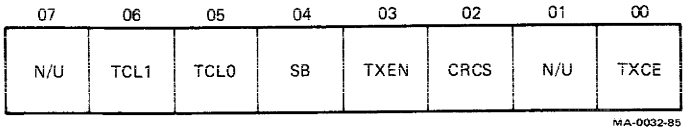
SB1	SB0	Mode
0	0	select synchronous operation
0	1	1 stop bit – asynchronous operation
1	0	1.5 stop bits – asynchronous operation
1	1	2 stop bits – asynchronous operation

Bit 01

E/O – Even/Odd Parity. It is a write-only bit that selects even or odd parity for both the receiver and transmitter when parity is enabled. A 1 selects even parity and a 0 selects odd parity.

Bit 00

PEN – Parity Enable. It is a write-only bit. When cleared, parity is disabled. When set, parity is enabled for both the receiver and transmitter. If the receiver character length is programmed to 8 data bits, the parity bit is not transferred to the processor. With other character lengths, the parity bit is transferred to the processor.



Bit 07 N/U – Not used.

Bit 06–05 TCL1–TCL0 – Transmitter Character Length. They are write-only bits that determine the transmitter character length as shown below.

TCL1	TCL0	Data Bits/Character
0	0	5 or less
0	1	7
1	0	6
1	1	8

Normally each character is sent to the transmitter right-justified and the unused bits are ignored. However, when sending 5 or less bits per character, the data should be formatted as follows.

D7	D6	D5	D4	D3	D2	D1	D0	Bits/Character
0	0	0	D4	D3	D2	D1	D0	5
1	0	0	0	D3	D2	D1	D0	4
1	1	0	0	0	D2	D1	D0	3
1	1	1	0	0	0	D1	D0	2
1	1	1	1	0	0	0	D0	1

Bit 04 SB – Send Break. It is a write-only bit. Writing a 1 to this bit causes the transmit data line to immediately go to the space condition. Writing a 0 to the bit allows normal transmitter operation.

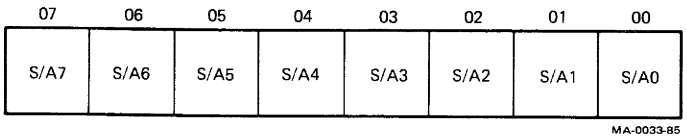
Bit 03 TXEN – Transmitter Enable. Writing a 1 to this bit enables the transmitter and should only be done after the transmitter has been initialized. Writing a 0 to this bit disables the transmitter which enters either the idle or mark state.

Bit 02 CRCS – CRC Select. It is a write-only bit that selects which CRC polynomial will be used by both the receiver and transmitter.

CRCS	Mode	Polynomial
16	15 5	
0	CRC-CCITT	X + X + X + 1
16	15 2	
1	CRC-16	X + X + X + 1

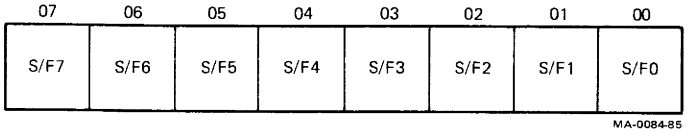
Bit 01 N/U – Not used.

Bit 00 TXCE – Transmitter CRC Enable. It is a write-only bit. Writing a 1 to this bit enables the transmitter CRC generator. Writing a 0 to this bit disables the transmitter CRC generator.



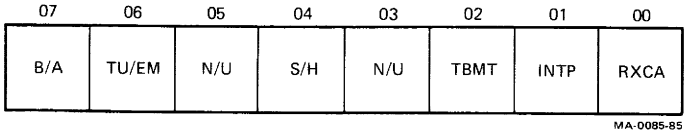
Bits 07–00

S/A7–S/A0 – Sync/Address Register. They are write-only bits. This register should be loaded with the transmit sync character in monosync mode, the low order 8 sync bits in bisync mode, or the address byte in SDLC mode.



Bits 07–00

S/F7–S/F0 – Sync/Flag Register. They are write-only bits. This register should be loaded with the receive sync character in monosync mode, the high order 8 sync bits in bisync mode, or the flag character (01111110) in SDLC mode.



Bit 07

B/A – Break/Abort. It is a read-only bit. When this bit is a 1 in asynchronous mode, it indicates the detection of a break (a null character plus a framing error which occurs when the receive input line is held in the space state for more than one character time). The B/A bit resets to a 0 when the line returns to the mark state. In SDLC mode, a 1 indicates the detection of an abort sequence (7 or more ones received in sequence). The B/A bit resets when a 0 is received. Any transition of the break/abort bit causes an external/status interrupt.

Bit 06

TU/EM – Transmitter Underrun/End of Message. It is a read-only bit that is set following a reset. The bit can only be reset by writing a Reset Transmitter Underrun/End of Message Latch command into WR0. When the transmit underrun condition occurs, this bit is set and an External/Status Interrupt is generated.

Bit 05

N/U – Not used. It is a read-only bit.

Bit 04

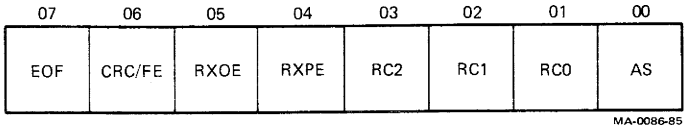
S/H – Sync/Hunt. It is a read-only bit. The meaning of this bit depends on the mode of operation. In asynchronous mode, the bit will be read as a 0. In monosync, bisync, or SDLC modes, this bit indicates whether the receiver is in the sync hunt or receive data phase of operation. A 0 indicates the receive data phase and a 1 indicates the sync hunt phase. A transition of this bit causes an external/status interrupt.

Bit 03 — N/U – Not used. It is a read-only bit.

Bit 02 — TBMT – Transmit Buffer Empty. It is a read-only bit that is set whenever the transmitter buffer is empty except during the transmission of CRC.

Bit 01 — INTP – Interrupt Pending. It is a read-only bit that is set when the vector of a pending interrupt is read from control/status register B. It is reset when an end of interrupt command is issued in WR0 and there is no other interrupt pending at the time.

Bit 00 — RXCA – Receive Character Available. It is a read-only bit that is set when the receiver buffer contains data and is reset when the buffer is empty.



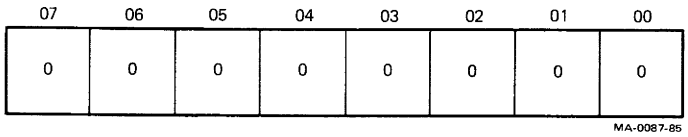
Bit 07 — EOF – End of Frame. It is a read-only bit that is valid only in SDLC mode. A 1 indicates that a valid ending flag has been received. EOF is reset by either an error reset command (in WR0) or upon reception of the first character of the next frame.

Bit 06 — CRC/FE – CRC/Framing Error. It is a read-only bit. In asynchronous mode, a 1 indicates a receiver framing error. In synchronous modes, a 1 indicates that the calculated CRC value does not match the last two bytes received. CRC/FE can be reset by issuing an error reset command in WR0.

Bit 05 — RXOE – Receiver Overrun Error. It is a read-only bit that, when set, indicates that the receiver buffer has been overloaded by the receiver. The last character in the buffer (the third character) is overwritten and flagged with this error. Once the overwritten character is read, this error is latched until reset by the error reset command in WR0.

Bit 04 — RXPE – Receiver Parity Error. It is a read-only bit. If parity is enabled, this bit is set for received characters whose parity does not match the programmed sense (odd/even). This bit is latched until it is reset by issuing a error reset command in WR0.

Bit 03–01 — RC2–RC0 – Residue Codes. They are read-only bits. Bit synchronous protocols allow I-fields that are not an integral number of characters. Since transfers from the communication port to the CPU are character oriented, the residue codes provide the capability of receiving leftover bits. Residue bits are right justified in the last two data bytes received.

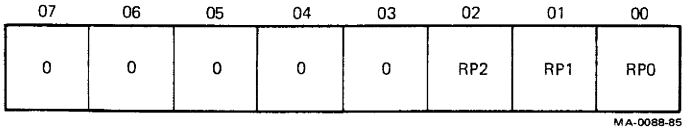


Bit 00 — AS – All Sent. It is a read-only bit. In asynchronous mode, this bit is set when the transmitter is empty and reset when a character is present in either the transmitter buffer or the transmitter shift register. In synchronous mode, this bit is always a 1.

Bits 07–00 — N/U – Not used. They are read-only bits. Always read as 0s.

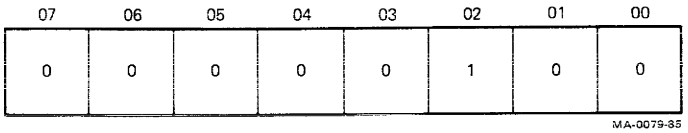
Control/Status Register B – Address 17773306

This register serves as a window to 11 internal registers as did control/status register A. The internal registers consist of eight write registers and three read registers. The write registers are labeled WR0–WR7 and the read registers are labeled RR0–RR2. An internal pointer register selects which of the WR or RR registers will be read or written during an access to control/status register B. After reset, the contents of the pointer register are 0. The first write to the control/status register causes the data to be loaded into WR0. The 3 least significant bits of WR0 serve as the pointer register. The next access to the control/status register accesses the internal register selected by the pointer register. The pointer is reset after the read or write operation is completed. In control/status register B, only WR0, WR1, WR2, and RR2 should be accessed.



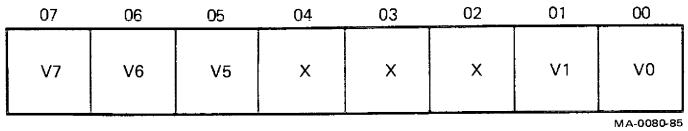
Bits 07–06 — N/U – Not used. They are write-only bits that must always be written as 0s.

Bits 02–00 — RP2–RP0 – Register Pointer bits. They are write-only bits that determine which write register the next byte is to be written into or which read register the next byte is to be read from. After reset, the first byte written goes into WR0. Following a read or a write to any register (except WR0) the pointer will point to WR0. The pointer should only be used to access WR0, WR1, WR2, and RR2.



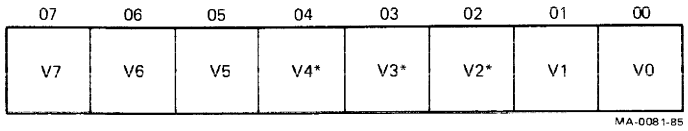
Bits 07–00

They are write-only bits. This register must be loaded with 00000100 to get proper vector information when servicing interrupts from the communication port. No other data should ever be written into this register.



Bits 07–00

V7–V0 – Vector bits. They are write-only bits. This register should be written with a base vector for the channel interrupts (receiver, special receive, transmitter, and external/status interrupts). It will be used when reading RR2 to get the vector. Bits 04–02 are "don't cares" because they will be modified to distinguish between the four channel interrupts.

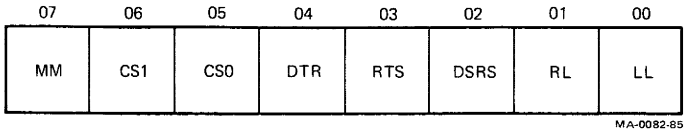


Bits 07–00

V7–V0 – Vector. They are read-only bits. This register is used to get the vector of the highest priority interrupt pending in the communication channel. The vector will be the same as the contents that were written into WR2 with bits V4–V2 modified to identify which condition caused the interrupt. After a receive/transmit interrupt causes the CPU to vector through location 210, the interrupt service routine should read RR2 to get the secondary vector that identifies the condition that caused the interrupt.

V4	**V3**	**V2**	**Condition Causing Interrupt**
1	0	0	Transmitter buffer empty
1	0	1	External/status change
1	1	0	Receiver character available
1	1	1	Special receiver condition

If RR2 is read when no interrupt is pending, the vector will be read with the variable bits, V4–V2, set to all 1s.



Bit 07

MM – Maintenance Mode. It is a read/write bit that, when set, loops the communication channel transmit data line onto the receiver data line. The transmit data signal to the modem is held in the mark state and the receive data from the modem is ignored. It is cleared at power up or by a RESET instruction.

Bits 06–05

CS1–CS0 – Clock Source. They are read/write bits that select the source of the transmit and receive baud rate clocks to the communication channel. The clock sources can be either the baud rate generator or the modem. The communication port is also capable of providing the transmit clock to the modem. The following list indicates how the selection is made.

Sources for Clocks

CS1	CS0	RXC	TXC	TXC/DTE
0	0	RBRG	TBRG	NONE
0	1	RXC/DCE	TXC/DCE	NONE
1	0	RXC/DCE	TBRG	TBRG
1	1	TBRG	TBRG	NONE

RBRG – clock is from receiver baud rate generator

TBRG – clock is from transmitter baud rate generator

RXC/DCE – clock is the receive clock line from modem

TXC/DCE – clock is the transmit clock line from modem

NONE – no clock signal is sent to modem

The RXC column gives the source of the receiver baud rate clock to the channel, the TXC column gives the source of the transmitter baud rate clock, and the TXC/DTE column indicates the clock that the communication port sends to the modem. It is cleared at power up or by a RESET instruction.

Bit 04

DTR – Data Terminal Ready. It is a read/write bit that, when set, is asserted to the modem. When cleared, the DTR signal is unasserted to the modem. It is cleared at power up or by a RESET instruction.

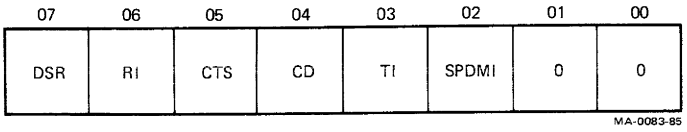
Bit 03

RTS – Request To Send. It is a read/write bit that, when set, is asserted to the modem. When cleared, the RTS signal is unasserted to the modem. It is cleared at power up or by a RESET instruction.

Bit 02 — DSRS – Data Signaling Rate Select. It is a read/write bit that, when set, is asserted to the modem. When cleared, the DSRS signal is unasserted to the modem. It is cleared at power up or by a RESET instruction.

Bit 01 — RL – Remote Loopback. It is a read/write bit that, when set, is asserted to the modem. When cleared, the RL signal is unasserted to the modem. It is cleared at power up or by a RESET instruction.

Bit 00 — LL – Local Loopback. It is a read/write bit that, when set, is asserted to the modem. When cleared, the LL signal is unasserted to the modem. It is cleared at power up or by a RESET instruction.



Bit 07 — DSR – Data Set Ready. It is a read-only bit that reflects the state of the data set ready signal from the modem. A 1 indicates that DSR is asserted and a 0 indicates that it is unasserted. A transition of this signal will generate a modem change interrupt.

Bit 06 — RI – Ring Indicator. It is a read-only bit that reflects the state of the ring indicator signal from the modem. A 1 indicates that RI is asserted and a 0 indicates that it is unasserted. A transition of this signal will generate a modem change interrupt.

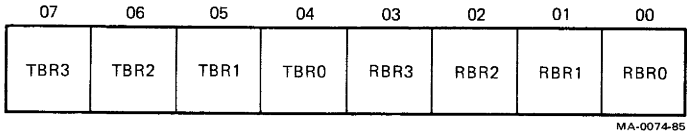
Bit 05 — CTS – Clear To Send. It is a read-only bit that reflects the state of the clear to send signal from the modem. A 1 indicates that CTS is asserted and a 0 indicates that it is unasserted. A transition of this signal will generate a modem change interrupt.

Bit 04 — CD – Carrier Detect. It is a read-only bit that reflects the state of the carrier detect signal from the modem. A 1 indicates that CD is asserted and a 0 indicates that it is unasserted. A transition of this signal will generate a modem change interrupt.

Bit 03 — TI – Test Indicator. It is a read-only bit that reflects the state of the test indicator signal from the modem. A 1 indicates that TI is asserted and a 0 indicates that it is unasserted.

Bit 02 — SPDMI – Speed Mode Indicator. It is a read-only bit that reflects the state of the speed mode indicator signal from the modem. A 1 indicates that SPDMI is asserted and a 0 indicates that it is unasserted.

Bits 01–00 — N/U – Not used. They are read-only bits that are always read as 0s.



Bits 07–04

TBR3–TBR0 – Transmitter Baud Rate select. These bits are used to program the transmitter baud rate generator.

TBR3	TBR2	TBR1	TBR0	Async 16 X Clock Baud Rate	Sync 1 X Clock Baud Rate
0	0	0	0	50	
0	0	0	1	75	1200
0	0	1	0	110	
0	0	1	1	134.5	
0	1	0	0	150	2400
0	1	0	1	300	4800
0	1	1	0	600	9600
0	1	1	1	1200	19200
1	0	0	0	1800	
1	0	0	1	2000	
1	0	1	0	2400	
1	0	1	1	3600	
1	1	0	0	4800	
1	1	0	1	7200	
1	1	1	0	9600	
1	1	1	1	19200	

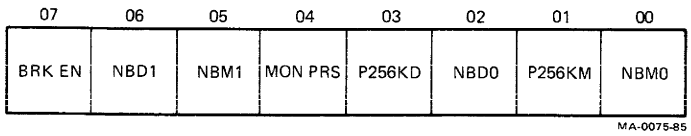
Bits 03–00

RBR3–RBR0 – Receiver Baud Rate select. These bits are used to program the receiver baud rate generator.

RBR3	RBR2	RBR1	RBR0	Async 16 X Clock Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19200

6.4.8 System Control and Status Register (SCSR)

This register uses only the low byte. The high byte is always read as all 0s and writes to the high byte have no effect. The system control and status register provides certain configuration information and allows the selection of certain modes of operation. The following shows the address location of the system control and status register.



Address
17773700

Bit 07 — BRK EN – Break Enable. It is a read/write bit that is used to enable hardware break detect on the printer port when that port is being used with a terminal. Mode register 1 need NOT be initialized before this bit is set (unlike the Professional 350). When BRK EN is set, hardware break detection is enabled. When cleared, break detection is disabled. If a printer is connected to the port, break detection is disabled regardless of the state of the BRK EN bit. BRK EN is cleared at power-up.

Bit 06 — NBD1. – number of banks on daughter board (bit 1)

Bit 05 — NBM1. – number of banks on mother board (bit 1)

Bit 04 — MON PRS – Monitor Present. It is a read-only status bit that indicates that a video monitor is connected to the video interface. MON PRS set indicates a monitor is present and cleared indicates no monitor present.

Bit 03 — P256K 0=64K parts, 1=256K parts

Bit 02 — NBD0. – number of banks on daughter board (bit 0)

Bit 01 — P256KM 0=64K parts, 1=256K parts

Bit 00 — NBM0. – number of banks on mother board (bit 0)

The register memory configuration is determined as shown in the list below.

NBx1	NBx0	P256Kx	Memory Size
0	0	X	No module present at group "x" (x=0 system module, x=1 daughter)
0	1	0	128 kilobytes in one bank of 64K parts
1	0	0	256 kilobytes in two banks of 64K parts
1	1	0	512 kilobytes in four banks of 64K parts
0	1	1	512 kilobytes in one bank of 256K parts
1	0	1	1 megabyte in two banks of 256K parts
1	1	1	2 megabyte in four banks of 256K parts

NOTE 1
X=M for system and X=D for daughter module.

NOTE 2
There is no commitment by DIGITAL to produce memory options of all of the above sizes.

6.4.9 LED/Mode Register

The following two sections provide information on the LED display and mode registers.

6.4.9.1 LED Display Register – The LED display register uses only the low byte. Any attempted read of this register will read the MODE register.

The power-up self-test firmware uses the LED display to indicate any errors that were detected. At the completion of the self-test, the LED display will contain the code for the first error detected. If no errors were found, the LED display will be cleared.

The following shows the address location of the LED display register.

Address
17773704 (write only)

Bits 07–04	These bits are not used and are always read as 0s.
Bits 03–00	LED3–LED0. They are write-only bits that control the state of the four red LEDs on the rear of the unit. Setting one of these bits will cause the corresponding LED to be turned off. Clearing a bit will cause the corresponding LED to be lit. All 4 bits are cleared (lit) at power up. The bits are always read as 0s.

6.4.9.2 Mode Register – This register is internal to the I/O gate array. It is accessed by reading 17773704, low byte only. A read of the high byte will result in all 0s. A write will result in a write to the LED display register.

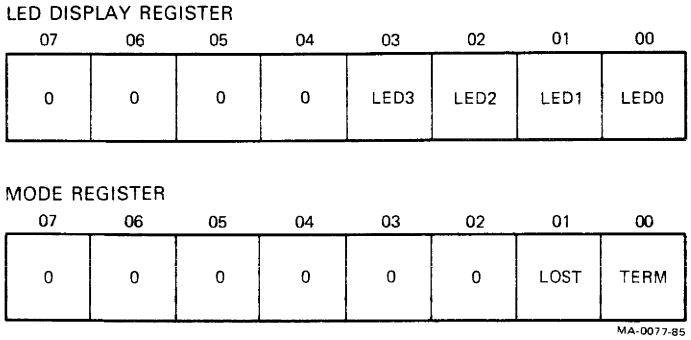
The following shows the address location of the LED display register.

Address
17773704 (read only)

Bits 07–02 Not used. They are always read as 0s.

Bit 01 LOST – Loop On Self-Test. This bit reflects the state of the LOST L signal. When high, it indicates that LOST L is asserted low. When low, it indicates that LOST L is unasserted or high.

Bit 00 TERM – Terminal. This bit reflects the state of the TERM L signal. When high, it indicates that TERM L is asserted low. When low, it indicates that TERM L is unasserted or high.



LOST	TERM	Description
0	0	Customer mode
0	1	Console mode
1	0	Service mode
1	1	Manufacturing mode

6.4.10 Real-Time System Clock

The 14 system clock registers use only the low byte. The high bytes are always read as all 0s and writes to high bytes have no effect.

The firmware initializes the clock after the power-up self-test is completed. This default state is as below.

CSR 0	bits <06:0>=0 1 0 (divider control) bits <03:00>=0 0 0 0 (no periodic rate)
CSR 1	bit 07 (the set bit) is cleared if the battery power got too low and is not effected otherwise bits <06:04>=0 0 0 (interrupt enables cleared) bits <03:00> are not effected
CSR 2	read-only register not initialized by firmware
CSR 3	bit 07=1 (VRT bit always set)

The following list shows the address location of the real-time system clock registers.

Addresses	
17773000	Seconds
17773002	Seconds alarm
17773004	Minutes
17773006	Minutes alarm
17773010	Hours
17773012	Hours alarm
17773014	Day of week
17773016	Date of month
17773020	Month
17773022	Year
17773024	CSR0
17773026	CSR1
17773030	CSR2
17773032	CSR3

Vector
230

6.4.10.1 Time, Date, Alarm Registers – The first 10 registers (17773000–17773022) handle the time, date, and alarm functions. The contents of these 10 registers can be programmed to be in either binary or BCD format. All of the registers must be the same format. Bit 02 in CSR1 determines the data format. The hours and hours alarm registers can be programmed to be in either 12- or 24-hour format. Both registers must be the same format. When the 12-hour format is selected, bit 07 of the two registers indicates AM (when cleared) or PM (when set).

The day of week register counts cyclicly from 1 to 7 where 1 represents Sunday. The year register counts cyclicly from 00 to 99.

The three alarm registers are used to generate an interrupt to the processor at the specified time if the alarm interrupt enable bit is set in CSR1. Each of the alarm registers can be programmed to a "don't care" state by setting bits 06 and 07. This allows alarm interrupts to occur every hour, every minute, or every second if desired. All 10 time, date, and alarm registers can be read or written but must be done following the appropriate procedures described below.

Once each second, a time and date update cycle is begun. The time and date are incremented by one second and the time is compared to the alarm registers. During the update cycle, the 10 time, date, and alarm registers are not accessible. Undefined data will be obtained if any of these registers are read during an update cycle.

Two methods of assuring proper data are provided.

1. Bit 07 in CSR0 is the update-in-progress bit (UIP). The UIP bit will pulse once per second. After the UIP bit goes high, the update cycle begins 244 microseconds later. Therefore, if the UIP bit is read as a low, the program has at least 244 microseconds to read the time and date before the update cycle begins and makes the information inaccessible. If the UIP bit is read as a high, the time and date may not be available.

2. An update ended interrupt is provided to indicate that the update cycle has completed. This interrupt will occur at the end of the update cycle if the update interrupt enable bit is set in CSR1. This method gives the program almost a full second to read the time and date before the next update cycle. The interrupt service routine must clear the update ended flag bit in CSR2 for proper operation.

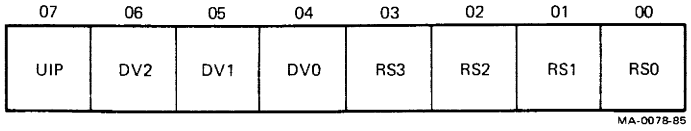
Setting the time and date or programming the alarm must not be done during an update cycle. The following procedures should be used.

1. Setting the time and date is accomplished by using the SET bit in CSR1. Setting the SET bit will inhibit the update cycles. (If an update is in progress when the program sets the SET bit, the update will complete.) With updates halted, the program should select the desired formats in CSR1, initialize the time and date registers with the appropriate information, and initialize the alarm registers, if used. The SET bit can then be cleared to enable update cycles to occur normally.

2. The alarm registers can be initialized when the time and date are set or when it is known that an update cycle is not in progress using one of the two previously described methods.

Address	Function	Decimal Range	Binary Mode	BCD Node in Hexadecimal
17773000	Seconds	00–59	000–073	00–59
17773002	Seconds alarm	00–59	000–073	00–59
17773004	Minutes	00–59	000–073	00–59
17773006	Minutes alarm	00–59	000–073	00–59
17773010	Hours: 12 hour AM mode	01–12	001–014	01–12
	Hours: 24 hour PM mode	01–12	201–214	81–92
	Hours: 24-hour mode	00–23	000–027	00–23
17773012	Hours alarm: 12-hour AM mode	01–12	001–014	01–12
	Hours alarm: 12-hour PM mode	01–12	201–214	81–92
	Hours Alarm: 24-hour mode	00–23	000–027	00–23
17773014	Day of week	01–07	001–007	01–07
17773016	Date of month	01–31	001–037	01–31
17773020	Month	01–12	001–014	01–12
17773022	Year	00–99	000–143	00–99

6.4.10.2 Control/Status Registers – The following describes the control/status registers for the real-time system clock.



Bit 07 — UIP – Update in Progress. It is a read-only bit. The UIP bit is a status flag that may be monitored by the program. It is set 244 microseconds before an update cycle begins and is cleared immediately after the update cycle is complete. UIP is not effected by a RESET.

Bits 06–04 — DV2–DV0 – Divider Control. They are read/write bits that should be initialized accordingly.

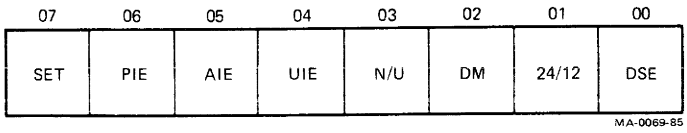
DV2	DV1	DV0
0	1	0

Any other state of these three bits will result in incorrect clock operation. These bits are not effected by RESET.

Bits 03–00

RS3–RS0 – Rate Select. They are read/write bits that select one of 13 periodic rates that may be used to generate an interrupt. These bits are not effected by RESET. The periodic rates are selected as follows.

RS3	RS2	RS1	RS0	Periodic Rate	Frequency
0	0	0	0	none	none
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 μs	8192 Hz
0	1	0	0	244.141 μs	4096 Hz
0	1	0	1	488.281 μs	2048 Hz
0	1	1	0	976.562 μs	1024 Hz
0	1	1	1	1.95313 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125.0 ms	8 Hz
1	1	1	0	250.0 ms	4 Hz
1	1	1	1	500.0 ms	2 Hz



Bit 07

SET – Set. It is a read/write bit that is used to halt update cycles so that the time and date registers can be initialized. When set, update cycles are inhibited. If the bit is set during an update, the update cycle will complete. When cleared, normal update cycles occur. SET is not effected by RESET.

Bit 06

PIE – Periodic Interrupt Enable. It is a read/write bit that, when set, enables periodic interrupts at the rate selected by bits RS3–RS0 in CSR0. When cleared, no periodic interrupts will occur. PIE is cleared by RESET.

Bit 05

AIE – Alarm Interrupt Enable. It is a read/write bit that, when set, enables alarm interrupts to occur at the time specified in the alarm registers. When cleared, no alarm interrupts will occur. AIE is cleared by RESET.

Bit 04

UIE – Update ended Interrupt Enable. It is a read/write bit that, when set, enables an interrupt to occur at the end of each update cycle. When cleared, no update interrupts will occur. UIE is cleared by RESET.

Bit 03

Not used. It is a read/write bit that is cleared by RESET.

Bit 02

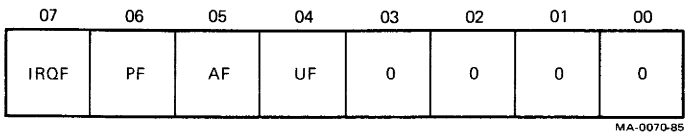
DM – Data Mode. It is a read/write bit that, when set, indicates that the time, date, and alarm registers will be in binary format. When cleared, BCD format is selected. DM is not effected by RESET. DM should only be changed when initializing all the time and date registers.

Bit 01

24/12 – 24-Hour Mode and 12-Hour Mode. It is a read/write bit that, when set, selects 24 hour clock format. When cleared, it selects 12 hour clock format and AM or PM is indicated by bit 07 in the hours register. 24/12 is not effected by RESET. 24/12 should only be changed when initializing all the time and date registers.

Bit 00

DSE – Daylight Savings Enable. It is a read/write bit. When set, two special updates are enabled. On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time reaches 1:59:59 AM for the first time, it changes to 1:00:00 AM. When DSE is cleared, these special updates do not occur. DSE is not effected by RESET. DSE should not be changed during an update cycle.



Bit 07

IRQF – Interrupt Request Flag. It is a read-only bit that, when set, indicates that the clock is generating an interrupt to the processor. IRQF is set when one or more of the following conditions occur.

1. PIE and PF bits are both set.
2. AIE and AF bits are both set.
3. UIE and UF bits are both set.

Bit 06

PF – Periodic Interrupt Flag. It is a read-once bit that is set at the end of each period time. The period time is determined by the periodic rate bits RS3–RS0. PF gets set independent of the state of the PIE bit. Setting PF will generate a clock interrupt to the processor and cause a 1 to appear in the IRQF bit if the PIE bit is also set. PF gets cleared by RESET or by reading CSR2.

Bit 05

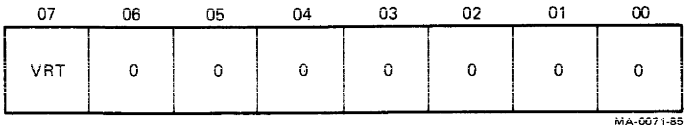
AF – Alarm Interrupt Flag. It is a read-once bit that gets set when the time matches the alarm time. AF gets set independent of the state of the AIE bit. Setting AF will generate a clock interrupt to the processor and cause a 1 to appear in the IRQF bit if the AIE bit is also set. AF gets cleared by RESET or by reading CSR2.

Bit 04

UF – Update-Ended Interrupt Flag. It is a read-once bit that gets set after each update cycle has completed. UF operates independent of the state of the UIE bit. UF being set will generate an interrupt to the processor and cause a 1 to appear in the IRQF bit if UIE is also set. UF gets cleared by RESET or by reading CSR2.

Bits 03–00

Not used. They are read-only bits that are always read as 0s.



Bit 07 — VRT – Valid RAM and Time. It is a read-once bit that, when set, indicates that the clock has not lost power and that the time and date have been updated properly since last initialized. If cleared, it indicates that the power to the clock was too low and the time and date may not be valid. The processor should set the VRT bit when it initializes the clock. Reading CSR3 will set the VRT bit. VRT is not effected by RESET. (This bit indicates the validity of the battery backed-up RAM as well.)

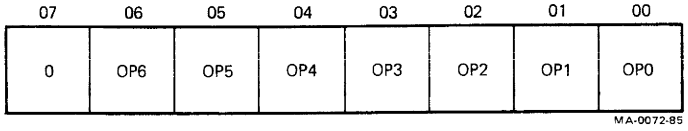
Bits 06–00 — Not used. They are read-only bits that are always read as 0s.

6.4.11 Option Module Present Register (OPRES)

The option module present register is used to indicate which of the six option module slots contains a module. It is a read-only register which uses only the low byte. The high byte is read as all 0s and all writes to the register have no effect.

The following is address location for the option module present register.

Address
17773700 Data Buffer



Bit 07 — Not used. It is a read-only bit that is always read as 0.

Bit 06 — OP6 – PC380 video present. It is a read-only bit that is always asserted (=1).

Bits 05–00 — OP5–OP0 – Option Present. They are read-only bits. A 1 in an OP bit indicates that a module is present in the corresponding option module slot. For example, if OP1 is set, a module is present in option module slot 1. A 0 in an OP bit indicates no module present in the corresponding slot.

The following list shows each option module address location with their associated interrupt request address vectors.

Slot	Address Location	A Vector	B Vector
0	17774000–17774177	300	304
1	17774200–17774377	310	314
2	17774400–17774577	320	324
3	17774600–17774777	330	334
4	17775000–17775177	340	344
5	17775200–17775377	350	354
6*	17775400–17775577	360	364

* This is a logical slot (not physically in the card cage). Slot 6 is dedicated to the video logic subsystem.

6.4.12 ID PROM

The system module contains a 32-byte ID PROM. Each board has a unique pattern in the PROM. The following is the address location of the ID PROM.

Address
17773600–17773676 32 Bytes PROM

All 32 word locations use only the low byte. The high bytes are always read as all 0s. Any attempt to write to the ID PROM locations will result in a nonexistent memory trap to location 4.

The ID code is a 12-BCD digit (6 byte) random number. The ID PROM should be blasted with the ID as shown in Table 6-10. This is included for use in software protection schemes.

Table 6-10 ID PROM Programming Table

Octal PROM Address	PROM Contents	22-bit System Address	
00	Random ID byte 1	17773600	
01	Random ID byte 2	17773602	
02	Random ID byte 3	17773604	
03	Random ID byte 4	17773606	
04	Random ID byte 5	17773610	
05	Random ID byte 6	17773612	
06	Error check byte 1	17773614	
07	Error check byte 2	17773616	
10	Random ID byte 1	17773620	
11	Random ID byte 2	17773622	
12	Random ID byte 3	17773624	
13	Random ID byte 4	17773626	
14	Random ID byte 5	17773630	**Error check bytes 1/2**
15	Random ID byte 6	17773632	**form a word check on**
16	Error check byte 1	17773634	**the 6-byte ID.**
17	Error check byte 2	17773636	
20	Random ID byte 1	17773640	
21	Random ID byte 2	17773642	
22	Random ID byte 3	17773644	
23	Random ID byte 4	17773646	
24	Random ID byte 5	17773650	
25	Random ID byte 6	17773652	
26	Error check byte 1	17773654	
27	Error check byte 2	17773656	
30	00000000	17773660	
31	11111111	17773662	
32	01010101	17773664	
33	10101010	17773666	
34	11111111	17773670	
35	00000000	17773672	**Error check bytes 3/4**
36	Error check byte 3	17773674	**form a word check on**
37	Error check byte 4	17773676	**the entire PROM.**

6.4.13 Maintenance Terminal

The maintenance terminal is included as a debug and test feature. It is physically the same port as the printer port. The printer port can be made to simulate a standard PDP11 DL interface. When a terminal is connected to the port instead of a printer, accesses to the maintenance terminal addresses 17777560–17777566 will function like the standard DL interface. In this mode, the port programs like a DL serial device with a receiver CSR, a receiver data buffer, a transmitter CSR, and a transmitter data buffer. Accesses to these registers when a terminal is not connected to the port will result in reads of all 0s and writes that have no effect. Accesses to the printer port registers, 17773400–17773406, will operate normally regardless of the device connected to the port.

Interrupts are not handled like a standard terminal DL. There are no interrupt enable bits in the CSR registers at locations 17777560 and 17777564. Interrupts must be enabled/disabled and handled through interrupt controller 0 like the printer port interrupts. The vectors can be changed from the printer port vectors of 220 and 224 to the terminal vectors of 60 and 64 by reprogramming the response memory in interrupt controller 0.

Hardware break detection can be enabled when a terminal is connected to the port. This allows the processor to halt into micro-ODT when the break key is depressed on the terminal. The hardware break detection will have no effect if a printer is connected to the port. The following is the address location of the maintenance terminal registers.

Addresses	
17777560	Receiver CSR
17777562	Receiver Data Buffer
17777564	Transmitter CSR
17777566	Transmitter Data Buffer

Vectors	
220*	Receiver
224*	Transmitter

NOTE

Refer to Section 6.4.3 DC362 I/O interface gate array registers for descriptions of the maintenance terminal registers.

6.4.14 Maintenance ODT

A portion of the microcode in the processor emulates the capability found on a "lights and switches" console. This feature is called microcode on-line debugging technique or micro-ODT. Micro-ODT accepts 22-bit addresses, allowing it to access 4088 kilobytes of memory plus the 8-kilobyte I/O page. The terminal at the standard bus address of 17777560 is used to perform console functions.

* Vectors of 60 and 64 can be obtained by proper programming of interrupt controller 0. Interrupts on this port are not handled like a standard PDP11 DL.

6.4.14.1 Overview – Communication between the processor and the user is via a stream of ASCII characters which are interpreted by the processor as console commands. The terminal addresses, 17777560 through 17777566 are generated in microcode and cannot be changed.

Terminal Interface
The hardware interface for a terminal (serial line) to communicate with ODT is the printer port. A terminal cable must be used in place of the printer cable at the printer connector. If the terminal cable is not used, read accesses of the terminal CSRs (addresses 17777560 and 17777564) will result in all 0s indicating that the transmitter and the receiver are not ready. The I/O gate array determines that the maintenance terminal is present when pin 9 of the printer port is GND (TERM L active).

Entry Conditions
The ODT console mode can be entered in the following two ways.

1. By execution of a HALT instruction in kernel mode, because ODT will wait until a terminal is connected if none is present.

2. From the maintenance terminal by depressing the BREAK key on the keyboard because the BREAK ENABLE bit in the system CSR must be set and the terminal cable must be used or the BREAK will be ignored. The BREAK ENABLE bit is in the CSR in the J11 control gate array. In order to generate the HALT for the J11 CPU, it is necessary for three conditions to be true:

    a. break enable bit set,
    b. terminal cable present, and
    c. break key depressed.

Upon entry, ODT causes the following initialization.

1. Print a <CR> and <LF>.

2. Print the contents of the PC (program counter) in 6 (16-bit octal).

3. Perform a read from RBUF (input data buffer at 17777562) and then ignore the character present in the buffer. This operation is done so that erroneous characters or user program characters are not interpreted by ODT as a command.

4. Print a <CR> and <LF>.

5. Print the prompt character, "@".

6. Enter a wait loop for terminal input. The Done flag (bit 7) in RCSR at 17777560 is constantly being tested via a read by the processor for a "1." If it is a "0," the processor keeps testing.

ODT Operation of Serial Line Interface
The processor's microcode operates the serial interface in half duplex mode by using program I/O techniques rather than interrupts. This means that when the ODT microcode is busy printing characters using the output side of the interface, the microcode is not monitoring the input side for incoming characters. In this case, all incoming characters will be lost. Even though the UART chip may post overrun errors, the microcode does not check any error bits in the serial interface.

Users should not try to "type ahead" to ODT because those characters will not be recognized. If another processor is at the end of the serial line, it must obey half duplex operation, in other words, no input characters should be sent until ODT's output has finished.

The input sequence for ODT is listed below (upon entry to ODT, the RBUF register will be read and the character ignored to eliminate a possible erroneous command).

1. Read RCSR bit 7 (Done Flag) and if a 0, continue testing.

2. If RCSR bit 7 is a 1, read low byte of RBUF.

The output sequence of ODT is as follows.

1. Read XCSR bit 7 (Done Flag) and if a 0, continue testing.

2. If XCSR bit 7 is a 1, write the character into the low byte of XBUF.

6.4.14.2 Command Set – The ODT command set is described in this section and when examples are used, the user's entry is not underlined while the processor's response is. The commands are a subset of ODT-11 and use the same command characters. ODT has 10 internal states and each state recognizes certain characters as valid input and responds with a "?" to all others. These states are described in Table 6-11 at the end of the section.

The parity bit (bit 7) on all input characters is ignored (i.e. - not stripped) by ODT and if the input character is echoed, the state of the parity bit is copied to the output buffer (XBUF). Output characters internally generated by ODT (e.g., <CR>) have the parity bit equal to 0. All commands are echoed except for <LF>.

In order to describe the use of a command, other commands will be mentioned before they have been defined. For the novice user, this section should be scanned first for familiarization and then read again for detail. The word "location," as used in this section, refers to a bus address, processor register, or processor status word (PSW).

/ (ASCII 057) SLASH
This command is used to open a bus address, processor register, or processor status word and is normally preceded by other characters which specify a location. In response to /, ODT will print the contents of the location (i.e., six characters) and then a space (ASCII 40). After printing is complete, ODT will wait for either new data for that location or a valid close command. The space character is issued so that the location's contents and possible new contents entered by the user are legible on the terminal.

Example: @001000/012525 <SPACE>

where:	@	=	ODT prompt character
001000		=	octal location in the address space desired by the user (leading 0s are not required)
	/	=	command to open and print contents of location
012525		=	contents of octal location 1000
<SPACE>		=	space character generated by ODT

The / command can be used without a location specifier to verify the data just entered into a previously opened location. The / produces this result only if it is entered immediately after a prompt character. A / issued immediately after the processor enters ODT mode will cause a ? <CR>, <LF>, to be printed because a location has not yet been opened.

Example: @1000/012525 <SPACE> 1234 <CR> <CR> <LF>
@/001234 <SPACE>

where:

first line = new data of 1234 entered into location 1000 and location closed with <CR>

second line = a / was entered without a location specifier and the previous location was opened to reveal that the new contents were correctly entered

<CR> (ASCII 15) CARRIAGE RETURN

This command is used to close an open location. If a location's contents are to be changed, the user should precede the <CR> with the new data. If no change is desired, <CR> will close the location without altering its contents.

Example: @R1/004321 <SPACE> <CR> <CR> <LF>
@

Processor register R1 was opened and no change was desired so the user issued <CR>. In response to the <CR>, ODT printed <CR> <LF> and @.

Example: @R1/004321 <SPACE> 1234 <CR> <CR> <LF>
@

In this case, the user desired to change R1 and the new data, 1234, was entered before issuing the <CR>. ODT deposited the new data in the open location and then printed <CR>, <LF>, and @.

ODT does not directly echo the <CR> entered by the user, but instead prints <CR>, <LF>, and @.

<LF> (ASCII 12) LINE FEED

This command is used to close an open location and then will open the next contiguous location. Bus addresses and processor registers will be incremented by two and one, respectively. If the PSW is open when a <LF> is issued, it will be closed and a <CR>, <LF>, and @ will be printed; no new location will be opened. If the open location's contents are to be changed, the new data should precede the <LF>. If no data is entered, the location is closed without being altered.

Example: @R2/123456 <SPACE> <LF> <CR> <LF>
@R3/054321 <SPACE>

In this case, the user entered <LF> with no data preceding it. In response, ODT closed R2 and then opened R3. When a user has the last register, R7, open, and issues <LF>, ODT will "roll over" to the beginning register, R0.

Example: @R7/000000 <SPACE> <LF> <CR> <LF>
@ R0/123456 <SPACE>

Unlike other commands, ODT will not echo the <LF>. Instead it will print <CR>, then <LF> so that teletype printers operate properly. In order to make this easier to decode, ODT will also not echo ASCII 0, 2 or 10, but will respond to these 3 characters with ? <CR>, <LF>, and @.

$(ASCII 044) OR R (ASCII 122) INTERNAL REGISTER DESIGNATOR
Either character when followed by a register number, 0 to 7, or PSW designator, S, will open that specific processor register.

The $ character is recognized to be compatible with ODT-11 and the R character was also introduced for the convenience of one key stroke and being representative of what it does.

Example: @$0/000123 <SPACE>

Example: @R7/000123 <SPACE>

If more than one character (digit or S) after the "R" or "$" is typed, ODT will use the last character as the register designator. An exception: If the last 3 digits equal 077 or 477, ODT will open the PSW rather than R7.

S (ASCII 123) PROCESSOR STATUS WORD
This designator is for opening the PSW (processor status word) and must be used after the user has entered an "R" or "$" register designator.

Example: @RS/100377 <SPACE> 0 <CR> <CR> <LF>
@/000010 <SPACE>

Note that the trace bit (bit 4) of the PSW cannot be modified by the user. The reason is so that PDP-11 program debug utilities (e.g., ODT-11) which use the T bit for single stepping will not be accidentally harmed by the user. If the user issues a <LF> while the PSW is open, the PSW will be closed and ODT will print a <CR>, <LF>, and @. No new location is opened in this case.

G (ASCII 107) GO
This command is used to start program execution at a location entered immediately before the "G." This function is equivalent to the "LOAD ADDRESS" and "START" switch sequence on other PDP-11 consoles.

Example: @200G <NULL> <NULL>

The ODT sequence for a "G" is listed below.

1. Print two nulls (ASCII 0) so the bus initialize that follows will not flush the "G" character from the double buffered UART chip in the serial line interface.

2. Load R7 (PC) with the entered data. If no data is entered, 0 is used. (In the above example, R7 will equal 200 and that is where program execution will begin).

3. The PSW, FPS (floating point status) registers, SR0<15:13,0>, SR3, PIRQ, and the CPU error register will be cleared to 0.

P (ASCII 120) PROCEED
This command is used to resume execution of a program and corresponds to the "CONTINUE" switch on other PDP-11 consoles. No programmer visible machine state is altered using this command.

Example: @P

Program execution resumes at the place pointed to by R7. After the "P" is echoed, the ODT state is left and the processor immediately enters the state to fetch the next microinstruction.

After the instruction is executed, outstanding interrupts, if any, are serviced. If a HALT request is asserted it will be recognized at the end (during the service state) of the instruction and the processor will enter the ODT state. Upon entry, the contents of the PC (R7) will be printed. In this fashion, a user can single instruction step through a program and get a PC "trace" displayed on his terminal.

SINGLE STEP
ODT on the J11 does not have an "H" command. Single stepping may be accomplished by writing a 1 to bit 4 of the SSODT register at address 17773706. This action asserts HALT_L low so that after typing "P," ODT will be reentered after executing one macroinstruction. Exit from single stepping mode by writing a 0 to bit 4 of SSODT. Note that this bit may be altered from ODT itself or by a macroinstruction. Note that bit 4 is the only bit in this register which a write operation affects.

<CONTROL-SHIFT-S> (ASCII 23) BINARY DUMP
This command is used for manufacturing test purposes and is not a normal user command. It is intended to display a portion of memory more efficiently than using the "/" and <LF> commands. The protocol is as follows.

1. After a prompt character, ODT receives a control-shift S command and echoes it.

2. The host system at the other end of the serial line must send two 8-bit bytes which ODT interprets as a starting address. These two bytes are not echoed. The first byte specifies starting address bits <15:8> and the second byte specifies starting address bits <7:0>. Bus address bits <21:16> are always forced to be 0; the dump command is restricted to the first 64 kilobytes of address space.

3. After the second address byte has been received, ODT will output to the serial line 12 octal bytes starting at the address specified previously. When the output is finished, ODT will print <CR>, <LF>, and @. If a user accidentally enters this command, it is recommended, in order to exit from the command, that two "@" characters (ASCII 100) be entered as a starting address. After the binary dump, the user will get a prompt character "@."

6.4.14.3 Addressing Scheme – Micro-ODT accepts 22-bit addresses, allowing it to access 4088 kilobytes of memory plus the 8 kilobyte I/O page. All addresses, including I/O, must be entered with all 22 bits specified. For example, if the user wanted to address slot 0, the user must enter 17774000, not 174000. Addresses 17760000 through 17777776 will correspond to the I/O page.

J11 Register Access
Accessing the general register sets is accomplished in the following way. Whenever R0–R5 are referenced in ODT, they access the general register specified by the PS register set bit (PS<11>). If a program operating in general register set 0 (PS<11)=0) is halted and a general register is opened, register set 0 is accessed. Similarly, if a program is operating in register set 1, "R0–R5" accesses register set 1.

If a specific register set is desired, PS<11> must be set by the user to the appropriate value, and then the "R0" to "R5" commands can be used. If an operating program has been halted, the original value of PS<11> must be restored in order to continue execution.

Example:

```
PS=00000
@R4/052525<SPACE> <CR> <CR><LF>
```

R4 in register set 0 has been opened.

```
@RS/000000<SPACE> 4000 <CR> <CR><LF>
@R4/177777<SPACE> <CR> <CR><LF>
@RS/004000<SPACE> 0 <CR> <CR><LF>
@P-
```

In this case, R4 in register set 1 was desired. The PS was opened, and PS<11> was set to 1 (register set 1). Then R4 was examined and closed. The original value of PS<11> was restored, and then the program was continued, using the P command.

Processor registers R0–R7 will not respond (i.e., time out will occur) to bus addresses 17777700–17777707 if referenced in ODT.

The MMU contains status registers and PAR/PDR pairs. These registers can be accessed from ODT by entering their bus address.

Example:

```
@17777572/000001 <SPACE>
```

In this case, memory management status register 0 was opened and the memory management enable bit is set.

The FP11 accumulators cannot be accessed from ODT. Only P11 instructions can access these registers.

Stack Pointer Selection

Accessing kernel, supervisor, and user stack pointer registers are accomplished in the following way. Whenever R6 is referenced in ODT, it accesses the stack pointer specified by the PS current mode bits (PS<15:14>). This is done for convenience. If a program operating in kernel mode (PS<15:14>=00) is halted, and R6 is opened, the kernel stack pointer is accessed.

Similarly, if a program is operating in user or supervisor mode, R6 accesses the user or supervisor stack pointer.If a different stack pointer is desired, PS<15:14> must be changed by the user to the appropriate value and then the R6 command can be used. If an operating program has been halted, the original value of PS<15:14> must be restored in order to continue execution.

Example:

```
PS=140000
@R6/123456 <SPACE>
```

The user mode stack pointer has been opened.

```
@RS/140000 <SPACE> 0 <CR> <CR> <LF>
@R6/001000 <SPACE> <CR> <CR> <LF>
@RS/000000 <SPACE> 140000 <CR> <CR> <LF>
@P
```

In this case, the kernel mode stack pointer was desired. The PS was opened and PS<15:14> was set to 00 (kernel mode). Then R6 was examined and closed. The original value of PS<15:14> was restored and then the program was continued using the P command.

Entering of Octal Digits
In general, when the user is specifying an address ODT will use the last eight octal digits if more than eight have been entered. When the user is specifying data, ODT will use the last six octal digits if more than six have been entered. The user need not enter leading 0s for either address or data; ODT forces 0s as the default. If an odd address is entered, ODT responds to the error by printing ?<CR><LF>@.

ODT Timeout
If the user specifies a nonexistent address, ODT will respond to the bus timeout by printing ?, <CR>, <LF>, @. The bus timeout is approximately 6.5 microseconds.

Invalid Characters
In general, any character which ODT does not recognize during a particular sequence will be echoed (with the exception of ASCII codes 0, 2, 10, or 12 as noted earlier) and ODT will print a ?, <CR>, <LF>, @. ODT has 10 internal states and each state has its own set of valid input characters. Some commands are only allowed when in certain states or sequences; thus an attempt has been made to lower the probability of a user unconsciously destroying himself by pressing the wrong key.

Table 6-11 defines the ODT states and valid input characters.

6.4.14.4 Professional 380 Debug Addressing – The following list provides a set of commonly used addresses when debugging the Professional 380.

Virtual address	15–13	APF	–	Active page field selects PAR
	12–06	BN	–	Block number
	05–00	DIB	–	Displacement in block
Physical address	21–06	obtained from adding BN to the PAR value		
	05–00	obtained from DIB bits		

17772300 – 17772316 kernel I space PDRs
17772320 – 17772336 kernel D space PDRs
17772340 – 17772356 kernel I space PARs
17772360 – 17772376 kernel D space PARs

17773200 – 17773212 Interrupt controller registers

Commands for all interrupt CSRs are as follows.
000 – RESET, IMR=1, IRR=0
05b – Clear, IMR bit b

17777572	MMR0	Memory management register #0
R/W	00	Enable relocation if set to 1

17777600 – 17777616 user I space PDRs
17777620 – 17777636 user D space PDRs
17777640 – 17777656 user I space PARs
17777660 – 17777676 user D space PARs

Table 6-11 ODT States

State	Example of Term Output	Valid Input	Comment
1	@	0–7 R,$ G P CTL-SHIFT-S	Octal digits
2	@R OR @$	0–7 S	
3	@1000/123456	0–7 CR LF	
4	@R1/123456	0–7 CR LF	
5	@1000	0–7 / G	
6	@R1 or @RS	0–7 S /	
7	@1000/123456 1000	0–7 CR LF	
8	@R1/123456 1000	0–7 CR LF	
9	@	/	Previous location was opened.
10	@ CTL-SHIFT-S	2 binary bytes	

17777766 - CPU error register, cleared by any write reference

R	0	15–8	Not used
R/	7	Illegal halt when set	
R/	6	Address error when set (odd or register I fetch)	
R/	5	Nonexistent memory	
R/	4	I/O bus timeout (no I/O page address)	
R/	3	Yellow stack trap	
R/	2	Red stack trap	
R	0	1–0	Not used

17777776 - Processor status register

R/W P	15–14	Current processor mode 00 Kernel 01 Supervisor or 40000 bit 10 Illegal or 100000 bit 11 User or 140000 bit
R/W P	13–12	Previous mode
R/W P	11	Register set, 0=set R0–R5, 1=set R0'–R5'
R 0	10–9	Unused, read as 0s
R/W	8	Reserved for future Digital use
R/W P	7–5	Processor interrupt priority level
R/W P	4	Trace trap (T-bit), 1=trap through vector 14
R/W	3–0	Processor condition codes NZVC

6.5 SYSTEM MODULE CONNECTORS

Tables 6-12 through 6-21 list all the connectors on the system module. Each connector is listed with pin and signal name.

Table 6-12 Memory Connector – J1
Table 6-13 Extended Bitmap Option Connector – J2
Table 6-14 Battery Connector – J3
Table 6-15 DC Power Connector – J4
Table 6-16 Video/Keyboard Connector – J5
Table 6-17 Printer Connector – J6
Table 6-18 Communications Connector – J7
Table 6-19 Remote Access Connector – J8
Table 6-20 NI Connector – J9
Table 6-21 Zero Insertion Force (ZIF) Connectors – J10, J11, J12, J13, J14, J15

Table 6-12 Memory Connector – J1

Pin	Signal
1	RASD1 L
2	GND
3	No connection
4	RASD2 L
5	+5 V
6	MUXA 1 L
7	+5 V
8	MUXA 2 L
9	GND
10	MUXA 0 L
11	GND
12	MUXA 4 L
13	GND
14	MUXA 7 L
15	GND
16	MUXA 3 L
17	D 03 H
18	D 04 H
19	D 02 H
20	D 05 H
21	D 01 H
22	D 06 H
23	D 00 H
24	D 07 H
25	D 08 H
26	D 15 H
27	D 09 H
28	D 14 H
29	D 10 H
30	D 13 H
31	D 11 H
32	MUXA 6 L
33	D 12 H
34	MUXA 5 L
35	GND
36	MUXA 8 L
37	GND
38	MWLB H
39	GND
40	RASD0 L
41	NBD0 L
42	CAS H
43	P256KD L
44	MWHB H
45	NBD1 L
46	No connection
47	RASD3 L
48	No connection

Table 6-13 Extended Bitmap Option Connector – J2

Pin	Signal	Pin	Signal
1	+5 V	2	+5 V
3	BRPLY L	4	INTRN L
5	IDAL 00 H	6	IDAL 01 H
7	IDAL 02 H	8	IDAL 03 H
9	IDAL 04 H	10	IDAL 05 H
11	IDAL 06 H	12	IDAL 07 H
13	GND	14	GND
15	IDAL 08 H	16	IDAL 09 H
17	IDAL 10 H	18	IDAL 11 H
19	IDAL 12 H	20	IDAL 13 H
21	IDAL 14 H	22	IDAL 15 H
23	BVID 0 H	24	BVID 1 H
25	IDAL 16 H	26	IDAL 17 H
27	IDAL 18 H	28	IDAL 19 H
29	IDAL 20 H	30	IDAL 21 H
31	IOSEL L	32	AS L
33	GND	34	GND
35	DS L	36	SDEN L
37	WLB L	38	WHB L
39	SS 6 L	40	INIT L
41	DCOK H	42	EBOPRES L
43	BVID 2 H	44	BVID 3 H
45	V20 MHz H	46	SI 1 H
47	SI 2 H	48	SI 3 H
49	HSYNC L	50	VSYNC L
51	VWAIT L	52	VDONE H
53	GND	54	GND
55	GVID 0 H	56	GVID 1 H
57	GVID 2 H	58	GVID 3 H
59	RVID 0 H	60	RVID 1 H
61	RVID 2 H	62	RVID 3 H
63	+5 V	64	CMPPRS L

Table 6-14 Battery Connector – J3

Pin	Signal
1	+3.6 V
2	GND

Table 6-15 DC Power Connector – J4

Pin	Signal
1	BDCOK H
2	KEY
3	BPOK H
4	−12 V
5	+12 V
6	+5 V
7	+5 V
8	+5 V
9	+5 V
10	GND
11	GND
12	GND
13	GND
14	GND
15	GND
16	GND

Table 6-16 Video/Keyboard Connector – J5

Pin	Signal	Backplane Pin
1	BLUE RETURN	87
2	GREEN RETURN	85
3	RED RETURN	83
4	MONO RETURN	89
5	GND	
6	GND	
7	+12 V	
8	+12 V	
9	BLUE VIDEO	88
10	GREEN VIDEO	86
11	RED VIDEO	84
12	MONO VIDEO	90
13	MON PRES L	
14	KBD RDATA	
15	KBD XDATA	

Table 6-17 Printer Connector – J6

Pin	Signal	CCITT V.24	EIA RS-232-C
1	Protective GND	101	AA
2	Transmit data	103	BA
3	Receive data	104	BB
4	PIN4 L		
5	Data terminal ready	108/2	CD
6	Data set ready	107	CC
7	Signal GND	102	AB
8	GND		
9	Terminal L		

Table 6-18 Communications Connector – J7

Pin	Signal	CCITT V.24	EIA RS-232-C
1	Protective GND	101	AA
2	Transmit data	103	BA
3	Receive data	104	BB
4	Request to send	105	CA
5	Clear to send	106	CB
6	Data set ready	107	CC
7	Signal GND	102	AB
8	Carrier detect	109	CF
9			
10			
11			
12	Speed mode indication	112	CI
13			
14			
15	Transmit clock (DCE)	114	DB
16			
17	Receive clock (DCE)	115	DD
18	Local loopback	141	
19			
20	Data terminal ready	108/2	CD
21	Remote loopback	140	
22	Ring indicator	125	CE
23	Data signal rate select	111	CH
24	Transmit clock (DTE)	113	DA
25	Test indicator	142	

Table 6-19 Remote Access Connector – J8

Pin	Signal	Backplane Pin
1	RAL 01	61
2	RAL 02	62
3	RAL 03	63
4	GND	
5	RAL 04	64
6	RAL 05	65
7	+12 V	
8	RAL 06	66
9	RAL 07	67
10	GND	
11	RAL 08	68
12	RAL 09	69
13	+5 V	
14	RAL 10	70
15	RAL 11	71
16	GND	
17	RAL 12	72
18	RAL 13	73
19	−12 V	
20	RAL 14	74
21	RAL 15	75
22	RAL 16	76

Table 6-20 NI Connector – J9

Pin	Signal	Backplane Pin
1	Shield	
2	Collision presence +	81
3	Transmit +	77
4		
5	Receive +	79
6	Power return (GND)	
7		
8		
9	Collision presence −	82
10	Transmit −	78
11		
12	Receive −	80
13	Power (+12 V)	
14		
15		

Table 6-21 Zero-Force-Insertion (ZIF) Connectors – J10, J11, J12, J13, J14, J15

Pin	Signal	Termination	Bus Driver	Bus Receiver
1	BDCOK H			8640
2	+5 V			
3	BPOK H			8640
4	GND			
5	BINIT L	1	74S05	
6	−12 V			
7	BDAL 15 L	1	8307	8307
8	BDAL 13 L	1	8307	8307
9	BDAL 14 L	1	8307	8307
10	BDAL 12 L	1	8307	8307
11	BSPARE 0	2		
12	BDAL 11 L	1	8307	8307
13	BRPLY L	1	74S05	CMOS
14	BDAL 10 L	1	8307	8307
15	GND			
16	BDAL 09 L	1	8307	8307
17	BMDEN L	1	74S241	74S241
18	BDAL 08 L	1	8307	8307
19	BWRITE L	1	74S241	74S241
20	BDAL 07 L	1	8307	8307
21	BWLB L	1	74S241	74S241
22	BDAL 06 L	1	8307	8307
23	BWHB L	1	74S241	74S241
24	BDAL 05 L	1	8307	8307
25	BSDEN L	1	74S241	74S241
26	BDAL 04 L	1	8307	8307
27	GND			
28	BDAL 03 L	1	8307	8307
29	SS n L		74S138	
30	BDAL 02 L	1	8307	8307
31	IRQB n L	2	CMOS	CMOS
32	BDAL 01 L	1	8307	8307
33	IRQA n L	2	CMOS	CMOS
34	BDAL 00 L	1	8307	8307
35	OPRES n L	3		74LS240
36	GND			
37	BDS L	1	74S241	74S241
38	+5 V			
39	BAS L	1	74S241	74S241
40	+12 V			
41	BSPARE 2	2		
42	BSPARE 3	2		
43	BIOSEL L	1	74S241	74S241
44	BDAL 21 L	1	8307	8307
45	BP 0 L	1		

Table 6-21 Zero-Force-Insertion (ZIF) Connectors - J10, J11, J12, J13, J14, J15 (Cont)

Pin	Signal	Termination	Bus Driver	Bus Receiver
46	BDAL 20 L	1	8307	8307
47	BP 1 L	1		
48	BDAL 19 L	1	8307	8307
49	BSPARE 1	2		
50	BDAL 18 L	1	8307	8307
51	GND			
52	BDAL 17 L	1	8307	8307
53	BMER L	1		CMOS
54	BDAL 16 L	1	8307	8307
55	DMR n L	2		CMOS
56	DMG n L	2	74LS138	
57	BBUSY L	1		CMOS
58	+5 V			
59	BSPARE 4	2		
60	GND			
61	RAL 01			
62	RAL 02			
63	RAL 03			
64	RAL 04			
65	RAL 05			
66	RAL 06			
67	RAL 07			
68	RAL 08			
69	RAL 09			
70	RAL 10			
71	RAL 11			
72	RAL 12			
73	RAL 13			
74	RAL 14			
75	RAL 15			
76	RAL 16			
77	TRANSMIT +			
78	TRANSMIT −			
79	RECEIVE +			
80	RECEIVE −			
81	COLLISION PRESENCE +			
82	COLLISION PRESENCE −			
83	RED RETURN			
84	RED VIDEO			
85	GREEN RETURN			
86	GREEN VIDEO			
87	BLUE RETURN			
88	BLUE VIDEO			
89	MONO RETURN			
90	MONO VIDEO			

CHAPTER 7
BIT MAP VIDEO CONTROLLER AND EXTENDED BIT MAP MODULES

7.1 INTRODUCTION

The bit map video controller and extended bit map are the display control components of the video subsystem for the Professional 350 system. Figure 7-1 shows the bit map video controller and extended bit map modules' relationship to the other components which make up the Professional 350 system.

7.1.1 Related Documentation

Refer to the *VC241 Extended Bit Option Field Maintenance Print Set* (MP-01471-00) while reading this chapter.

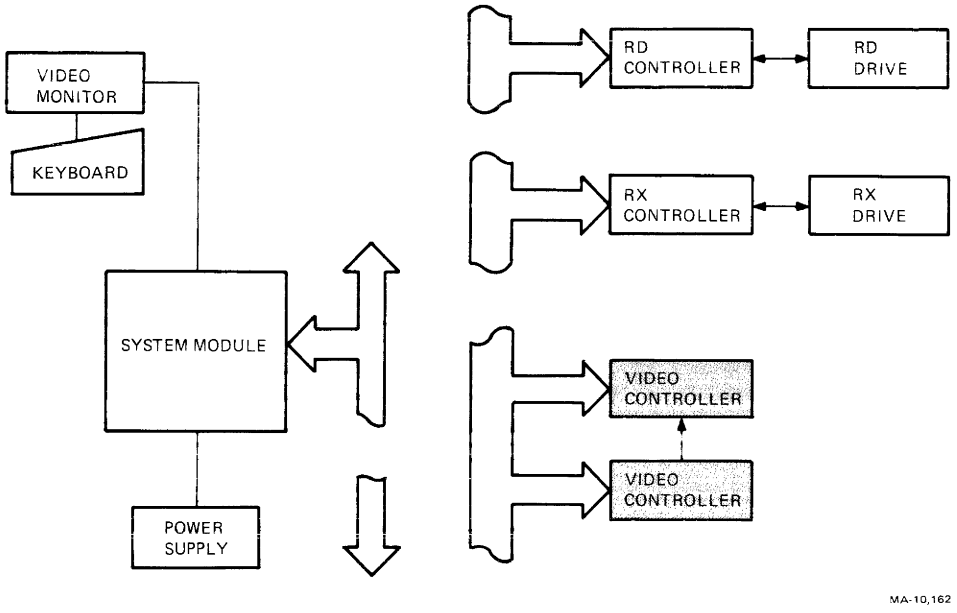


Figure 7-1 System Block Diagram

7.1.2 General Information

The bit map video controller and extended bit map modules generate video drive signals for a monochrome or color monitor (Figure 7-2). Both modules are 5.2 × 12-inch field replaceable units (FRU). The bit map video controller (FRU PN 54-15138) occupies one slot of the CTI Bus option space in the Professional 350 card cage. This module is a required component for a video subsystem of the Professional 350 system. The extended bit map (FRU PN 54-15146) occupies the slot on the CTI Bus following the bit map video controller.

The extended bit map module is optional for a video subsystem that supports only monochrome monitors. For this application, the module provides two additional planes of video display storage.

The extended bit map module is required for a video subsystem that supports both color and monochrome monitors. For a color monitor the module supplies data storage and video generation for green and red video signals (nonmapped mode) or data storage and color mapped video generation.

A zero insertion force (ZIF) connector (J1) at the bottom of each module makes the module compatible to the CTI Bus. This connector allows the host processor to control the operations of the controller from the CTI Bus.

One cable (PN 17-00303) connects the bit map video controller module to the extended bit map module, at connectors (J2) at the top of each module. The bit map video controller is the master of the extended bit map. It directs the operations of the extended bit map module via signals passed over this cable. Each module can be accessed directly. For data transfers between the host processor and the extended bit map, the host processor accesses the bit map video controller to control receiving or sending data over the CTI Bus to the extended bit map.

Refer to Chapter 5 for the connector description and signal definitions for J1. Refer to Section 11.4 for the connector descriptions and signal definitions for J2.

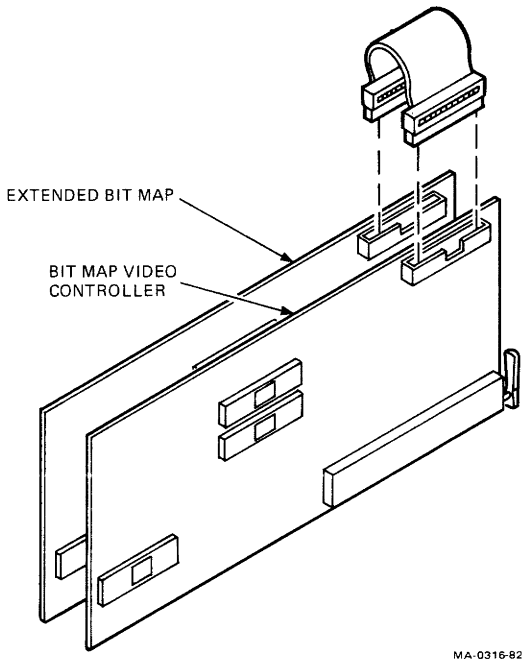


Figure 7-2 Bit Map Video Controller and Extended Bit Map Modules

7.2 FUNCTIONAL COMPONENTS

The following sections describe the functional components of the bit map video controller and the extended bit map modules of the Professional 350 system.

7.2.1 Bit Map Video Controller Circuit Components

To the host processor, the bit map video controller appears as a set of registers and 16K words (32 kilobytes) of video memory that is accessible from the CTI Bus. The host processor reads and writes to the registers to issue video memory data modification commands to the controller and to select video display characteristics. The host processor directly accesses the video memory (16K word video bit maps) for read-modify-write operations. Refer to the register definitions in Section 11.5 for more information.

Data transfers between the video memory and the host processor are program controlled by the host processor. Under this program, the host processor reads and writes to the video memory on the bit map video controller. The video memory appears as a 16K word (32 kilobyte) page in the host processor address space. The controller sequentially reads the video memory and converts the data to a video drive signal. This signal contains the necessary vertical and horizontal synchronization pulses and equalization pulses to drive a display monitor.

The bit map video controller module contains one bit map (video memory) to provide one plane of displayable data. This plane is displayed in one of three register-selectable horizontal resolution modes: 1024, 512, or 256 pixel resolution. In the 1024 pixel resolution mode, each bit in memory controls one screen pixel; the pixel can be on or off. In the 512 pixel resolution mode, two memory bits control each screen pixel; the pixels are twice as big as in the 1024 pixel mode and have one of four intensity levels. In the 256 pixel resolution mode, four memory bits control one screen pixel; the pixels are four times as big as in the 1024 pixel mode and have one of 16 intensity levels.

Figure 7-3 is a simple block diagram of the bit map video controller module. This module contains circuits that access commands and control the data flow on the bit map video controller and the extended bit map modules. These circuits are the video memory control circuits, CTI Bus to memory access circuits and register access control circuits.

The bit map video controller consists of the following circuits (Figure 7-3).

CTI Bus interface
CTI Bus register access
Registers
CTI Bus video memory access
Video memory control and update
Video memory
Clock generator
Video generator

7.2.1.1 CTI Bus Interface Circuits – The host processor gains access to the video subsystem through these circuits by reading and writing to the bit map video controller and extended bit map registers and video memories. For the host processor to access video subsystem, the CTI Bus interface circuits perform the following functions.

1. Acknowledge accesses to the bit map video controller or the extended bit map registers and video memories by the host processor

2. Pass data between the host processor and bit map video controller registers and video memory

3. Pass interrupts to the host processsor to indicate vertical retrace and the completion of a command

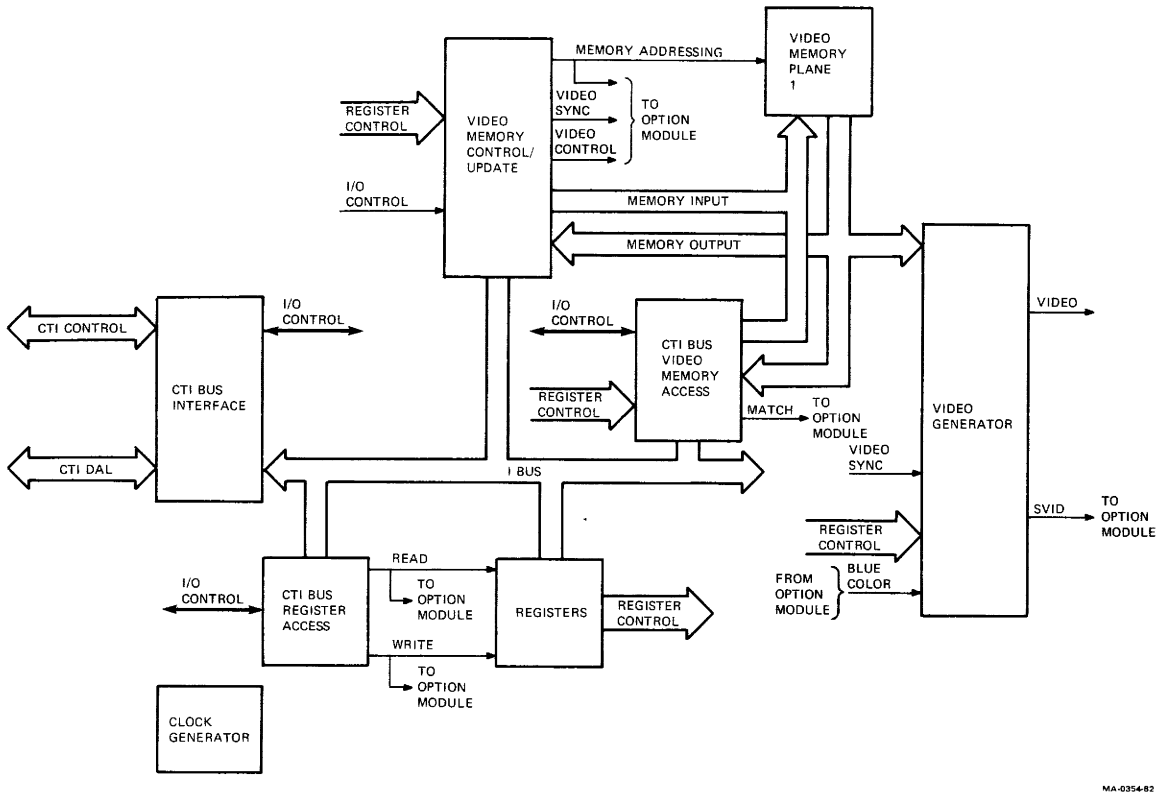


Figure 7-3 Bit Map Video Controller Block Diagram

7.2.1.2 CTI Bus Register Access Circuits – When the host processor accesses a register in the bit map video controller or the extended bit map, the CTI Bus interface circuits pass the address and I/O control signals to the CTI Bus register access circuits. These circuits decode the address and I/O control signals to generate register read and write signals for registers on the bit map video controller and the extended bit map modules.

7.2.1.3 Registers – The bit map video controller contains nine registers which can be read or written to by the host processor. Access to these registers allows the host processor to control the bit map video controller and the extended bit map modules and access status data. These registers provide register control signals for the video memory control/update circuits, video generator, and the extended bit map. Refer to Section 7.5 for detailed information on each register.

7.2.1.4 CTI Bus Video Memory Access – The bit map video controller contains one bit map memory plane (video memory). The host processor can read or write to this memory through the CTI Bus interface circuits and the CTI Bus video memory access circuits. For the host processor to access the video memory, these circuits perform the following operations.

1. Determines if an address on the CTI Bus from the host processor is in the video memory address page

2. Passes data between the video memory and the CTI Bus interface circuits for the host processor

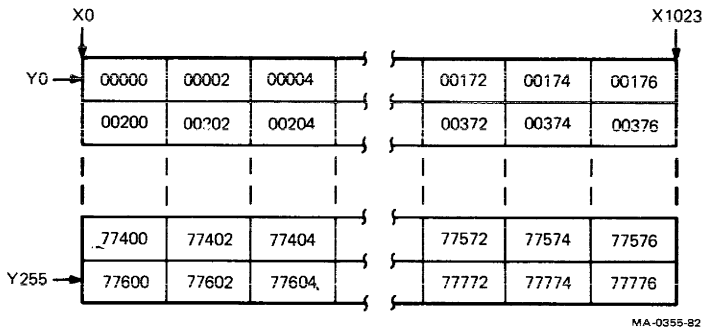


Figure 7-4 Video Memory Bit Map Layout

7.2.1.5 Video Memory Control and Update Circuits – These circuits synchronize the bit map video controller and the extended bit map modules operations. During most operations, the video memory is accessed. These circuits control read-modify-write operations and read-only accesses to the video memory. The read-modify-write operations occur during host processor accesses and video memory update modification operations to the video memory. The read only operations sequentially pass the video memory data to the video generator to refresh the screen.

To perform these operations, the video memory control and update circuits perform the following operations.

1. Generate video memory addresses for read-modify-write and read-only operations
2. Generate video sync signals for the video generator
3. Perform logical operations on data stored in the bit map video controller video memory
4. Pass video timing and video memory address signals to the extended bit map module

7.2.1.6 Video Memory – The video memory is a 16K × 16-bit word memory and is addressed by the video memory control and update circuits. During read-modify-write cycles, addressed data passes between the video memory, the video memory control and update circuits, and the CTI Bus video memory access curcuits. During read-only cycles, sequentialy addressed data passes from the video memory to the video generator circuits.

This memory is mapped such that each bit (or group of bits) directly controls a video screen pixel (Figure 7-4). The bit map arrangement provides a greater horizontal resolution than vertical resolution. For vertical resolution, up to 255 lines of data are available, however, the line spacing is fixed. For horizontal resolution, each line is controlled by 1024 bits of information. This allows for the selection of three different pixel lengths and up to 16 different pixel intensities.

7.2.1.7 Video Generator Circuit – The video generator circuit generates a composite video drive signal for a monochrome or color monitor. This signal is generated from data stored in the video memory and video sync signals from the video memory control and update circuits.

The video generator circuit can operate in one of three monochrome resolution modes selected by the register control signals (nonmapped). For mapped operation, the video generator serializes data from the video memory and passes it to the extended bit map module. The extended bit map then returns color map control signals to the video generator. This generates a blue video drive signal and a monochrome video drive signal. The generated video drive signal is passed to the CTI private Bus and then routed to the connector on the system box.

7.2.2 Extended Bit Map Module Circuit Components

With the exception of the color map register, the circuits on the extended bit map module operate like the circuits on the bit map video controller module. The extended bit map module is optional when the video subsystem supports a monochrome monitor. It provides two additional 16K word video memory planes for the video subsystem. The extended bit map module is required when the video subsystem supports a color monitor.

When the module is used for color video signal generation, it can operate in two modes: nonmapped or mapped. For mapped modes, video memory plane 1 on the bit map video controller module contains the display data for generating a primary blue video. The extended bit map module video memory planes 2 and 3 store data for generating primary green and red video.

When the subsystem operates in the mapped mode, the video memory planes store addresses for an eight word color map register (CMR). The CMR provides data control signals to the three video generators for blue, green, and red signals. The simultaneously addressed video memory planes each provide serial data to the CMR. One bit from each plane provides a 3-bit address to the CMR. The host processor preloads each of the CMR locations with a data word to select one of 256 possible colors.

When a CMR location is addressed by the 3 data bits formed from each of the three planes, color map signals are sent to each video generator. These signals control each video generator to set the intensity level for each primary color pixel in a color cluster to show one of eight colors.

For monochrome monitors, all three video memory planes operate in either mapped or nonmapped modes. Refer to Section 7.2.1 for the resolution modes the video memory planes can operate in while the subsystem is in nonmapped operation. Each plane can also be turned on or off under program control. This allows for any combination of displayed planes.

Figure 7-5 is a simple block diagram of the extended bit map module circuit. This module requires control, timing, and video memory addressing signals from the bit map video controller module to perform its operations. When this module is accessed directly by the host processor, it returns an identification byte to the host processor. Host processor accesses to the bit map video controller module provide accesses to the extended bit map module's registers and its video memory planes.

The extended bit map module contains the following circuits.

CTI Bus interface
Plane and color map registers
Two CTI Bus video memory access circuits
Two video memory update circuits
Two video memories
Two video generator circuits

7.2.2.1 CTI Bus Interface Circuit – The CTI Bus interface circuits can be accessed in two modes, direct and indirect host processor accesses. For direct host processor accesses to the extended bit map modules register address space, these circuits place a module identification code on the CTI Bus. For an indirect access to the extended bit map module, the host processor accesses the bit map video controller module which generates control signals for the CTI Bus interface circuit. These control signals enable the circuits to pass I/O control signals and data between the CTI Bus and the module's internal bus.

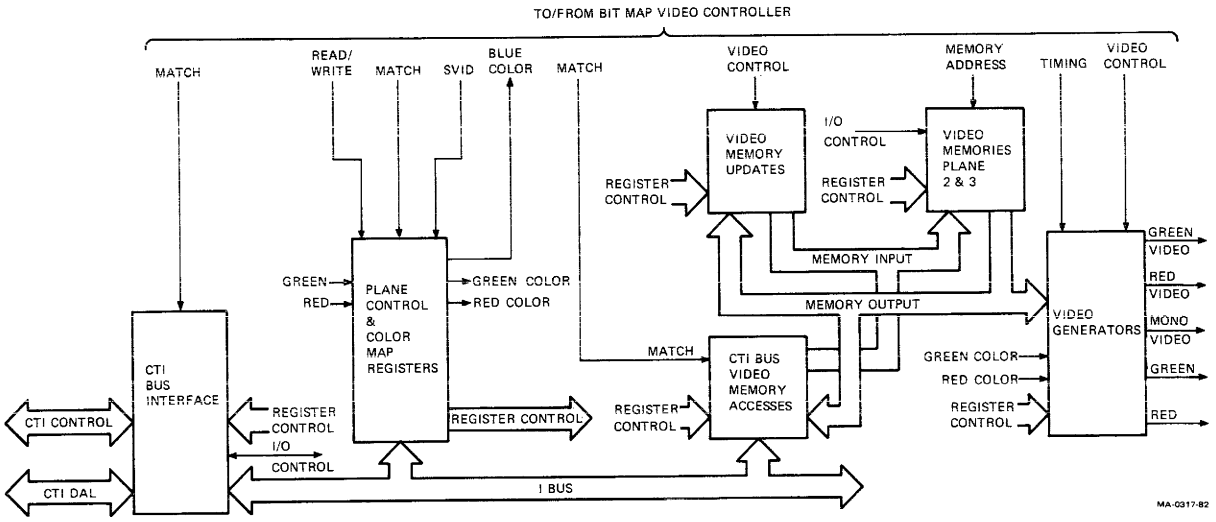


Figure 7-5 Extended Bit Map Block Diagram

7.2.2.2 Plane and Color Map Registers – The bit map video controller module enables these registers for writing and reading. Data is passed between the registers and the CTI Bus through the CTI Bus interface circuits. The plane register allows the host processor to control each plane's resolution and update modification mode, and enables each plane for operation. The color map register selects eight displayable colors during the video subsystem's mapped operation.

7.2.2.3 CTI Bus to Video Memory Access Circuits – The extended bit map contains two CTI Bus video memory access circuits, one for each video memory plane: plane 2 (green plane) and plane 3 (red plane). These circuits are controlled by the bit map video controller and the extended bit map plane 2 and 3 control register. These circuits allow data to pass between these respective video memories and the host processor through the CTI Bus interface circuits.

7.2.2.4 Video Memory Update Circuits – The extended bit map contains two video memory update circuits, one for each video memory plane: plane 2 (green plane) and plane 3 (red plane). These circuits are controlled by the bit map video controller and the extended bit map plane 2 and 3 control register. These circuits allow logical operations to be performed on data stored in their respective video memory planes.

7.2.2.5 Video Memory – The extended bit map contains two video memory planes: plane 2 (green plane) and plane 3 (red plane). Each video memory plane is a 16K × 16-bit word memory plane and is mapped like plane 1 (blue plane) on the bit map video controller (Section 7.2.1.6).

Both video memory planes are addressed by the bit map video controller for read-modify-write and read-only cycles. The CTI Bus interface circuits provide additional I/O control signals to the video memories during read-modify-write cycles. The plane 2 and 3 control register provides control signals to select each plane during read-modify-write cycles.

During read-modify-write cycles, addressed data passes between the video memory, the video memory update circuits, and the CTI Bus video memory access circuits. For read-only cycles sequentially addressed data passes from the video memory to its respective video generator circuits during nonmapped operation, or to the color map during mapped operation.

7.2.2.6 Video Generator – The extended bit map contains two video generator circuits, one for each respective video memory plane: plane 2 (green plane) and plane 3 (red plane). The video generator circuits are controlled by the bit map video controller and the extended bit map plane 2 and 3 control register. Each video generator generates a video signal to drive a monochrome or color monitor. The video signal is generated from data stored in the video memory for nonmapped operations or by the color map for mapped operations. The plane 2 (green) video generator also receives and passes video synchronization signals from the bit map video controller.

For nonmapped operations, each video generator circuit can operate in one of three resolution modes. For mapped operations, each video generator serializes data from its video memory and passes it to the color map register (CMR). The CMR then returns color map control signals to each video generator for controlling its video drive signals' generation. Each video drive signal is passed to the CTI private Bus and routed to the connector on the system box.

7.3 THEORY OF OPERATION

The following section describes the theory of operation of the bit map video controller and the extended bit map modules of the Professional 350 system.

7.3.1 Bit Map Video Controller Detailed Operation

The bit map video controller is a required module for generating composite video signals for the Professional 350 system. This module contains the following circuits.

CTI Bus interface
CTI Bus register access
Registers
CTI Bus video memory access
Video memory control and update
Video memory
Clock generator
Video generator

7.3.1.1 CTI Bus Interface Detailed Operation – The CTI Bus interface circuit passes CTI Bus control signals, data, and addresses between the host processor and the bit map video controller (Figure 7-6). To perform this function, this circuit uses the following components.

CTI Bus control signal buffer
CTI Bus high byte data address buffer
CTI Bus data address transceiver
Transmit decoder

CTI Bus I/O Control Signal Buffering

All control signals passed between the bit map video controller and the CTI Bus are buffered to isolate the current drain of the module from the CTI Bus. Table 7-1 lists the CTI Bus control signals and their functions on the module.

Refer to Chapter 5 for further information on CTI Bus control signal timing sequences.

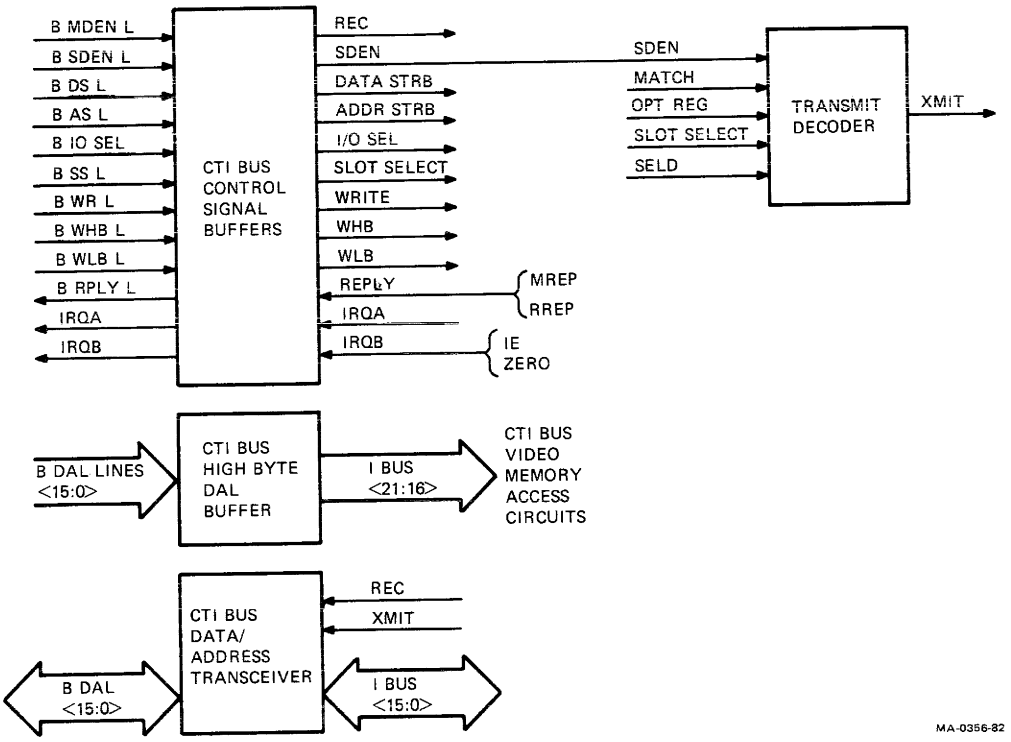


Figure 7-6 CTI Bus Interface Circuit Operation

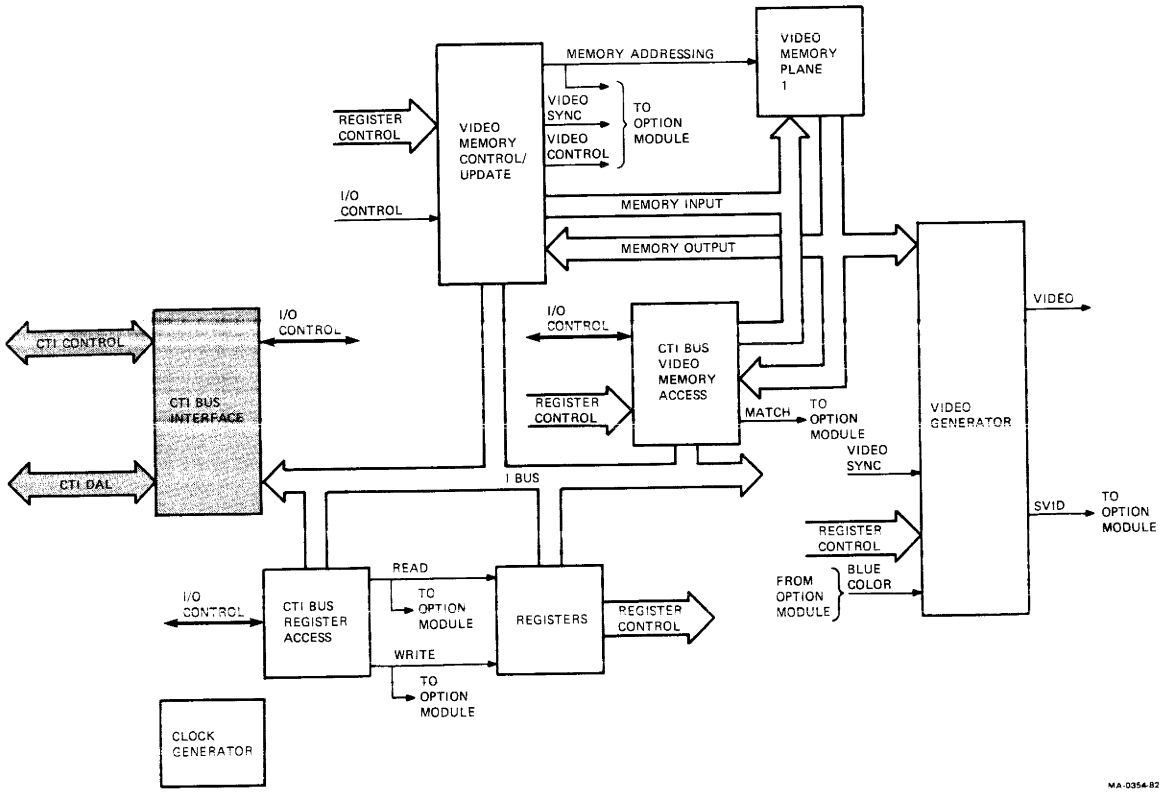


Table 7-1 CTI Bus Control Signal Functions

CTI Bus Signal	Module Signal	Function
B MDEN L	REC	Controls module to accept addresses or data from the CTI Bus
B SDEN L	SDEN	Enables transmit decoder
B AS L	ADDR STRB	Enables the module to latch the address on the CTI Bus into the register access control, CTI Bus to video memory access, and video memory control/update circuits
B DS L	DATA STRB	Enables the module to pass data between its registers or video memory and the CTI Bus
B IOSEL L	I/O SEL	Enables the CTI Bus to video memory access circuits
B SS L	SLOT SELECT	Enables host processor access to the modules registers
B WR L	WRITE	Enables the host processor to write words to the module (accept data from the CTI Bus) or read words from the module (pass data to the CTI Bus)
B WHB L	WHB	Enables the host processor to write high bytes to the module (accept data from the CTI Bus) or read high bytes from the module (pass data to the CTI Bus)
B WLB L	WLB	Enables the host processor to write low bytes to the module (accept data from the CTI Bus) or read low bytes from the module (pass data to the CTI Bus)
B RPLY L	REPLY	An acknowledgement signal from the module to the host processor, it indicates the host processor properly accessed a register or a video memory plane on either the bit map video controller or the extended bit map.
B IRQA L	IRQA	An interrupt signal from the module to the host processor, it indicates the module is performing a vertical retrace.
B IRQB L	IRQB	An interrupt signal from the module to the host processor, it indicates the counter register is empty.

CTI Bus To/From Internal Bus Address and Data
All addresses and data pass between the host processor and the bit map video controller via the CTI Bus B DAL lines. A CTI Bus high byte DAL buffer isolates the B DAL <21:16> lines from the module's internal bus (I BUS <21:16>). These lines are used only during video memory addressing sequences (Section 7.3.1.4). The CTI Bus data/address transceivers isolate the B DAL <15:00> lines from the module's internal bus (I BUS <15:00>). The receive (REC) signal from the CTI Bus control signal buffers enable these transceivers to pass data or addresses on the CTI Bus to the internal bus. The transmit (XMIT) signal from the transmit decoder enables these transceivers to pass data on the internal bus to the CTI Bus.

The host processor controls the module to receive addresses and data with the CTI Bus signal B MDEN L (REC). When the module transfers data to the CTI Bus, the CTI Bus signal B SDEN L enables a transmit decoder. This decoder generates a transmit signal for the transceiver for two conditions, video memory access or bit map video controller register access.

For video memory accesses, the SDEN signal enables the transmit decoder. The decoder looks for a MATCH and a SELD signal. The MATCH signal, from the CTI Bus to video memory circuit, indicates a host processor access to the video memory address range. The SELD signal, from the plane 1 control register, indicates that the video memory plane is enabled.

For bit map video controller register access, the transmit decoder is enabled by SDEN, OPT REG, and SLOT SELECT. The XMIT signal is enabled if the SLOT SELECT signal indicates that the module is selected and the OPT REG signal indicates that the accessed register is on the bit map video controller.

7.3.1.2 CTI Bus Register Access Detailed Operation – The CTI Bus register access circuit decodes register addresses from the host processor and generates register read and write strobes (Figure 7-7). The strobes are generated for registers on the bit map video controller and the extended bit map. To perform this function, this circuit uses these two components.

Address latch
Register access decoder

When the CTI Bus interface circuits pass a video subsystem register address to the I BUS, they also pass an ADRS STRB signal to the address latch. Six address bits are loaded into the latch for decoding (I BUS <6:1> to ADDRESS<6:1>). These bits allow access to 64 registers on word boundaries between address 0 and 176 (HEX).

The register access decoder generates register read and write strobes only to existing registers. If a nonexisting register is addressed, the decoder does not generate a read or write strobe. If SLOT SELECT is asserted during a DATA STRB, the decoder generates an RREP register reply (RREP) for the CTI Bus interface circuits. This occurs regardless of the address register.

The CTI Bus I/O control signals from the CTI Bus interface circuit enable and clock the decoder. The generation of a read or write strobe from the decoded address is direct. If REC and SLOT SELECT are asserted during a data strobe, an address of 20 (HEX) with the WRITE, WHB, and WLB unasserted generates an RD20 strobe.

If an extended bit map register is addressed (RD10, WR10, RD12, or WR12), the OPT REG signal is asserted. This disables the CTI Bus interface circuits and enables circuits on the extended bit map module.

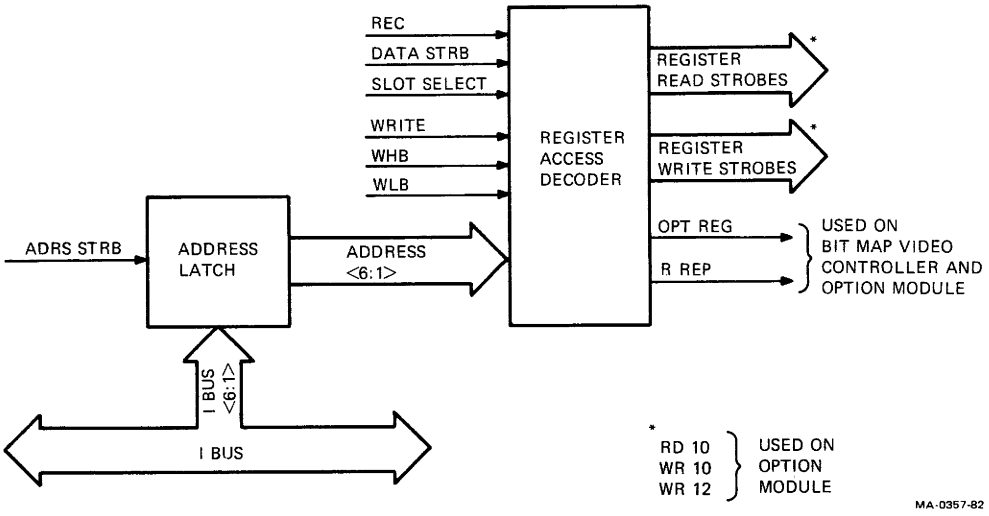
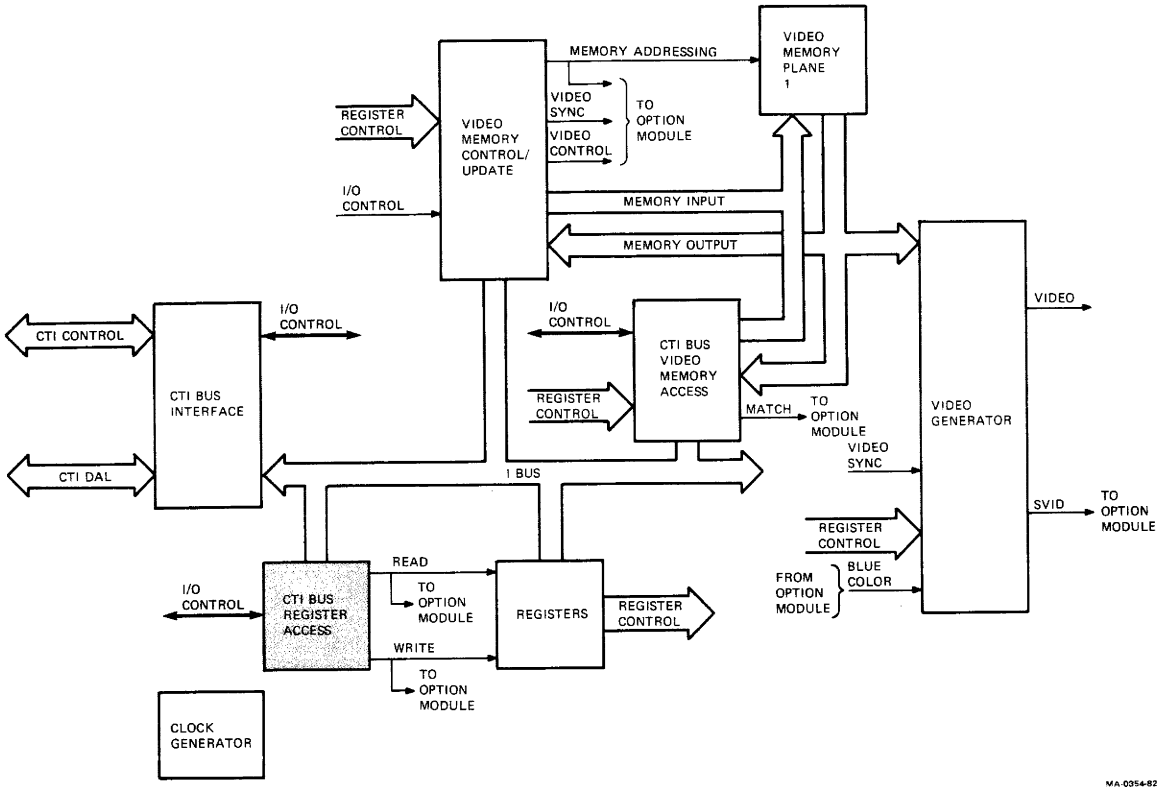


Figure 7-7 CTI Bus Register Access Circuit Operation



7.3.1.3 Registers – The bit map video controller contains nine registers. The host processor uses these registers to identify, control, and acquire status information from the controller. Registers are accessed through the CTI Bus register access circuits. Table 7-2 lists the addresses, access, and operation of each register. Figures 7-8 through 7-15 show the operation and location of each register. They also show the control and status signal interfacing the registers to the remaining bit map video controller circuits. Refer to Section 7.5 for further information about the registers.

Table 7-2 Controller Register Access Functions

Address	Access	Operation
XXXXXX00	Read-only	Provides the identification code of the bit map video controller to the host processor
XXXXXX04	R/W	The control and status register of the bit map video controller, it is cleared upon initialization of the module. The low byte of this register is in the video controller chip (DC715), the high byte is a discrete register. The high and low bytes can be written to independently. A read operation provides both high and low byte information.
XXXXXX06	R/W	The plane register which selects the operational mode of the video data chip (DC716) and the video generator on the bit map video controller
XXXXXX14	R/W	The scroll register contained in the video controller chip (DC715) on the bit map video controller
XXXXXX16	R/W	The X coordinate register contained in the video processor chip (DC717) used during video memory update operations
XXXXXX20	R/W	The Y coordinate register contained in the video processor chip (DC717) and used during video memory update operations
XXXXXX22	Write-only	The counter register indicates the number of read-modify-write cycles the host processor performs to the video memory.
XXXXXX24	Write-only	The pattern register used as the LSB data during read-modify-write cycles to the video memory, this register must be loaded before the counter register.
XXXXXX26	Write-only	The memory base register sets the 16K page location of the video memory for host processor access.

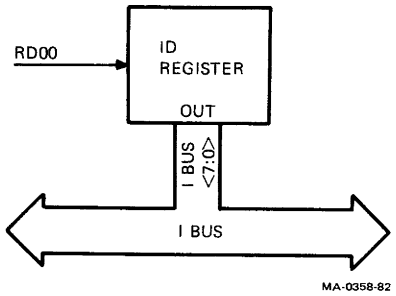
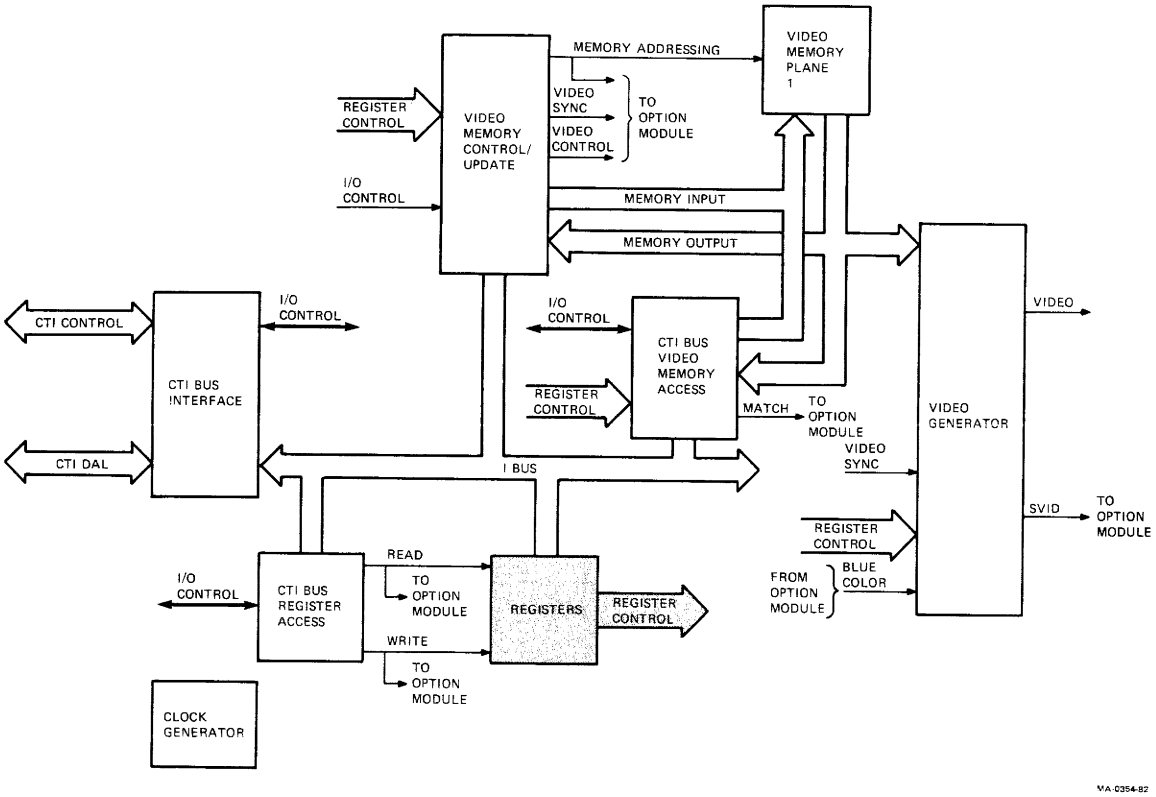


Figure 7-8 ID Register Operation



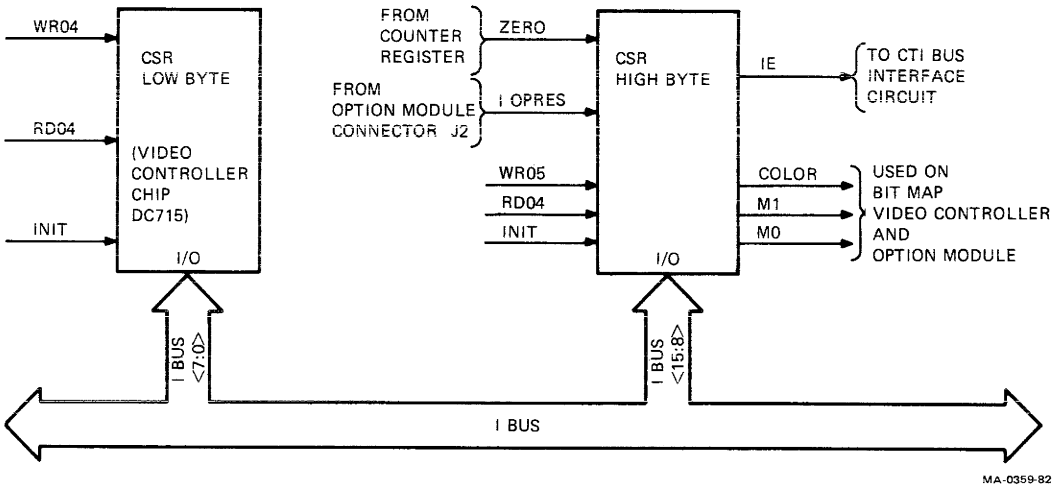
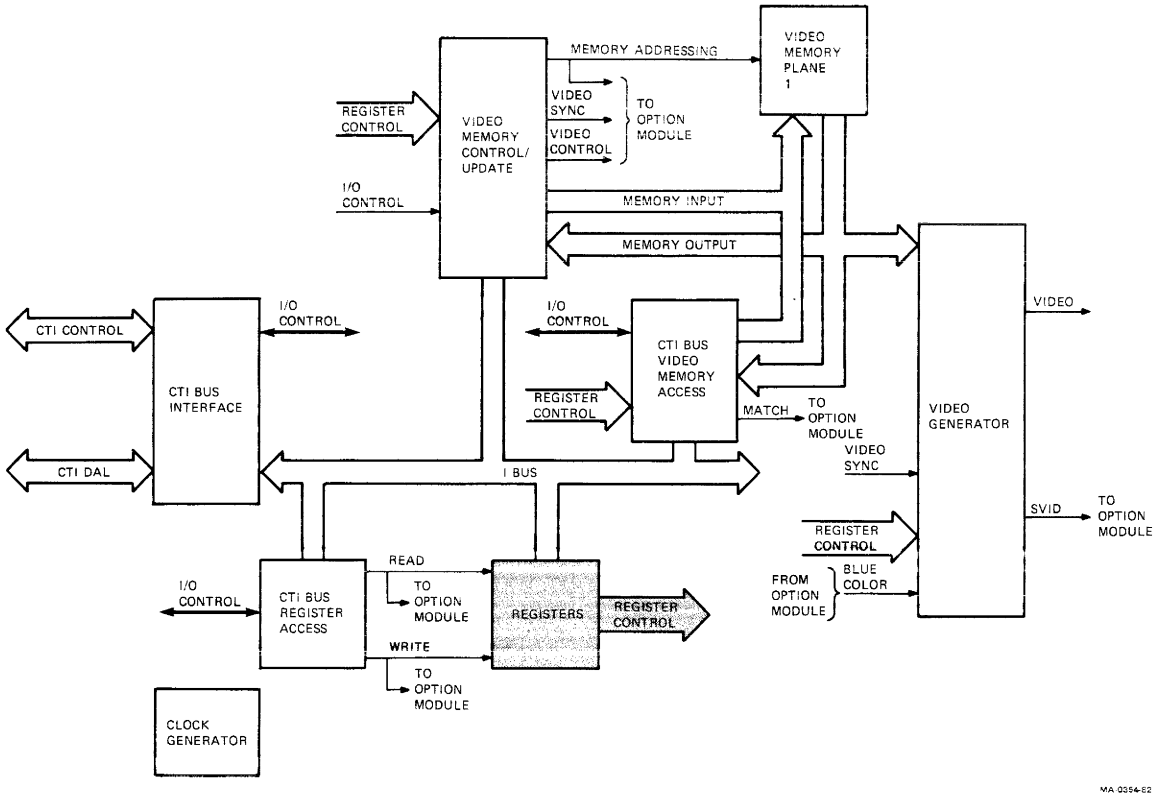


Figure 7-9 CSR Register Operation



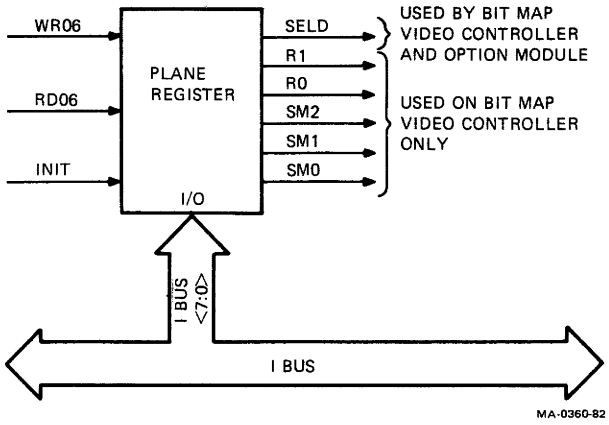
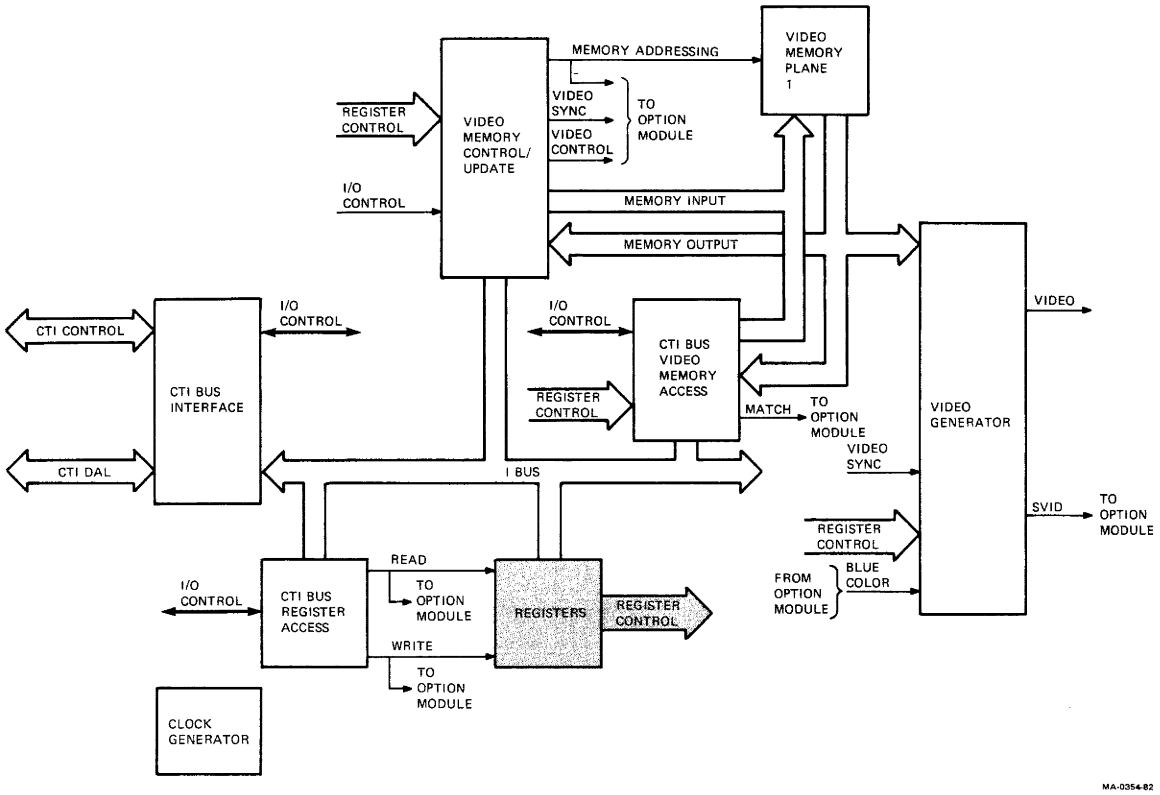


Figure 7-10 Plane Register Operation



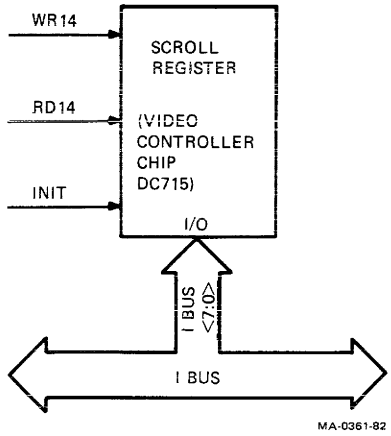
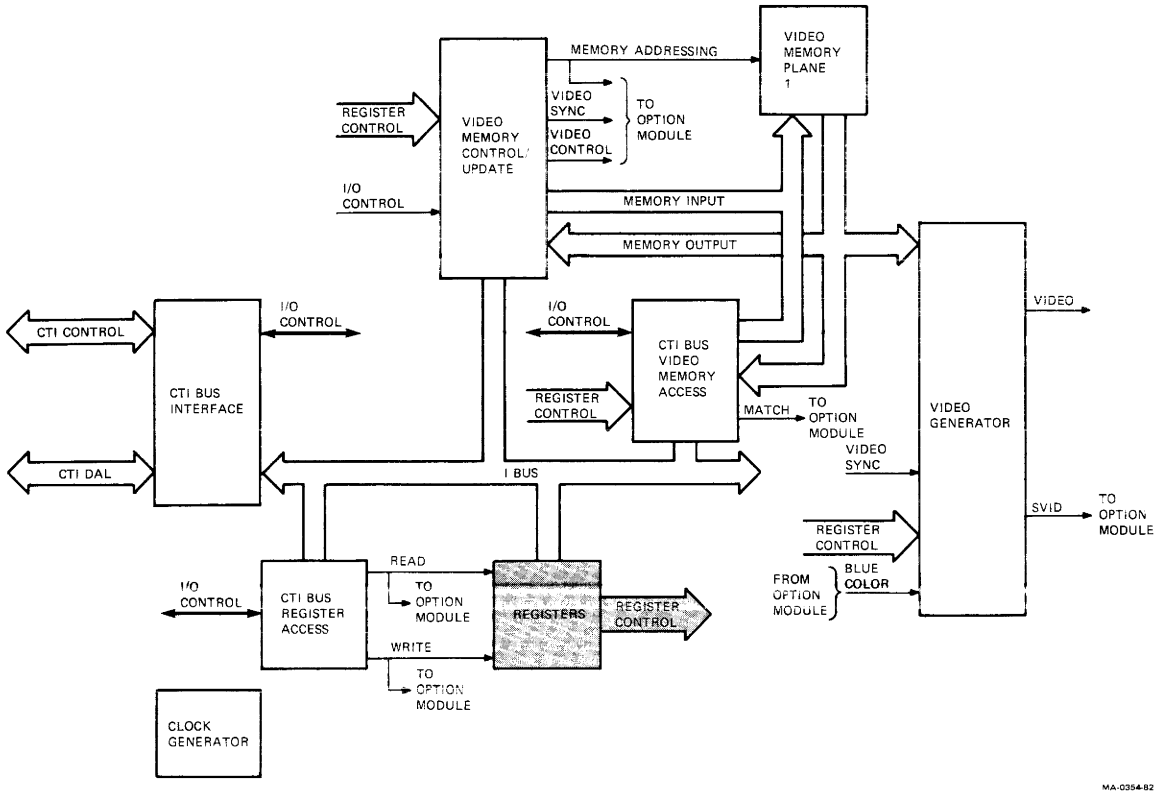


Figure 7-11 Scroll Register Operation



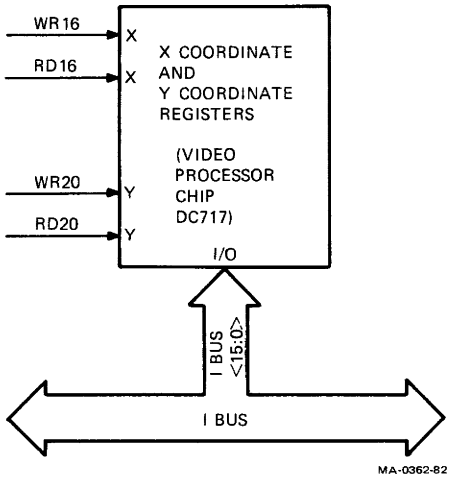
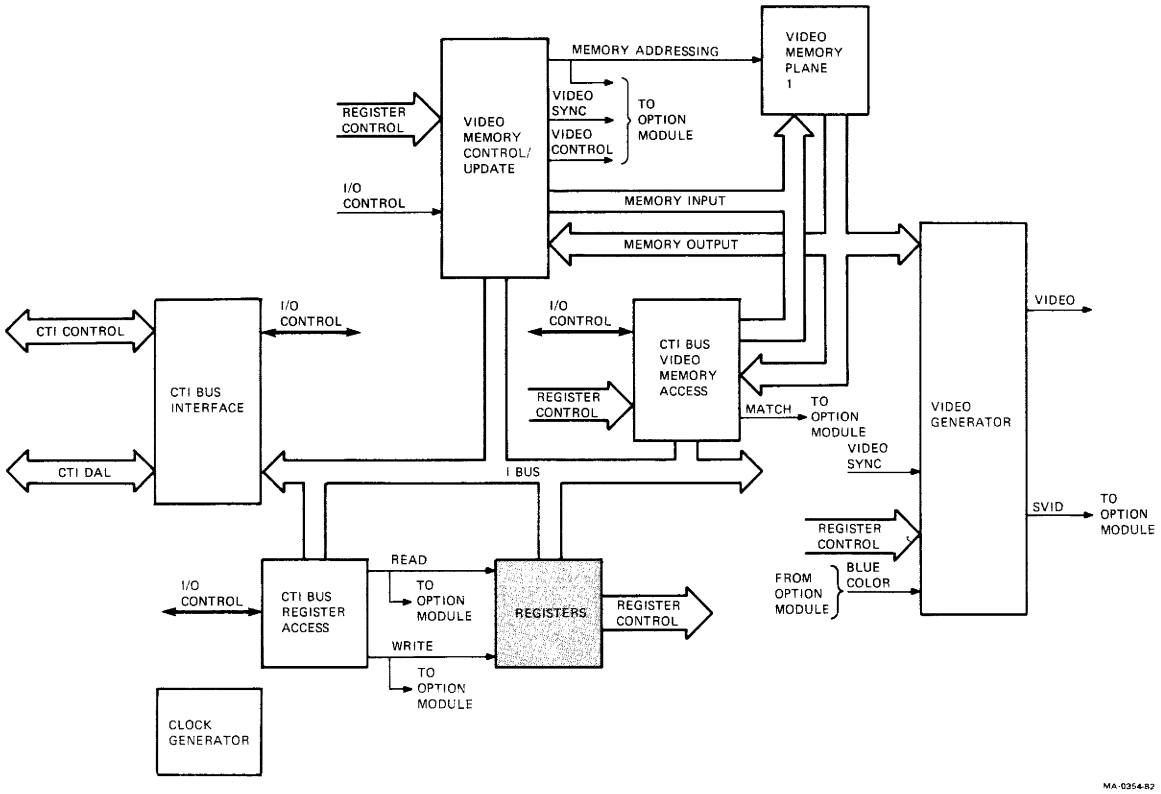


Figure 7-12 X and Y Coordinate Register Operation



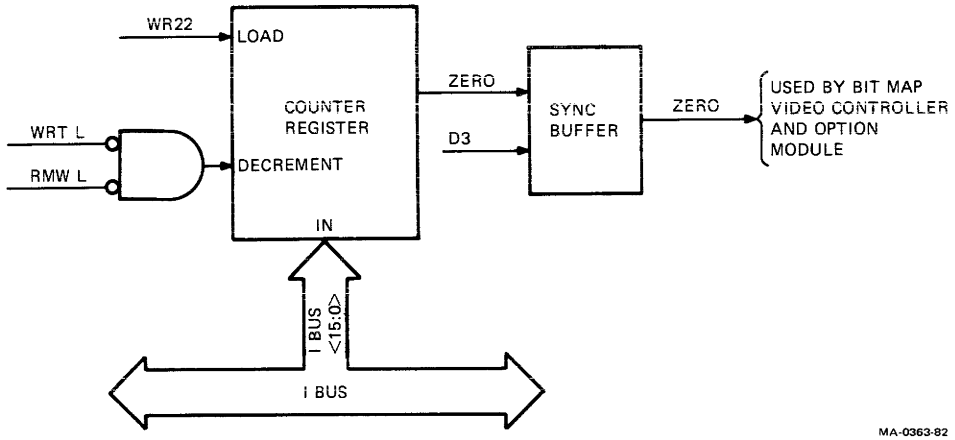
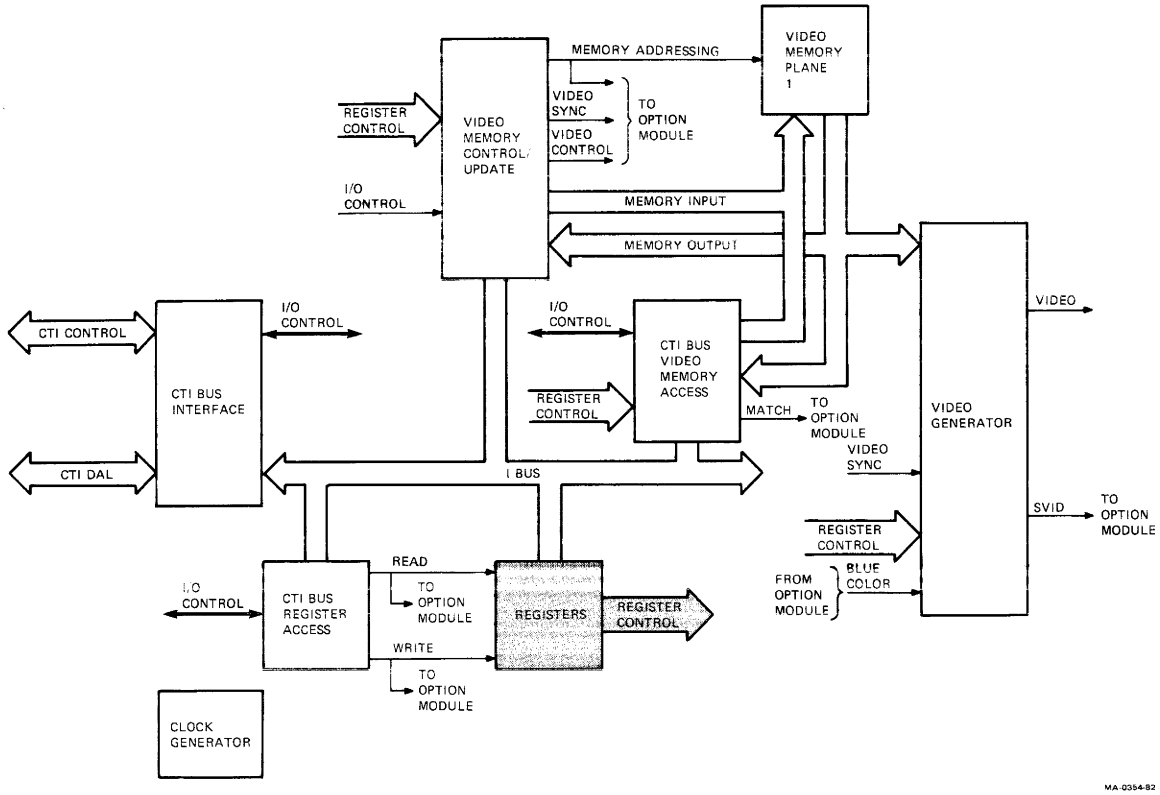


Figure 7-13 Counter Register Operation



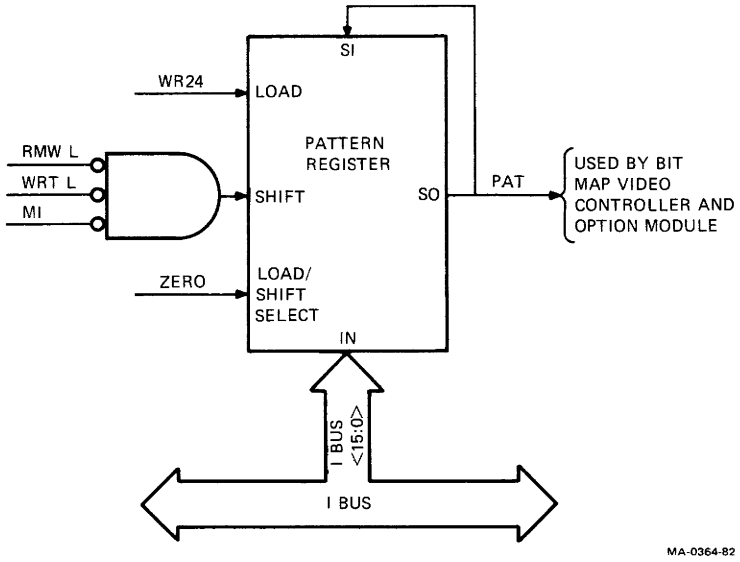
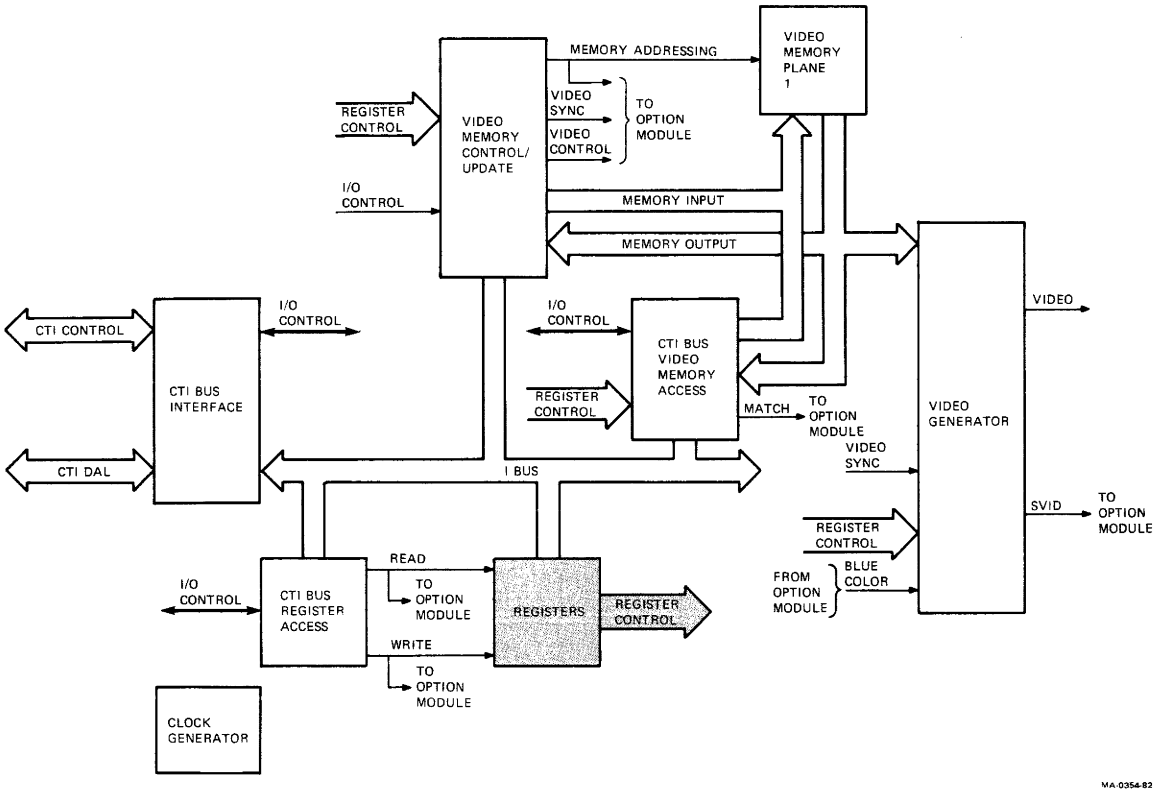


Figure 7-14 Pattern Register Operation



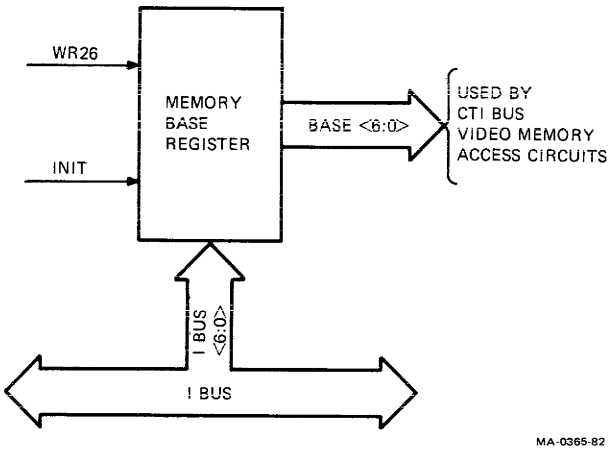
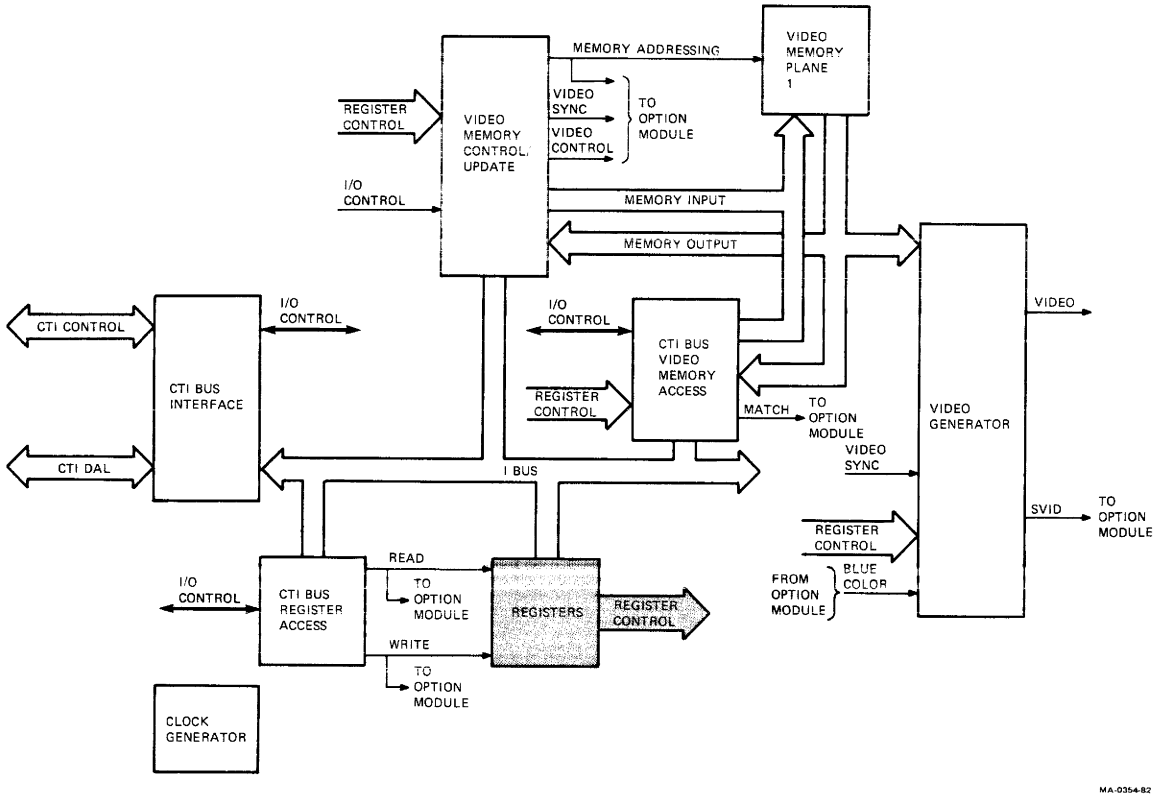


Figure 7-15 Memory Base Register Operation



7.3.1.4 CTI Bus Video Memory Access Circuits – The CTI Bus video memory access circuit (Figure 7-16) passes data between the internal bus and the video memory during host processor accesses to the video memory. To perform this function, this circuit uses the following components.

- Video memory address comparator
- CTI Bus video memory enable and reply buffer
- CTI Bus to video memory port
- Video memory to CTI Bus port

Video Memory Address Matching
To access the video memory, the host processor selects the video memory plane by accessing the plane 1 control register and setting the enable bit. Refer to Section 7.5 for the plane 1 control register definition. The video memory address comparator senses an enable video memory plane through the SELF and NO MEM signals.

The host processor then places a video memory address on the CTI Bus and asserts the I/O SEL signal. The I/O SEL enables the video memory address comparator to compare the 7-bit address in the base register to the seventh most significant bit (MSB) of the CTI Bus (I BUS <21:15>) on the module. If a match occurs, the ADRS STRB (generated by the host processor) latches the comparator to generate a MATCH signal. This signal indicates that host processor is accessing a video memory plane address.

Video Memory Data Transfers
After a video memory MATCH is established, the DATA STRB from the host processor clocks the CTI Bus video memory enable and reply buffer. This generates a memory enable signal (MEM). During a DATA STRB, a clock signal (D3) which synchronizes read-modify-write video memory accesses, asserts a memory reply signal (MREP) for the CTI Bus interface circuits.

During a host processor read cycle, the WRITE signal from the CTI Bus interface circuit and a video memory write enable signal (WRT) from the video memory control and update circuits remain unasserted. This enables the video memory to latch to a CTI Bus port when MREP, MEM, and SELF are asserted. When enabled, the addressed memory location data (MDO<15:0>) passes to the I BUS for the host processor.

During write cycles, the CTI Bus to video memory port passes data from the I BUS to the video memory data inputs (MDI>15:0>) when the memory enable signal (MEM) and the read-modify-write enable signal (D3) are asserted.

7.3.1.5 Clock Generator – The clock generator circuit (Figure 7-17) generates the required clock signals to synchronize all internal operations on the bit map video controller and the extended bit map modules. To perform this function, this circuit uses the following components.

20 MHz clock generator
Clock divider
High resolution clock generator

The 20 MHz clock generator provides three 20 MHz signals: CLKL, CLK1, and CLK2. Signal CLKL is sent to the extended bit map. Signals CLK1 and CLK2 are used by the bit map video controller.

The CLK1 signal is divided into a 10 MHz (D0), a 5 MHz (D1), and a 1.25 MHz (D3) signal. Signals D0, D1, and D3 are synchronized to the parallel enable (PE) signal from the video memory control and update circuits. This allows the clock signals to clock circuits at the desired intervals for every read-modify-write and read-only cycle.

The CLKL, CLK1, CLK2, D0, D1, and D3 are all 50% duty cycle clocks. The high resolution clock generator produces a 5 MHz clock (DX) with a 25% duty cycle for the video generator circuits on the bit map video controller and the extended bit map.

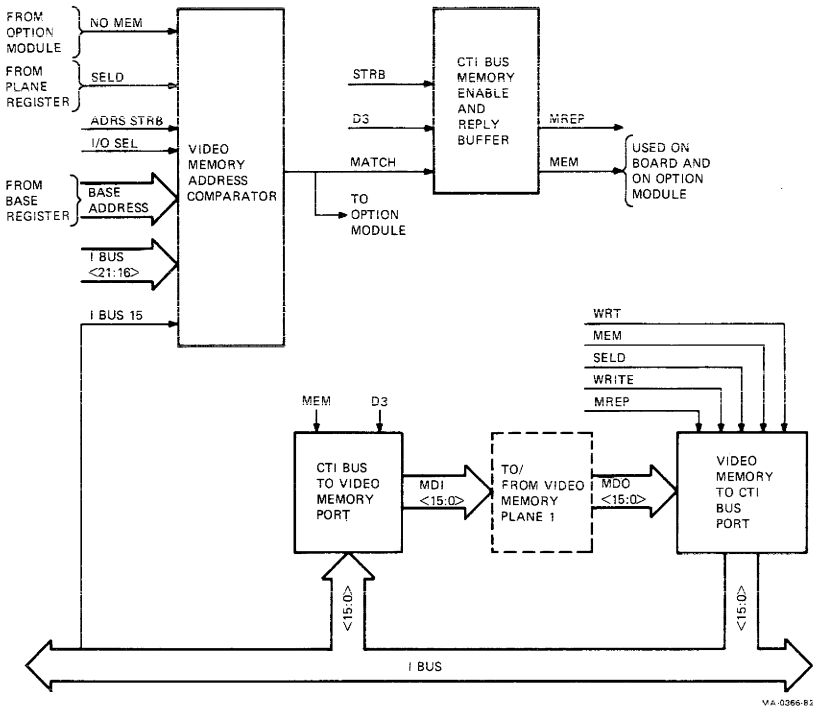
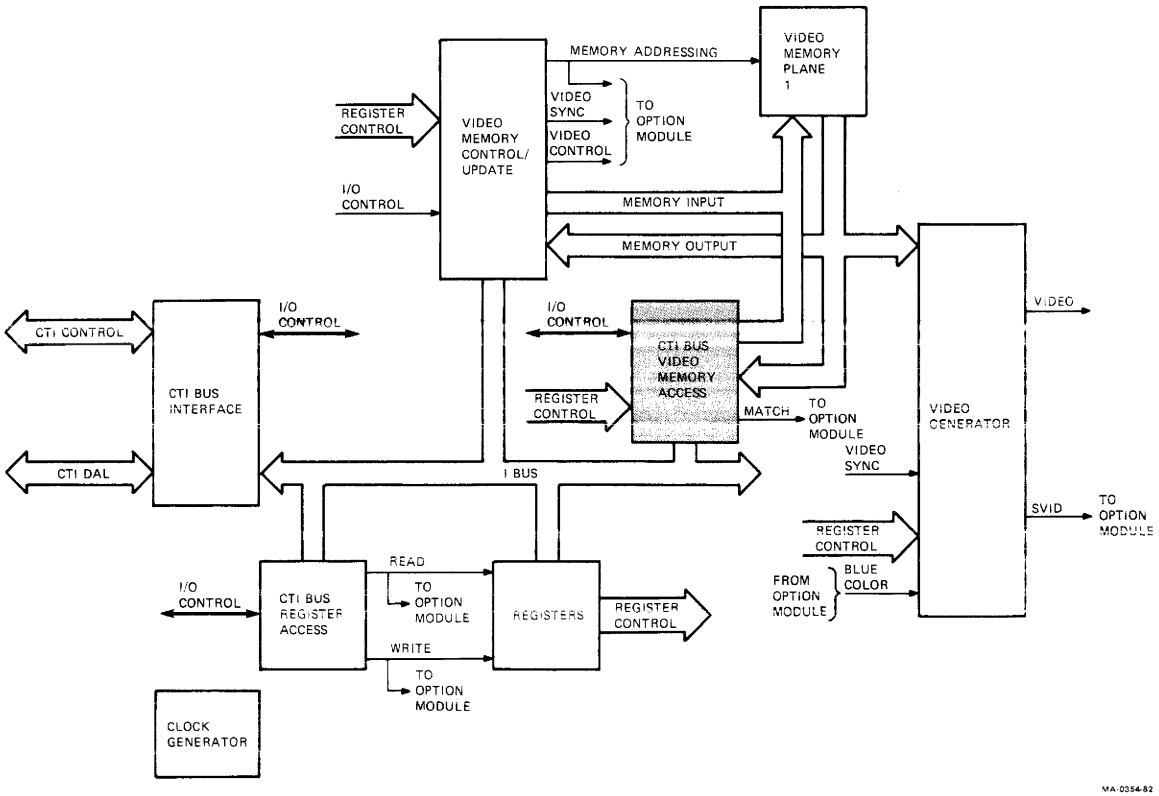


Figure 7-16 CTI Bus Video Memory Access Circuit Operation



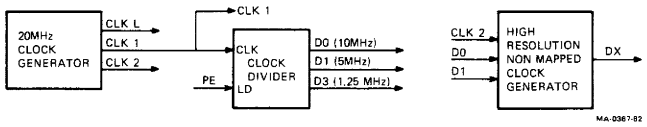
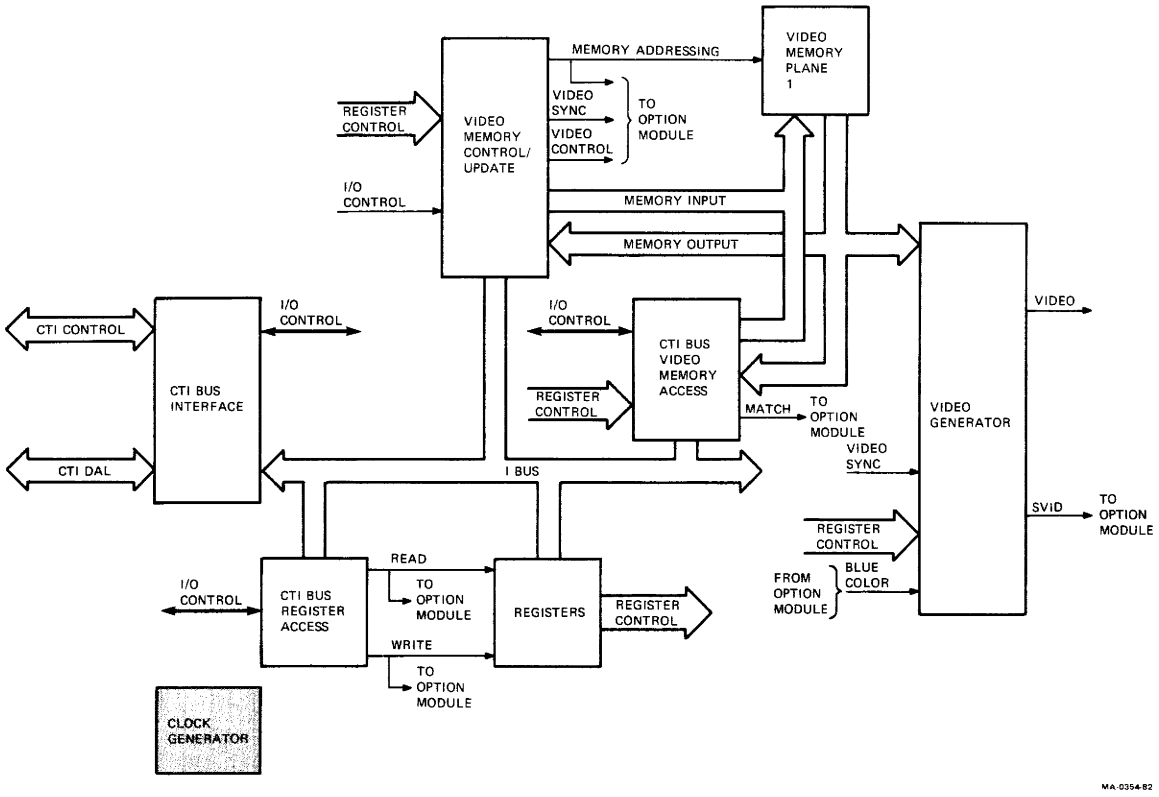


Figure 7-17 Clock Generator Circuit Operation



7.3.1.6 Video Memory Control and Update Circuit Operation – The video memory control and update circuits process commands from the host processor for both modules, control the generation of video signals for both modules, and update the video memory on the bit map video controller (Figure 7-18). To perform this function, this circuit uses the following components.

Video processor chip (DC717)
Video controller chip (DC715)
Synchronization buffer
Memory write enable buffer
Video data modification chip (DC716)

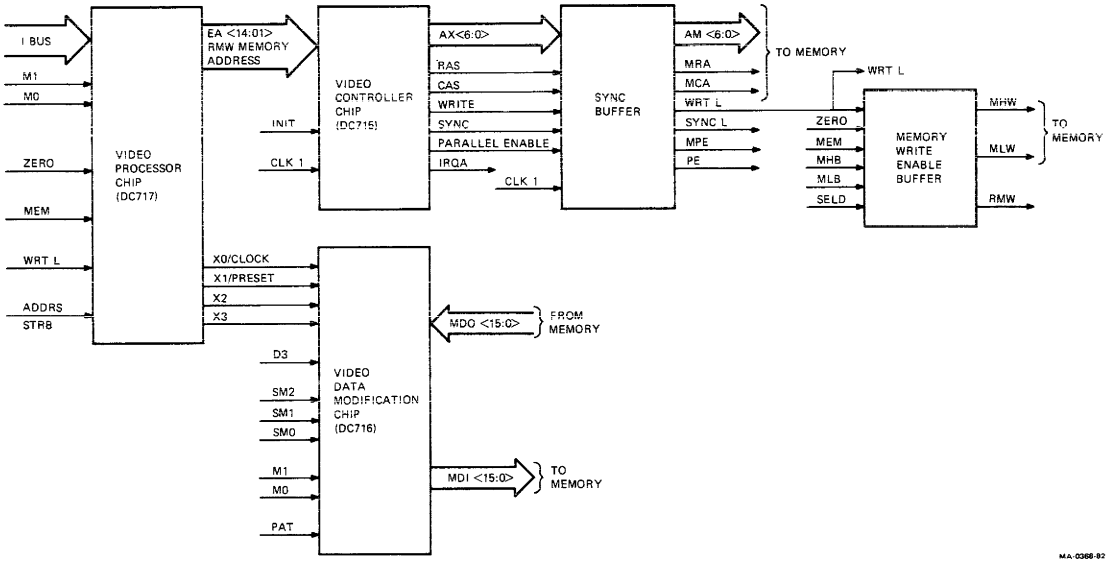
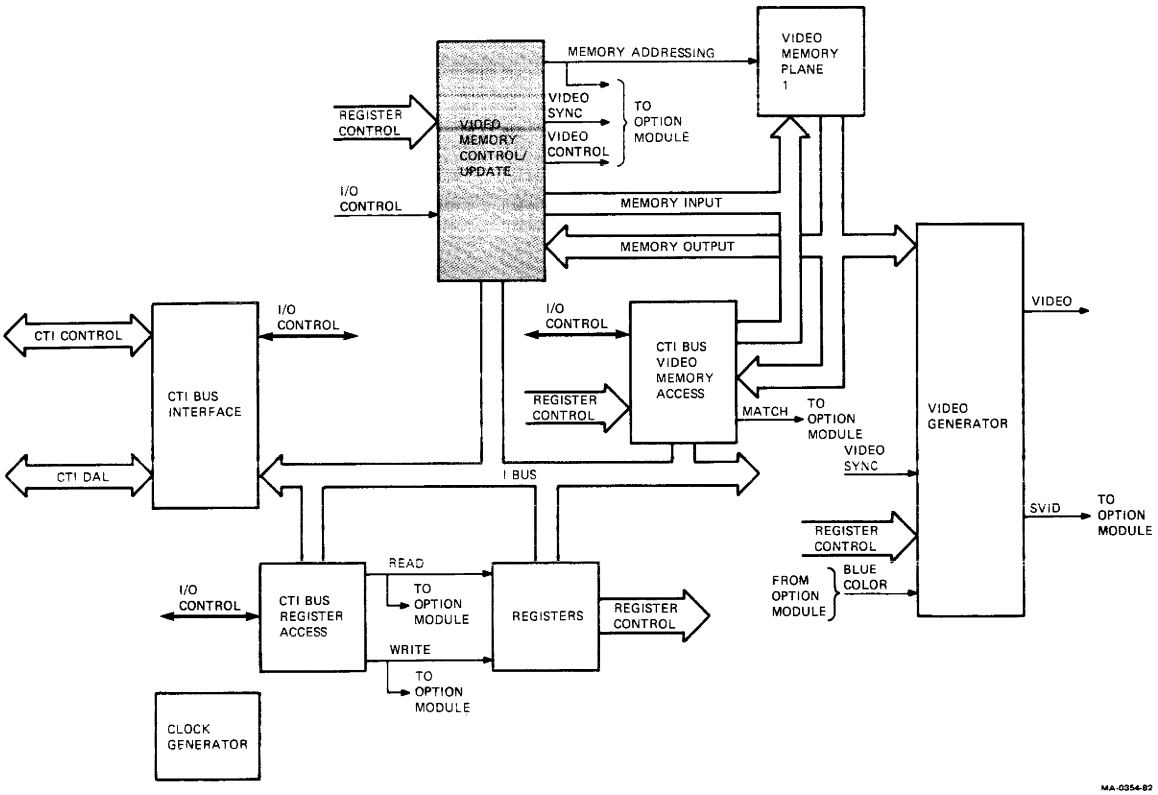


Figure 7-18 Video Memory Control and Update Circuit Operation



Video Processor Chip (DC717) Operation

The video processor chip is a 48-pin-low power schottky-type gate array integrated circuit. This chip controls all read-modify-write cycles for the video memories. Two types of read-modify-write cycles can occur for the video memories: a host processor access read-modify-write cycle or a video processor read-modify-write cycle.

For a host processor read-modify-write cycle, a 14-bit address of the desired memory location is loaded into the video processor chip from the I BUS by an asserted ADDR STRB signal. The memory enable signal (MEM) from the CTI Bus video memory access circuits cause the chip to send the address to the video controller chip on the EA<14:01>lines.

For a video processor read-modify-write cycle, the X coordinate register, Y coordinate register, CSR, and counter register control the 14-bit address the chip provides to the video controller. The X and Y coordinate registers are internal to the video processor chip and the CSR and counter registers are discrete. See Section 7.3.1.3 for further information about registers.

The four least significant bits (LSBs) of the X coordinate register define the bit to be modified within the word and are sent to the video data modification chip. These same lines are multiplexed with the timing signals, CLOCK and PRESET, for the video data modification chip.

The video processor chip also contains control logic. The control logic controls the X and Y coordinate registers, the multiplexing of the read-modify-write address, and multiplexing of the bit in the word with the timing signals. This control logic receives M0, M1, ZERO, MEM, and WRT. Table 7-3 lists the operations the video processor chip performs when these signals are enabled.

In bit mode (M1 low), the X0 through X3 bits are the X coordinate register's least significant bit outputs to the video data modification chip. In word mode (M1 high), CLOCK is the WRT L buffered, and PRESET indicates an underflow or overflow of the most significant bit from the X coordinate register.

Table 7-3 Video Processor Chip Operation Mode Selection

Signal	Description
MEM	If present, this signal selects a host processor read-modify-write cycle for the video memory and disables the X and Y coordinate registers. If not present, a video processor read-modify-write cycle is selected and the X and Y coordinate registers are selected.
ZERO	Counter register ZERO disables the X and Y coordinate registers to count and enables the registers to be loaded.
WRT L	The clock signal for the X and Y cooordinate registers to increment or decrement.
M1 and M0	These 2 bits from the CSR indicate a X and Y coordinate register mode as follows.

M1	M0	Operations
0	0	Bits shifted left to right
0	1	Bits shifted top to bottom
1	0	Words shifted left to right
1	1	Words shifted right to left

Video Controller Chip (DC715) Operation

The video controller chip is a 48-pin low power schottky-type gate array integrated circuit manufactured by Digital. The chip controls all memory and video timing, generates screen refresh addresses, and controls vertical scroll.

For memory timing, this chip divides the 20 MHz system clock (CLK1) by 16 (800 ns). The 800 ns clock represents two memory cycles, one read-modify-write cycle for modifying memory data and one read-only cycle for screen refresh. The chip also generates the RAS and CAS signals and time multiplexes the 14-bit video memory address for both memory cycles into a 7-bit multiplexed address bus (AX<6:0>) for the synchronization buffer.

For video timing, the CSR controls this chip to generate horizontal, vertical, and video sync signals. The CSR programs horizontal and vertical counters internal to the chip to provide 50 or 60 Hz operation and interlaced or noninterlaced operation. These counters also coordinate the video memories addressing for the screen refresh cycles.

The 6 least significant bits of the horizontal counter form the 6 least significant bits of the screen refresh address (word within line). The 8 least significant bits of the vertical counter form the 8 most significant bits of the screen refresh address.

The chip contains a multiplexer to switch between the external address (EA01–EA14) for read-modify-write cycles generated by the video processor chip, and the internally generated read-only addresses for screen refresh cycles. The memory timing clock controls this multiplexer. During the first half of every 800 ns display cycle, the multiplexer selects the external address. During the second half of the cycle, the multiplexer selects the internal address.

The video controller chip contains the scroll register. This register's contents are always added to the 8 most significant bits of the selected memory address. This operation modifies all addresses to the video memory. This moves all information in memory and causes a vertical scroll.

Table 7-4 describes the signals generated by the video controller chip for the synchronization buffer.

Table 7-4 Video Controller Chip Output Signal Definitions

Signal	Description
AX<6:0>	The time multiplexed RAS/CAS address bus for dynamic RAM devices
RAS	Row address select for video memory control
CAS	Column address select for video memory control
WRITE	WRITE pulse for video memory control
PE	A parallel enable signal is generated to parallel load the video shift register in the video generator with memory data. It is only generated during the active portion of the video timing (64 times per line during 256 lines in 625 line mode or 240 lines in 525 line mode).
SYNC	This signal contains the complete video sync signal with horizontal sync, vertical sync, and equalization pulses.
IRQA	When enabled by the CSR, this signal is the vertical retrace interrupt request for the host processor.

Video Memory Address and Video Control Synchronization
The video control chip generates the video memory address and video control signals. These signals are synchronized by the synchronization buffer and the memory write enable buffer. This allows all signals to switch on the 20 MHz system clock edges. The video memory address AX<6:0> becomes AM<6:0>. The row and column address strobes RAS and CAS become MRA and MCA. The write strobe for video processor cycles becomes WRT L. The video sync signal for the video generator circuits becomes SYNC L. The parallel enable signal goes to the video generator circuits as MPE and to the clock generator circuits as PE.

Two more signals are provided for write operations to the video memory: the memory high byte write (MHW) and memory write low byte (MLW). These signals are generated for both host processor to video memory accesses and video processor to video memory accesses. For a host processor cycle, the ZERO, MEM, and SELD enable the buffer while the CTI Bus interface circuit signals WHB and WLB select MHW and MLW respectively. For a video processor cycle, the synchronized WRT L signal generates both MHW and MLW and a RMW signal to indicate a video processor read-modify-write cycle.

Video Data Modification Chip (DC716) Operation
The video data modification chip is a 48-pin low power schottky-type gate array integrated circuit. This chip performs the data modification to the bit map video controllers video memory during video processor controlled read-modify-write cycles.

This chip receives control signals from the video processor chip and register control signals from the CSR, plane control, and pattern registers. These signals control the video data modification chip to modify the data stored in the video memory. Table 7-5 describes the video data modification chip operation selection.

Refer to Section 7.5 for further information on video processor logical operations.

Table 7-5 Video Data Modification Chip Operation Selection

Signal	Function
X3–X0	In bit mode, these four inputs specify the bit to be modified within the addressed word.
CLOCK/PRESET	In word mode, these two signals control shift operations.
M1–M0	These signals specify the bit and word operation modes.
SM2–SM0	These submode signals specify the logical operation to be performed by the chip.
PAT	The least significant bit of the pattern register can be used as data for the logical operations.
D3	A timing signal that controls the memory data inputs and outputs.
RMW	This read-modify-write signal enables the chip to perform a logical operation.

7.3.1.7 Video Memory Circuit Operation – The video memory is an array of 16 (16K × 1-bit) dynamic RAMs (Figure 7-19). The video memory control and update circuit address these RAMs for all read-modify-write operations and read-only operations. Memory input data (MDI<15:0>) comes from the video memory control and update circuits or the CTI Bus to video memory access circuits. Memory output data (MDO<15:0>) goes to the video memory control and update circuits, the CTI Bus to video memory access circuits or the video generator circuits.

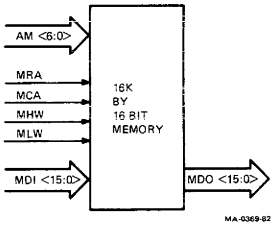
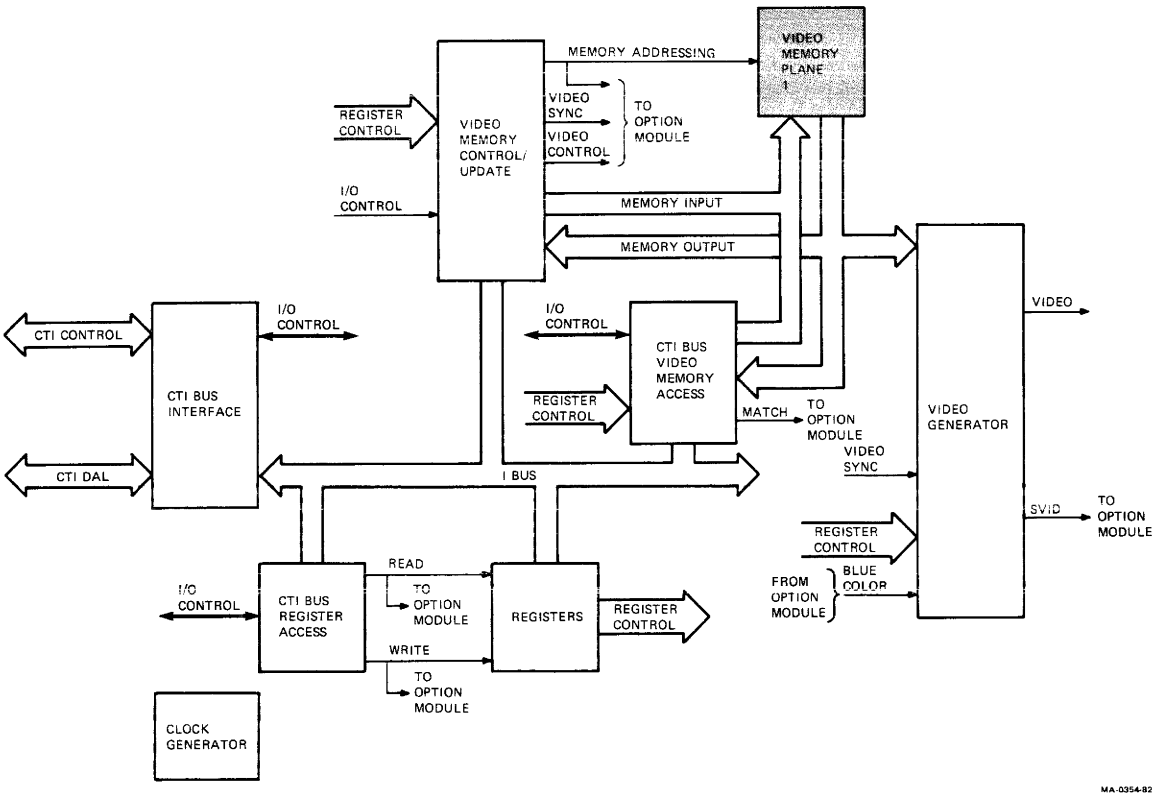


Figure 7-19 Video Memory Circuit Operation



7.3.1.8 Video Generator Circuit Operation – The video generator circuit (Figure 7-20) assembles the video data and sync pulses, then amplfies them for transmission over the CTI private Bus to the monitor. To perform this function, this circuit uses the following components.

Parallel-to-serial converter
Serial shift buffer
Nonmapped resolution decoder
Nonmapped video sync buffer
Mapped video sync buffer
Video drivers

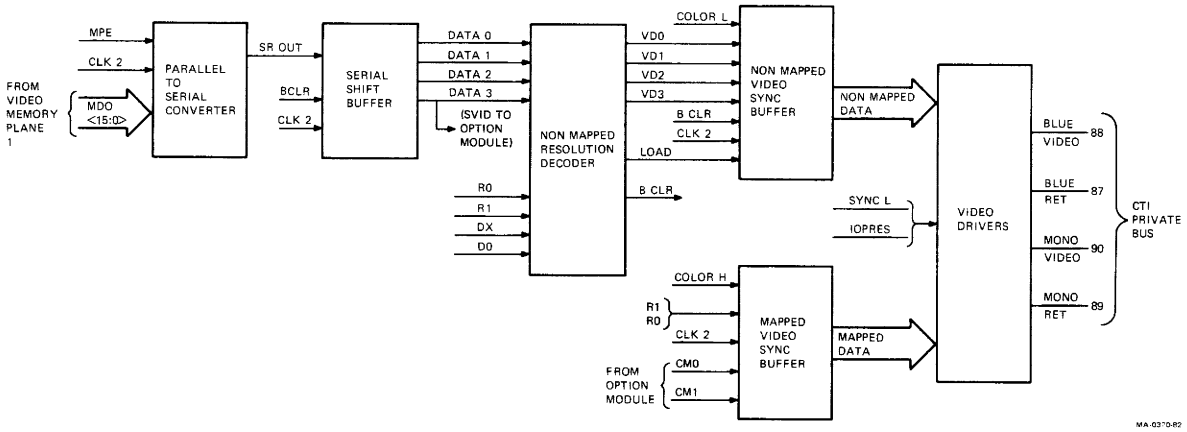
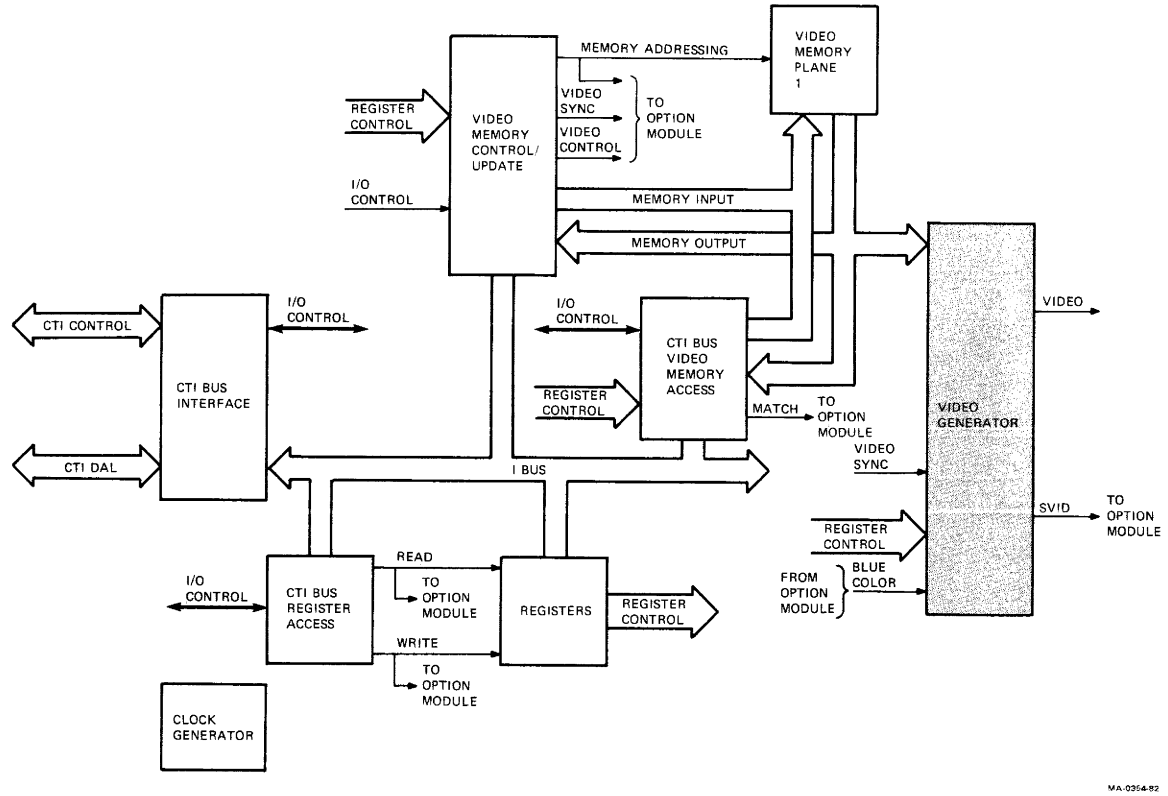


Figure 7-20 Video Generator Circuit Operation



The video generator operates in two modes: nonmapped or mapped. The COLOR signal, from the plane register, selects the operation for either mode. All circuits necessary for single plane nonmapped mode video signal generation (monochrome monitor only) are on the bit map video controller. For mapped mode operation, these circuits serialize the video memory data and pass it to the extended bit map module. The external bit map returns blue video data (CM1 and CM0) and generates a BLUE VIDEO signal and a MONO VIDEO signal.

Nonmapped Video Signal Generation

During a read-only operation, the parallel enable signal (MPE) from the video memory control and update circuit enables the parallel-to-serial converter to load a data word from the video memory. The 20 MHz clock (CLK2) shifts the data (SROUT) to the serial shift buffer. The video memory control and update circuits have complete control over the converter. These circuits control the loading and shifting of the data to a serial format for lines and disable data loading during vertical and horizontal retraces.

The serial shift buffer provides the serial data to the nonmapped resolution decoder in three forms: single-bit at a 20 MHz rate (D0), dual-bit at 10 MHz rate (D0 and D1), and quad-bit at a 5 MHz rate (DATA 0 through DATA 3).

The nonmapped resolution decoder receives the resolution selection signals (R1 and R0) from the plane 1 control register and clock signals (D0 and DX) from the clock generator. The R1 and R0 signals select one of four modes of operation: single-bit resolution, dual-bit resolution, quad-bit resolution, or a blank screen. Table 7-6 shows which data bits are provided to the nonmapped video sync buffer as video data and how the different resolution modes are selected.

The video data is synchronized with the CLK2 signal by the nonmapped video sync buffer and passed to the video drivers. The drivers amplify the video data and the sync pulse from the video memory control and update circuits and pass the composite video signal to the CTI private Bus as MONO VIDEO. Figure 7-21 shows the three types of composite video signals the video generator produces during nonmapped operation.

Table 7-6 Nonmapped Resolution Mode Operation

R1	R0	Load	VD3	VD2	VD1	VD0	DUTY	BCLR L
0	0	0	Data 0	Data 0	0	0	50 ns	1
0	1	DO	Data 1	Data 0	0	0	100 ns	1
1	0	DX	Data 3	Data 2	Data 1	Data 0	200 ns	1
1	1	0	0	0	0	0	none	0

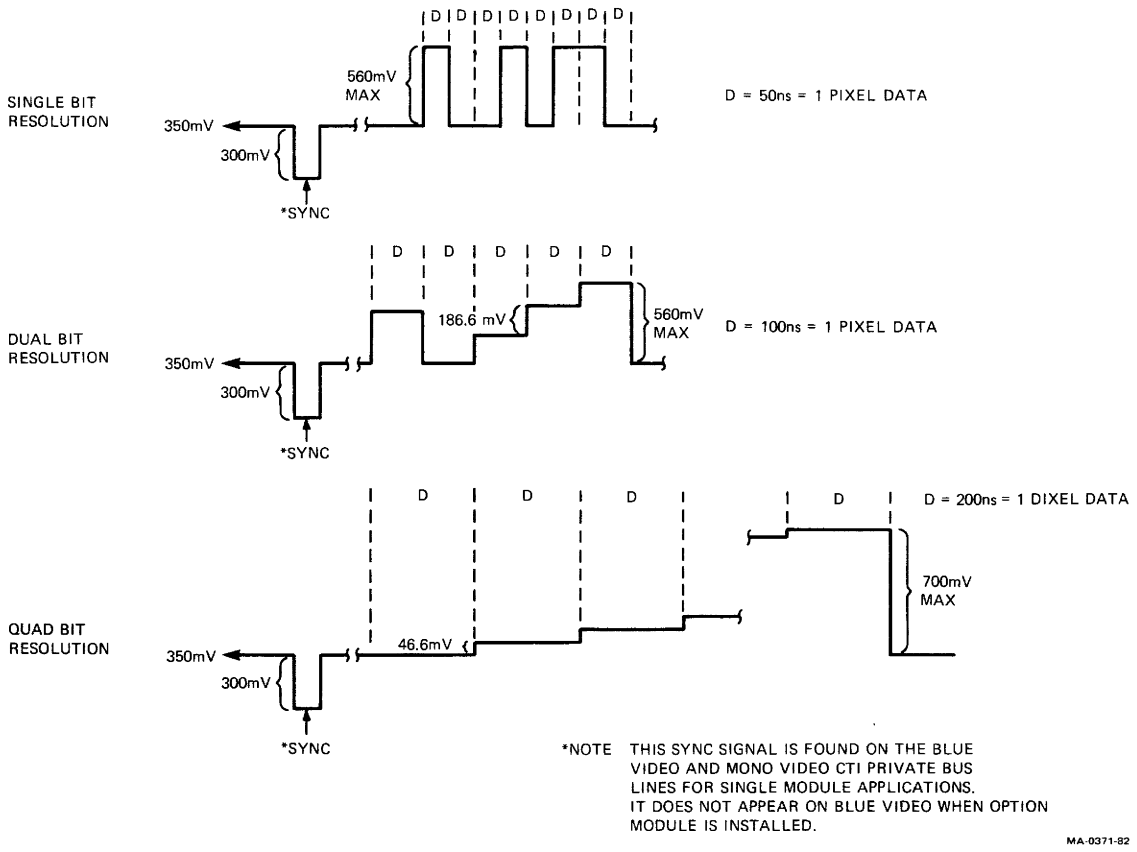


Figure 7-21 Nonmapped Video Signal Characteristics

Mapped Video Signal Generation

During a read-only operation, the parallel enable signal (MPE) from the video memory control and update circuit enables the parallel-to-serial converter to load a data word from the video memory. The 20 MHz clock (CLK2) shifts the data (SROUT) to the serial shift buffer. The video memory control and update circuits have complete control over the converter. These circuits control the loading and shifting of the data to a serial format. The converter is not loaded during vertical and horizontal retraces.

The serial shift buffer delays the serial data by 200 ns and then sends it to the extended bit map (DATA 3 – SVID). The extended bit map returns two serial data bits (CM1 and CM0) to the mapped video sync buffer. This buffer is clocked by the 20 MHz system clock (CLK2) to synchronize the data at the video drivers' inputs. If one of the resolution bits (R1 and R0) is a 0, the mapped video sync buffer is enabled. If both resolution bits are a 1, the mapped video sync buffer is disabled.

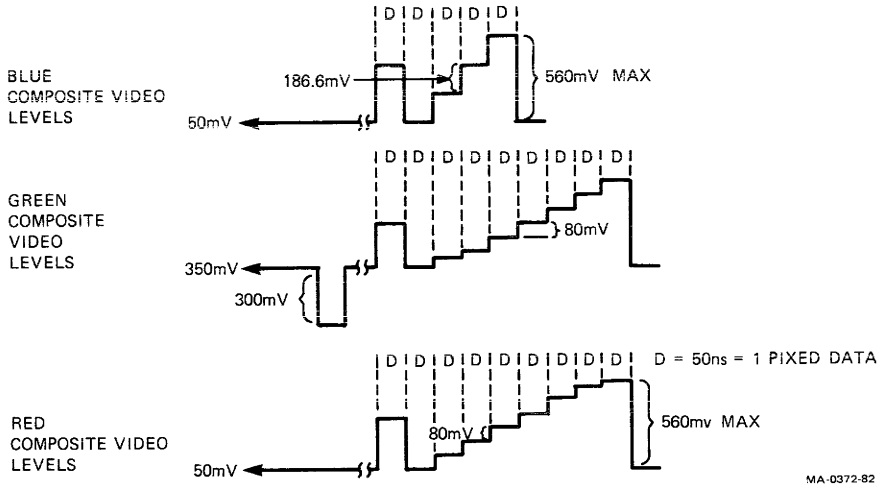


Figure 7-22 Mapped Video Signal Characteristics

The video drivers amplify the color video data from the video memory control and update circuits. The drivers then pass BLUE VIDEO and MONO VIDEO signals to the CTI private Bus. The video generator produces the video signal (Figure 7-22) during mapped operations.

NOTE

When the extended bit map module is not in the video subsystem, the plane 1 video generator amplifies the SYNC signal. The signal appears on the BLUE VIDEO line and the MONO VIDEO line. When the extended bit map module is in the video subsystem, the plane 2 video generator on the extended bit map amplifies the SYNC signal. This signal appears on the GREEN VIDEO line and the MONO VIDEO line.

7.3.2 Extended Bit Map Module Detailed Operation

The extended bit map is an optional module when used to provide alternate display planes for monochrome monitors. It is required for color monitors for to provide the required data storage and red and green video signals. To perform these functions, the module uses the following circuits.

CTI Bus interface
Plane and color map registers
Two CTI Bus video memory access circuits
Two video memory update circuits
Two video memory planes
Two video generators

7.3.2.1 CTI Bus Interface Circuit Operation – The CTI Bus interface circuit for the extended bit map module (Figure 7-23) passes data between the CTI Bus and the internal bus (I Bus) for direct and indirect accesses. To perform this function, this circuit uses the following components.

CTI Bus control signal buffer
Memory plane access decoder
CTI Bus data/address transceivers
Identification buffer

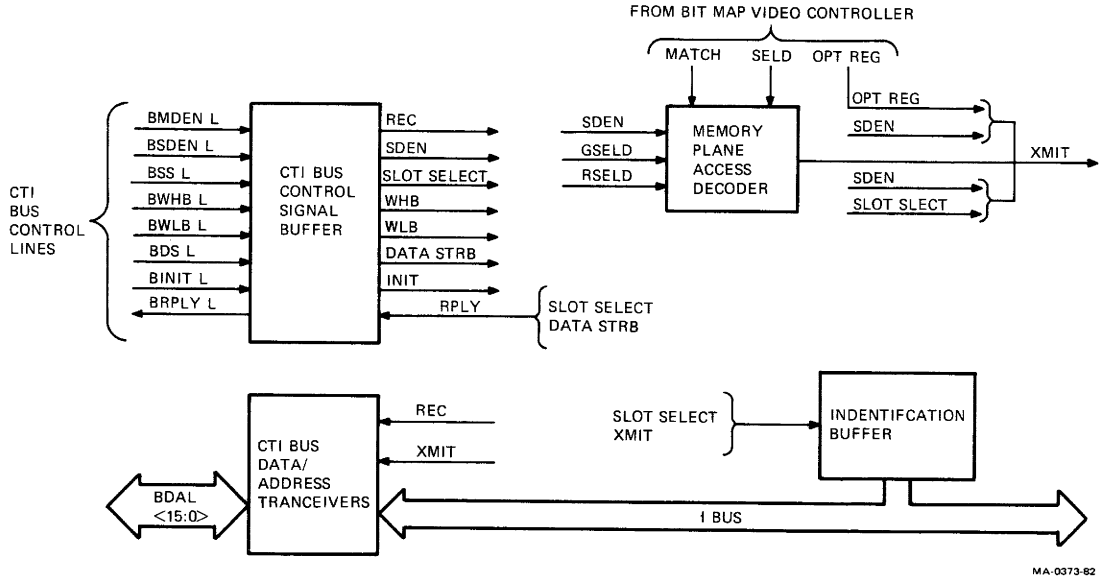
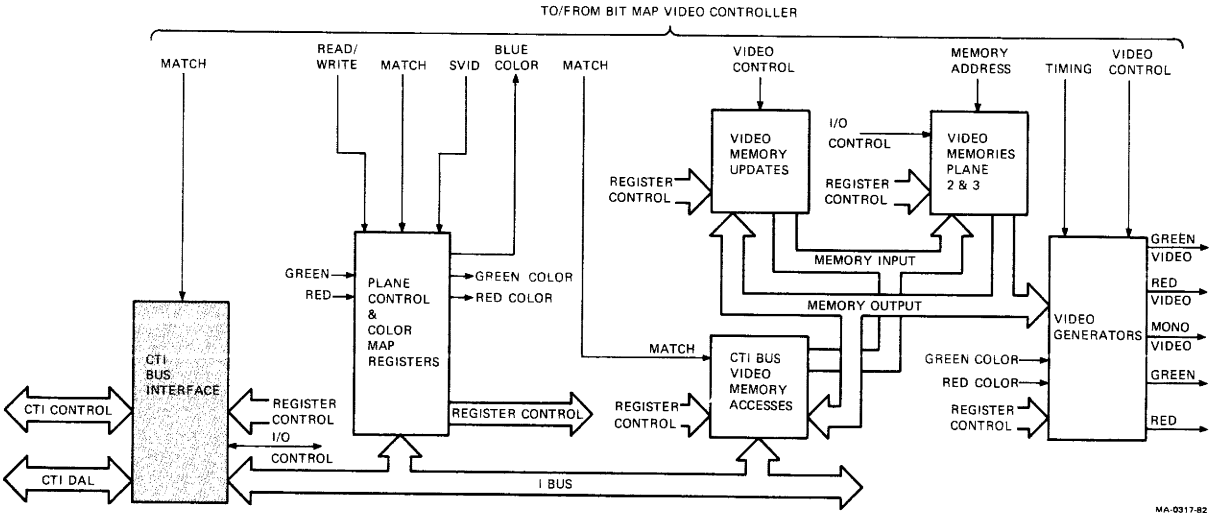


Figure 7-23 CTI Bus Interfaced Circuit Operation (Option Module)



Direct Extended Bit Map Module Accessing
The extended bit map module responds to direct host processor read accesses with the module identification code. Host processor write accesses to the module have no affect on the module operation. For direct accesses to the module, the host processor asserts the slave device enable signal (B SDEN L) and the slot select signal (BSS L) to the CTI Bus control signal buffer. These signals generate a module transmit signal (XMIT) and an enable identification buffer signal (ENAID). These signals simultaneously enable the identification buffer and CTI Bus data/address transceivers. This allows the buffer to pass the module's identification code over the I Bus to the CTI Bus BDAL lines to the host processor.

The module also generates an acknowledgement signal (REPLY) for the host processor. It is generated when the CTI Bus DATA STRB is asserted with the SLOT SELECT signal.

Indirect Extended Bit Map Module Accessing
For indirect extended bit map module accessing, the host processor does not assert the SLOT SELECT signal. A buffered B MDEN L signal (REC) passes data from the host processor to the modules internal bus (I Bus). This signal enables the CTI Bus data/address transceivers to pass data on the BDAL lines to the internal bus (I Bus). Data is passed from the internal bus to the host processor in two modes: register access or video memory access.

During a read access to the extended bit map module registers, a transmit (XMIT) signal is generated for the CTI Bus data/address transceivers. An option register access signal (OPT REG) from the bit map video controller enables the slave device enable signal (SDEN) to generate a XMIT signal. The data is then passed over the I Bus from the registers to the CTI Bus.

During a read access to the extended bit map's video memory, the memory plane access decoder generates the XMIT signal for the CTI Bus data/address transceivers. A MATCH signal from the bit map video controller enables the decoder. This indicates that the host processor accessed an address in the assigned 16K word (32 kilobyte) video memory plane range. The slave device enable signal generates an XMIT signal during the following conditions.

1. The video memory plane on the bit map video controller is not enabled (SELD unasserted).

2. One of the video memory planes on the extended bit map is enabled (GSELD or RSELD is asserted).

7.3.2.2 Plane 2 and 3 Control and Color Map Register Operation – The plane 2 and 3 control and color map registers (Figure 7-24) are written or read to with data from the module's internal bus, under control of the bit map video controller. The plane 2 and 3 control register selects the operational mode of the video memory update circuits for the plane 2 (green) and plane 3 (red) video memories, and the plane 2 (green) and plane 3 (red) video generators on the extended bit map. The color map register controls the generation of the color composite video signals during mapped operations.

Plane 2 and 3 Control Register
The plane 2 and 3 control register is read or written to under control of the bit map video controller. A write strobe (WR10) loads data from the internal bus (I Bus) into the register. A read strobe (RD10) places the register contents on the internal bus. Refer to Section 7.3.2.1 for further information on host processor-to-module and module-to-host processor transfers.

A CTI Bus initialization signal (INIT), passed to the module by the CTI Bus interface circuits, resets the plane 2 and 3 control register contents. This ensures that no video memory plane is selected or enabled after an initialization.

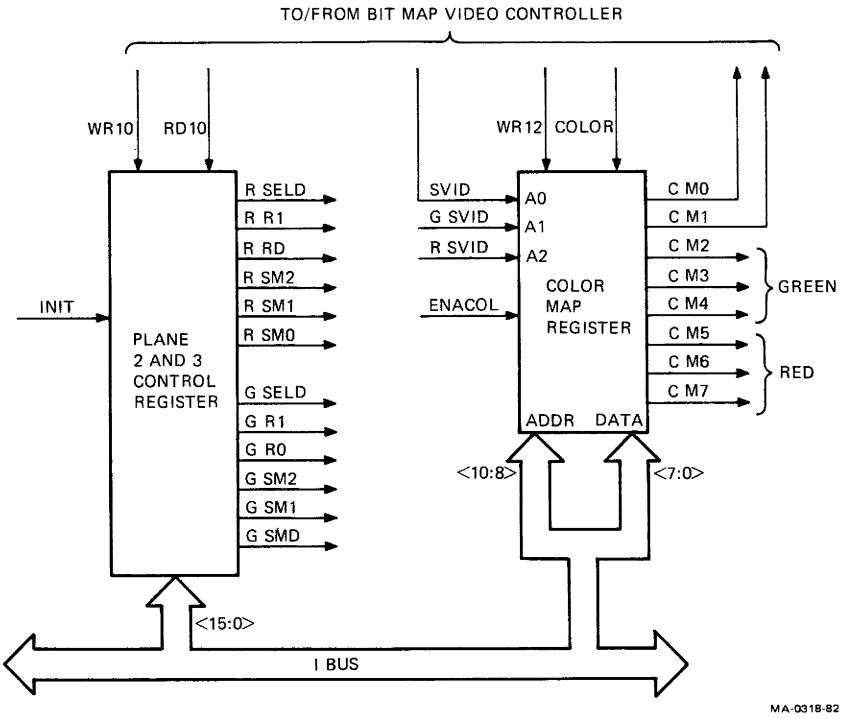
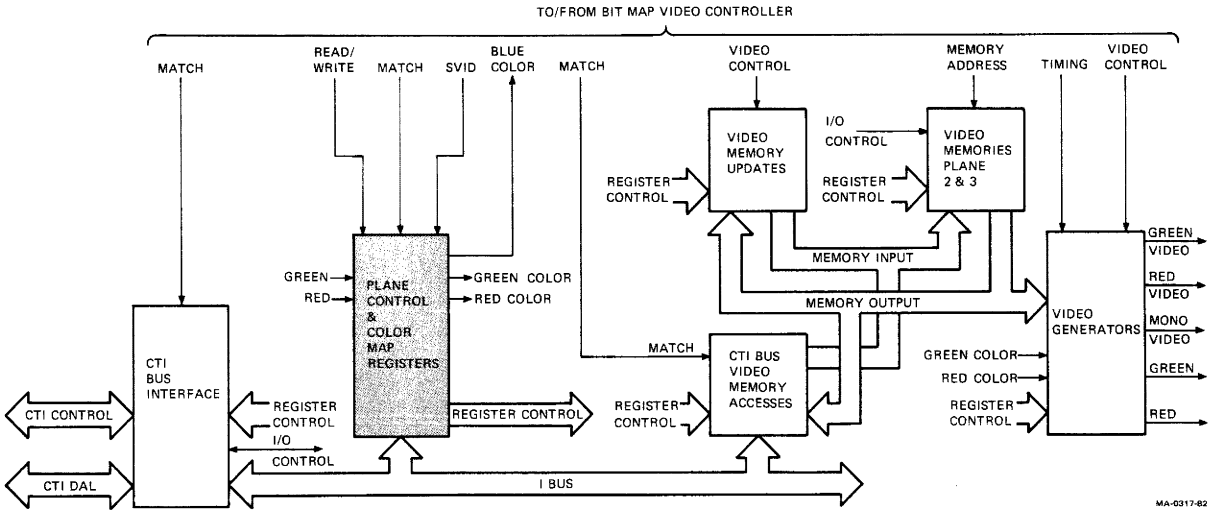


Figure 7-24 Plane 2 and 3 Control and Color Map Register Operation (Option Module)



Color Map Register Operation
During mapped operations, the color map register (CMR) provides data for the generation of composite video signals. This register is an eight word × 8-bit memory. Each word is preloaded with a value which controls each of the three video generators on both modules to generate a composite video signal. There are eight (out of 256) preselected combinations that the video subsystem can generate on a color or monochrome monitor.

The bit map video controller loads the CMR (WR12 asserted) from the internal bus (I Bus). The low byte on the I Bus (I<7:0>) is the data word. The upper three bits (I<10:8>) define the address the data word is loaded into. This procedure is performed to define the eight combinations the subsystem will generate for an application.

After the CMR is loaded, serial video data from the three video generators on both modules form a 3-bit address for the color map register. The serial data from the plane 1 video generator is A0, the serial data from the plane 2 video generator plane is A1, and the serial data from the plane 3 video generator is A2.

The addressed 8-bit word is split up with certain bits passed back to each video generator. The bits select composite video signal levels which each video generator produces. For the plane 1 video generator, CM0 and CM1 select one of four levels; for the plane 2 video generator, CM2, CM3, and CM4 select one of eight levels; for the plane 3 video generator, CM5, CM6, and CM7 select one of eight levels.

The COLOR signal from the bit map video controller enables the color map register to operate and puts the video subsystem in the mapped operation mode.

The ENACOL signal is a 51 μs disable signal to blank the color map register output during horizontal and vertical screen retraces.

7.3.2.3 CTI Bus Video Memory Access Circuit Operation – The extended bit map contains two CTI Bus to video memory access circuits, one for each video memory plane. Figure 7-25 shows the operation of both pairs of circuits. To pass data between the host processor and each video memory, these circuits use the following components.

Video memory plane access control circuit
Plane 2 (green) video memory plane output port
Plane 3 (red) video memory plane output port
Plane 2 (green) video memory plane input port
Plane 3 (red) video memory plane input port

Each port is controlled by the video memory plane access control circuit. This circuit is controlled by signals generated by the bit map video controller. The operation and function of this circuit is similar to the CTI Bus video memory access circuits on the bit map video controller. See Section 7.3.1.4 for further information.

7.3.2.4 Video Data Update Circuit Operation – The extended bit map contains two video data update circuits, one for each video memory plane. Figure 7-26 shows the circuits for both pairs of circuits. To update each video memory two video data modification chips use common control signals from the bit map video controller module but separate sub mode signals (SM2–SM0) from the plane 2 and 3 control register. The operation of these chips is similiar to the video data modification chip described in Section 7.3.1.6.

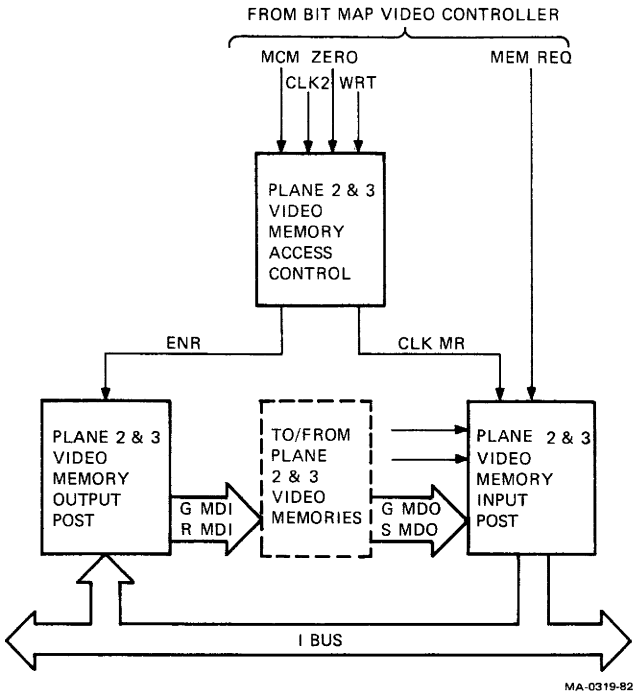
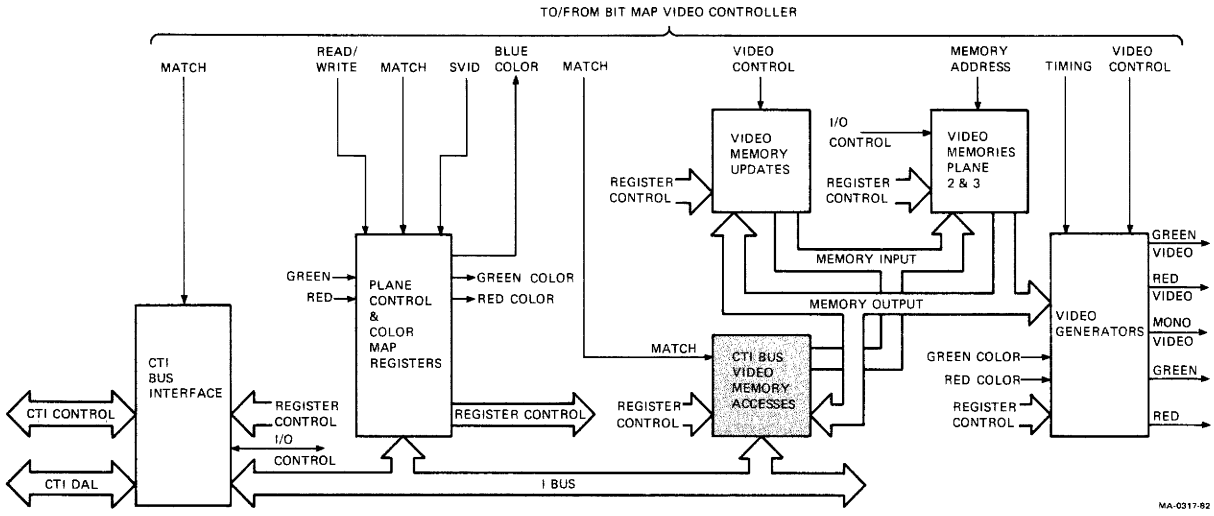


Figure 7-25 CTI Bus Video Memory (Plane 2 and 3) Access Circuits Operation (Option Module)



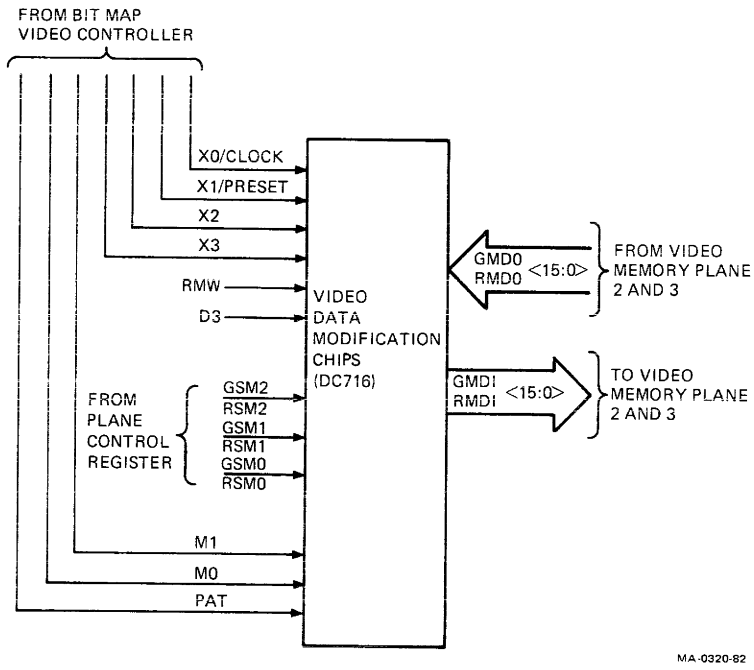
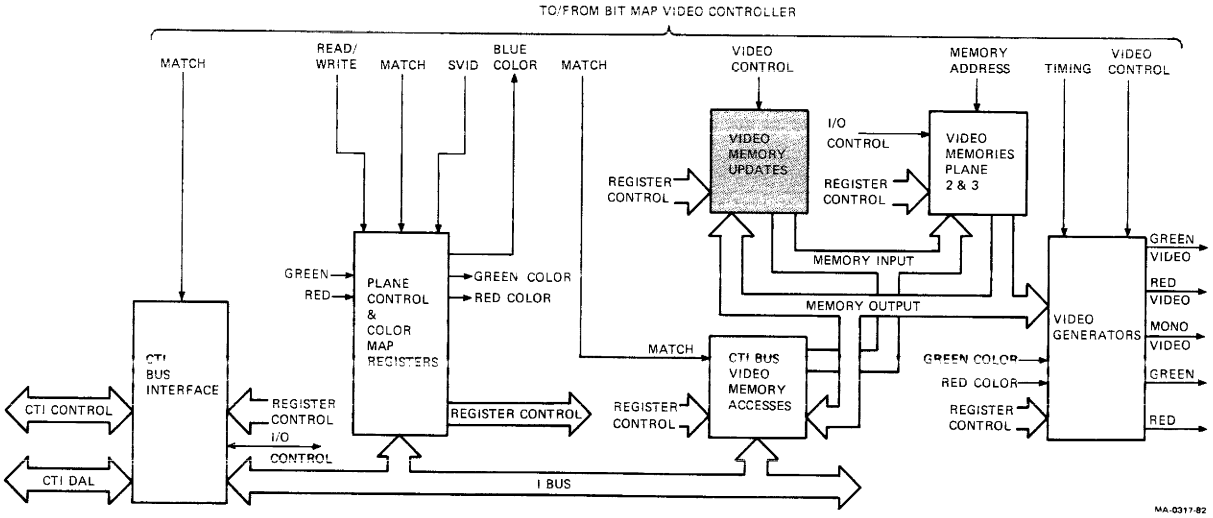


Figure 7-26 Video Data Update Circuit Operation (Option Module)



7.3.2.5 Video Memory Plane 2 and 3 Circuit Operation – The extended bit map contains two video memory planes, one for each video generator. Figure 7-27 shows the circuits for both planes. Each video memory plane is a 16K × 16-bit (32K byte) memory with a write control circuit. Both video memories are addressed by common address signals from the bit map video controller module. The write control circuits generate a memory high write (MHW) strobe and a memory low write (MLW) strobe by control signals it receives from the CTI Bus or the bit map video controller. Before these signals are generated, the write control circuit must be enabled by the plane 2 and 3 control register (GSELD or RSELD) and the read-modify-write (RMW) signal. The operation of these video memory planes is similiar to the operation of the video memory on the bit map video controller.

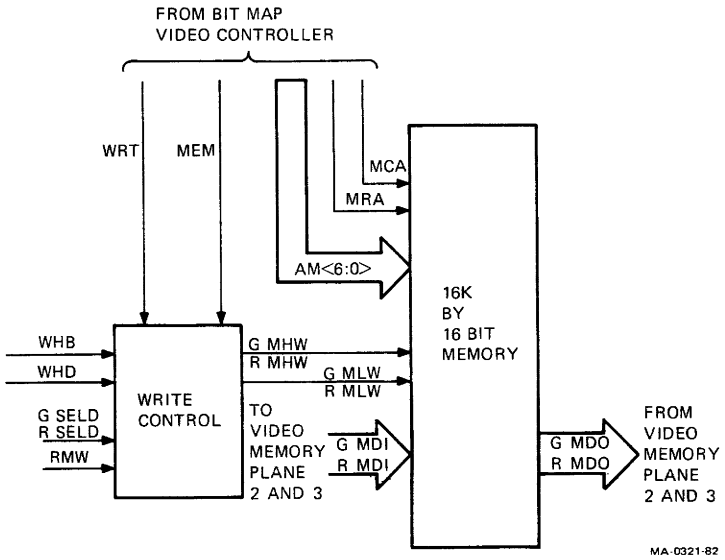
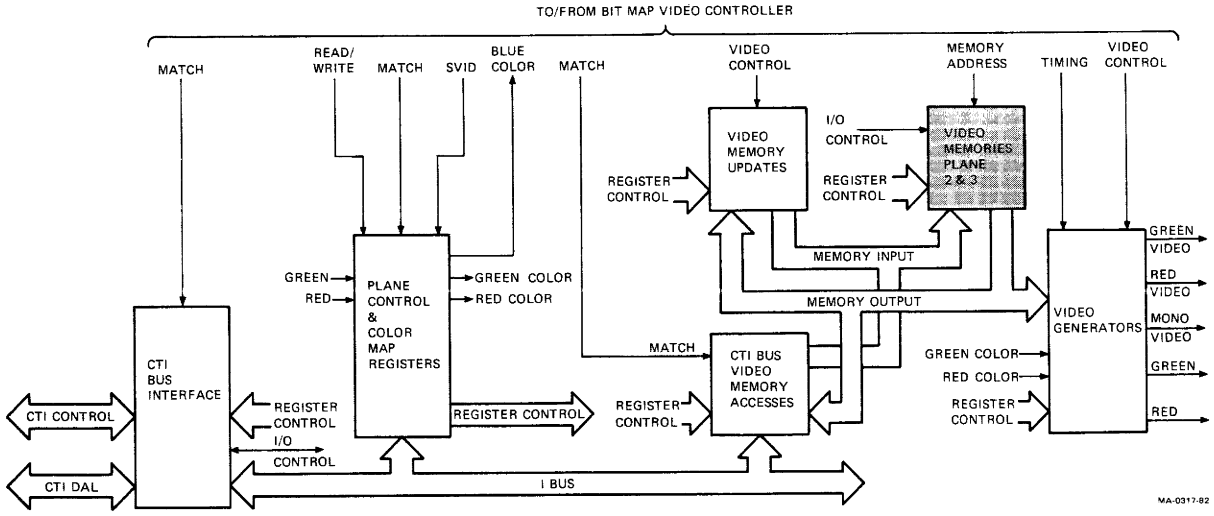


Figure 7-27 Video Memory (Plane 2 and 3) Circuit Operation (Option Module)



7.3.2.6 Video Generators Circuit Operation – The extended bit map contains two video generator circuits, one for each video memory plane. Figure 7-28 shows the circuits for both pairs of circuits. These circuits generate MONO VIDEO signals which electrically connect to the MONO VIDEO signal generated by the bit map video controller. These circuits also generate composite GREEN VIDEO and RED VIDEO signals.

Each circuit receives common clocks, select, and synchronization signals from the bit map video controller module. Each circuit also receives its own data (RMD0 for red and GMD0 for green) from its video memory plane and separate resolution select signals (RR1 – RR0 for red and GR1 – GR0 for green).

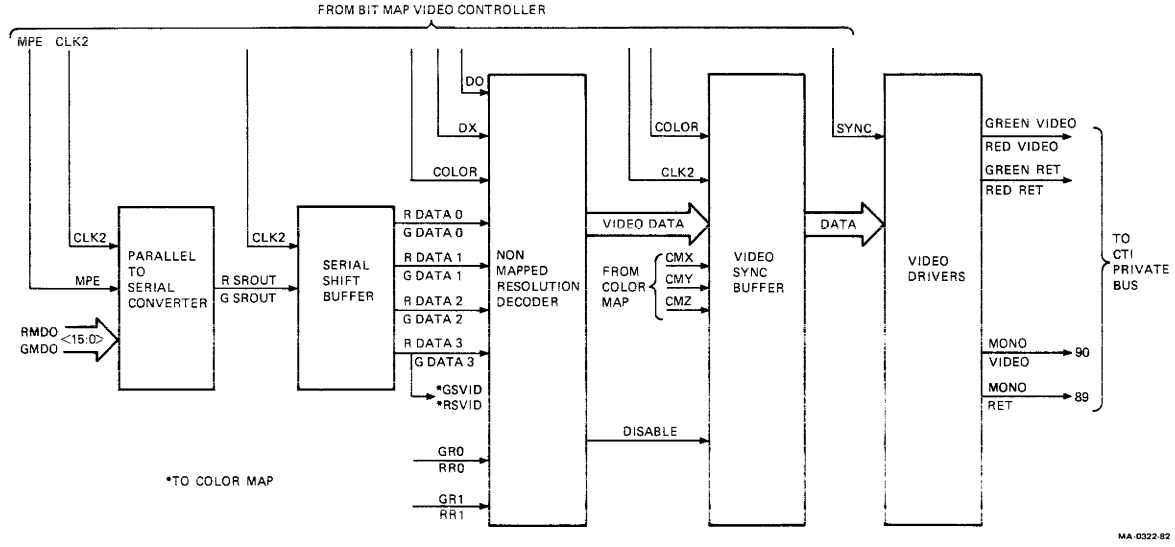
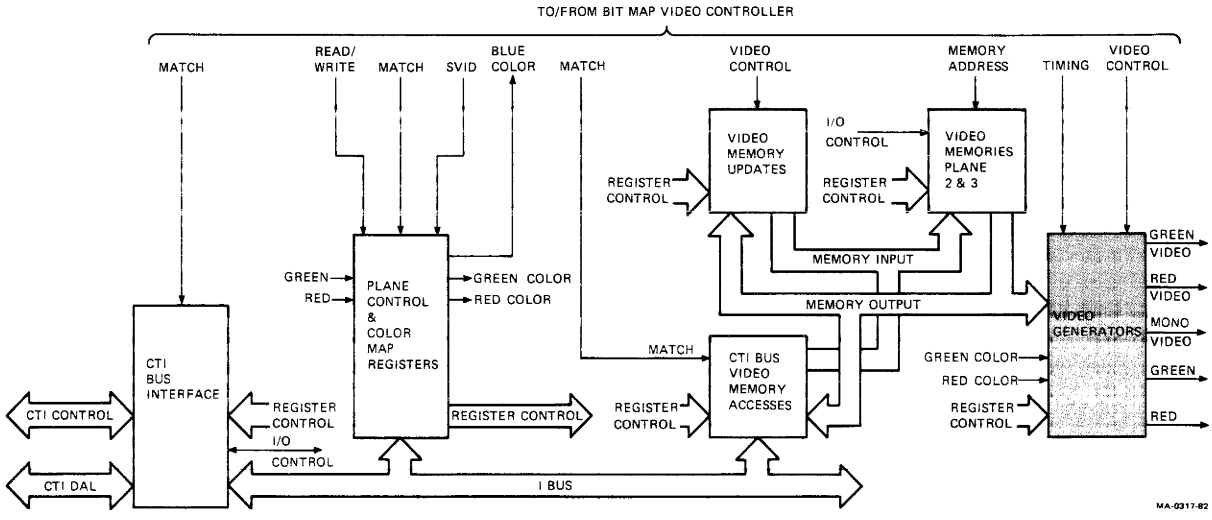


Figure 7-28 Video Generator Operation (Option Module)



The operation of these video generators is similar to the video generator described in Section 7.3.1.8. The only difference is each of these video generators contain a single video sync buffer that is used for both mapped and nonmapped applications.

NOTE

The SYNC signal, which is amplified by the plane 1 video generator when the extended bit map module is not in the video subsystem, is switched to the plane 2 video generator on the extended bit map for amplification. It appears on the GREEN VIDEO line and MONO VIDEO line when the extended bit map is in the system.

7.4 DETAILED CONNECTOR DESCRIPTIONS

The following section describes the connectors of the bit map video controller and extended bit map modules. The pins on the connectors are described as either inputs or outputs of each module.

7.4.1 CTI Bus Interface J1

The bit map video controller and extended bit map modules use the data/address and control lines of the CTI Bus to implement program data transfers. Figure 7-29 shows the pin functions and signal directions of this connector (for details see Chapter 5).

7.4.2 Drive Interface Connector J2

Table 7-7 lists the pin functions of the bit map video controller and extended bit map modules J2 connector shown in Figure 7-29. This connector allows direct communication between the bit map video controller and extended bit map modules.

The signal mnemonic column describes the asserted state of the signal. An L after the mnemonic indicates an asserted low state (logic zero). An H after the signal name indicates an asserted high state (logic high).

7.4.2.1 NOMEM H Signal – The extended bit map module generates this signal. When asserted, it indicates that either plane 2 or 3 video memories are selected. A video memory plane must be selected before host processor or data modification is assessed. To set the appropriate select bits, refer to the plane control register definitions in Section 7.5.

7.4.2.2 COLOR H Signal – The bit map video controller generates this signal. When asserted, it indicates that the color map is enabled.

7.4.2.3 BSELD L Signal – The bit map video controller generates this signal. When asserted, it indicates that the plane 1 video memory is enabled. If the plane 1 video memory is enabled for accesses, then accesses to plane 2 and 3 video memories are disabled.

7.4.2.4 WR12 H Signal – The bit map video controller generates this signal. It is a write strobe signal for the color map register during host processor accesses.

7.4.2.5 RD10 H Signal – The bit map video controller generates this signal. It is a read strobe signal for the plane 2 and 3 control register during host processor accesses.

7.4.2.6 WR10 H Signal – The bit map video controller generates this signal. It is a write strobe signal for the plane 2 and 3 control register during host processor accesses.

7.4.2.7 DX H Signal – The bit map video controller generates this signal. It is a 5 MHz clock with a 25% duty cycle used during high resolution (quad-bit) applications.

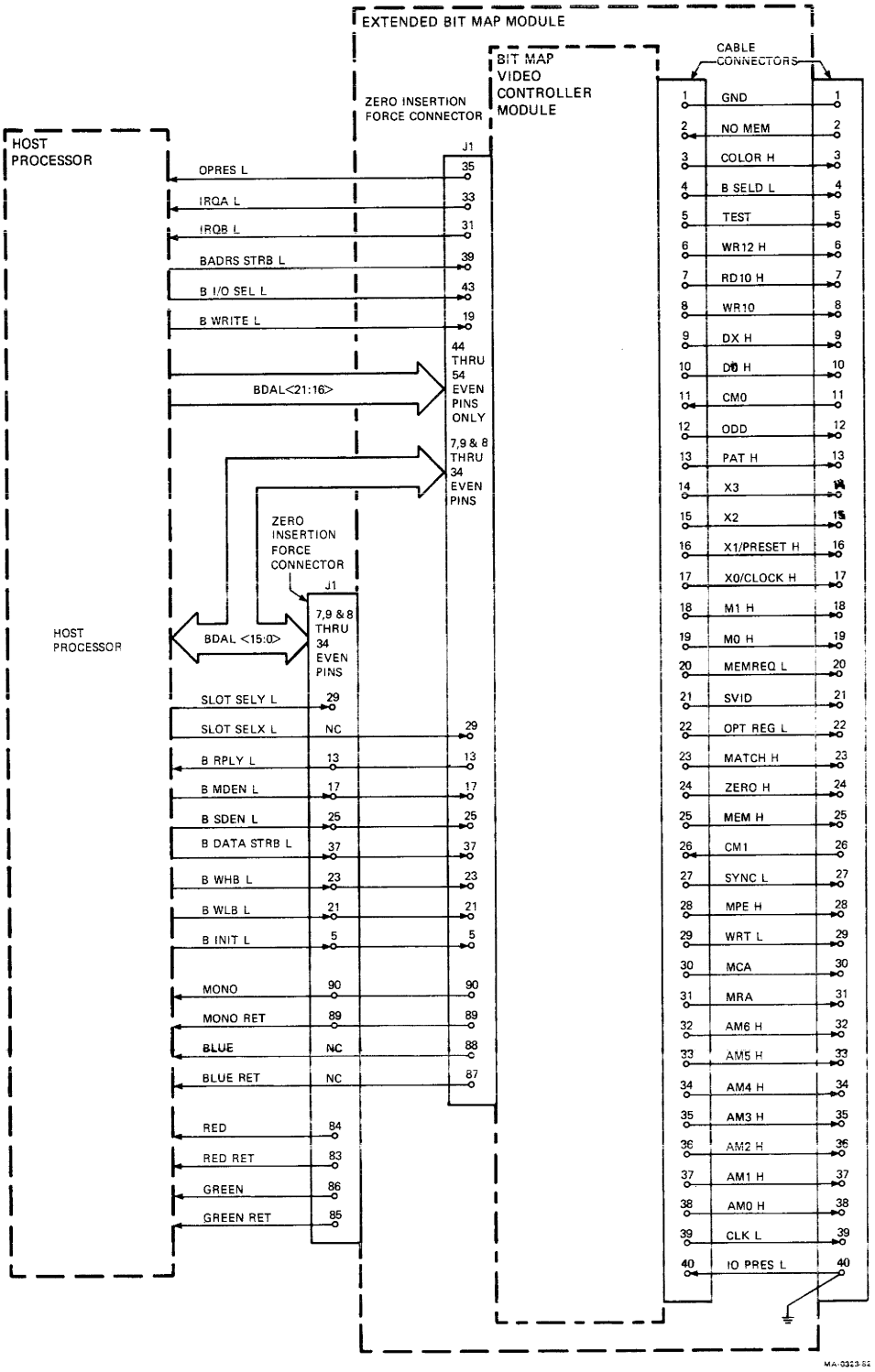


Figure 7-29 Bit Map Video Controller and Extended Bit Map Modules I/O Signal Flow

Table 7-7 Connector J2 Pin Description

Pin	Signal Meaning	Signal Mnemonic
1	Ground	
2	No memory	NOMEM H
3	Enable color map	COLOR H
4	Plane 1 selected	BSELD L
5	–	not used
6	Color map write strobe	WR12 H
7	Plane register read strobe	RD10 H
8	Plane register write strobe	WR10 H
9	5 MHz 25% duty clock	DX H
10	10 MHz clock	D0 H
11	Color map data	CM1
12	–	not used
13	Pattern	PAT H
14	Data modification bit	X3 H
15	Data modification bit	X2 H
16	Data modification bit	X1/PRESET H
17	Data modification bit	X0/CLOCK H
18	Data modification bit	M1 H
19	Data modification bit	M0 H
20	Host memory request	MEMREQ L
21	Plane 1 serial data	SVID
22	EBO register access	OPTREG L
23	Video memory access	MATCH H
24	Counter empty	ZERO H
25	Video memory enable	MEM H
26	Color map data	CM0
27	Video syncronization	SYNC L
28	Memory parallel enable	MPE H
29	Data modification write	WRT L
30	Memory column address	MCA
31	Memory row address	MRA
32	Memory address bit	AM6 H
33	Memory address bit	AM5 H
34	Memory address bit	AM4 H
35	Memory address bit	AM3 H
36	Memory address bit	AM2 H
37	Memory address bit	AM1 H
38	Memory address bit	AM0 H
39	20 MHz clock	CLK L
40	EBO present	IOPRES L

7.4.2.8 D0 H Signal – The bit map video controller generates this signal. It is a 10 MHz Clock with a 50% duty cycle used during medium resolution (dual-bit) applications.

7.4.2.9 CM1 and CM0 Signals – The extended bit map generates these signals. When the subsystem operates in the mapped mode, the color map provides these signals to generate a BLUE VIDEO signal on the bit map video controller.

7.4.2.10 PAT H Signal – The bit map video controller generates this signal. It is a pattern signal used during video memory update modification cycles.

7.4.2.11 X3 H, X2 H, X1/PRESET H, and X0/CLOCK H Signals – The bit map video controller generates these signals. During bit mode operations for a video memory update modification cycle, these bits specify the bit within the designated word to modify. During word mode operations for a video memory update modification cycle, these bits control shift operations to be performed on the video memory data.

7.4.2.12 M1 H and M0 H Signals – The bit map video controller generates these signals. During video memory update modification cycles, these bits specify the bit or word mode operation to be performed.

7.4.2.13 MEMREQ L Signal – The bit map video controller generates this signal. It is a host processor-to-video memory access indicator signal that enables video memory output to the CTI Bus.

7.4.2.14 SVID Signal – The bit map video controller generates this signal. When the subsystem operates in the mapped mode, this plane 1 video memory serial data addresses the color map to generate the CM1 and CM0 signals during screen refresh cycles.

7.4.2.15 OPTREG L Signal – The bit map video controller generates this signal. It is a host processor-to-extended bit map register access enable indicator signal.

7.4.2.16 MATCH H Signal – The bit map video controller generates this signal. It is a host processor-to-video memory access indicator signal that enables circuits to process video memory accesses to plane 2 and 3 video memories.

7.4.2.17 ZERO H Signal – The bit map video controller generates this signal. It is a counter register empty indicator signal.

7.4.2.18 MEM H Signal – The bit map video controller generates this signal. It is a host processor-to-video memory access indicator signal that enables the video memory.

7.4.2.19 SYNC L Signal – The bit map video controller generates this signal. It is a video synchronization signal which contains the horizontal, vertical, and equalization pulses needed to generate a composite video signal.

7.4.2.20 MPE H Signal – The bit map video controller generates this signal. It is a memory parallel enable signal used during screen refresh cycles.

7.4.2.21 WRT L Signal – The bit map video controller generates this signal. It is a data modification write strobe used during video memory update modification cycles.

7.4.2.22 MCA Signal – The bit map video controller generates this signal. It is a video memory column address strobe used during all video memory access cycles.

7.4.2.23 MRA Signal – The bit map video controller generates this signal. It is a video memory row address strobe used during all video memory access cycles.

7.4.2.24 AM6 H Through AM0 H Signals – The bit map video controller generates these signals. They are the address bits for the video memory and are used with the MCA and MRA signals.

7.4.2.25 CLK L Signal – The bit map video controller generates this signal. It is a 20 MHz clock signal for the extended bit map module.

7.4.2.26 IOPRES L Signal – The extended bit map module generates this signal. If the cable is connected between the modules, this signal is generated. It indicates the presence of the extended bit map module.

7.5 PROGRAMMING

The following section describes the bit map video controller and extended bit map modules programming registers. These registers are the host processor's access to the subsystem's video processing commands.

The bit map video controller module contains nine 16-bit registers to allow the host processor access to commands and status data of the controller. The extended bit map module contains additional registers to control its operations: a plane control register and a color map register. Access to all registers is done by accessing the CTI Bus register space of the bit map video controller module.

The bit map video controller module can be installed in any one of the six slots in the CTI Bus card cage. The starting address of the register address space (XXXXXX) depends on the card cage slot the module is installed in. Refer to Chapter 5 for assigned slot addresses and their address ranges.

Table 7-8 defines the 11 registers of the bit map video controller and the extended bit map modules. The plane 2 and 3 control register (OPC) and the color map register (CMP) are located on the extended bit map module and are accessible only when the optional module is installed.

NOTE

The register address XXXXXX02, is used only for CTI Bus protocol and is not recognized by the bit map video controller.

The control status register (XXXXXX04) is the only register on the bit map video controller that is byte addressable, all other registers are word addressable.

Table 7-8 Bit Map Video Controller Programming Registers

Address	Mnemonic	Function	Type
XXXXXX00	IDR	Identification code	Read-only
XXXXXX02	–	Reserved	
XXXXXX04	CSR	Control status	Read/write
XXXXXX06	P1C	Plane 1 control	Read/write
XXXXXX10	OPC	Plane 2 and 3 control	Read/write
XXXXXX12	CMP	Color map	Write-only
XXXXXX14	SCL	Scroll register	Read/write
XXXXXX16	X	X coordinate	Read/write
XXXXXX20	Y	Y coordinate	Read/write
XXXXXX22	CNT	Counter	Write-only
XXXXXX24	PAT	Pattern	Write-only
XXXXXX26	MBR	Memory base	Write-only

These registers also control the interrupts the bit map video controller sends to the host processor. These interrupts are controlled via the control and status register. An end of frame interrupt controls CTI interrupt line IRQA if the interrupt is enabled. A transfer done interrupt controls CTI interrupt line IRQB if the interrupt is enabled.

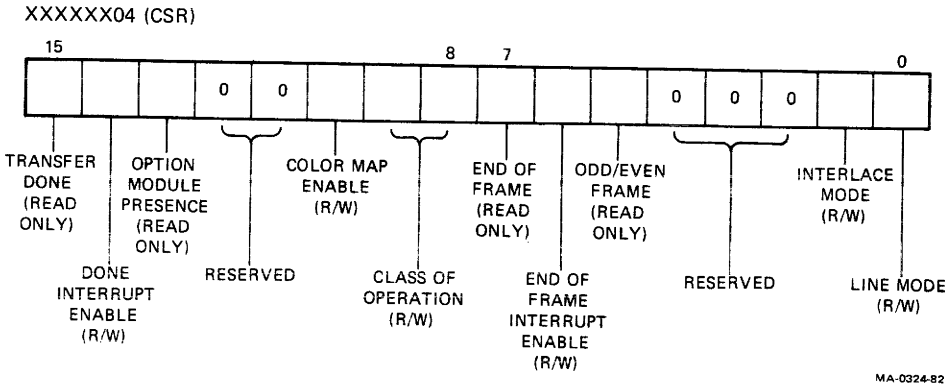
Registers should not be loaded unless the transfer done bit (CSR bit 15) is set. However, the X and Y registers are an exception. They may be loaded during an operation without affecting that operation.

7.5.1 Identification Code Register (IDR)

The host processor uses this register to identify the module for software routine selection. When read by the host processor, this register returns an identification value of 1002 (octal).

7.5.2 Control Status Register (CSR)

This register controls the general operation and video timing of the bit map video controller and the extended bit map module. The following is the bit organization of this register.



7.5.2.1 Bit 0 / Line Mode Definition – When this bit is reset (0), 525 line mode operation is selected (526 line for noninterlaced). When this bit is set (1), 625 line mode operation is selected (626 line for noninterlaced). This bit is reset during initialization.

7.5.2.2 Bit 1 / Interlace Mode Definition – When this bit is reset (0), a noninterlaced operation mode is selected. When this bit is set (1), an interlaced operation mode is selected. This bit is reset during initialization.

7.5.2.3 Bit 5 / Odd/Even Frame Definition – This bit indicates when the subsystem scans the odd lines (bit reset) or the even lines (bit set).

7.5.2.4 Bit 6 / End of Frame Interrupt Enable Definition – When this bit is reset (0), the end of frame interrupt to the host processor is disabled. When this bit is set (1), the end-of-frame interrupt is generated (IRQA) to the host processor when bit 7 goes set.

7.5.2.5 Bit 7 / End of Frame Definition – When this bit is set (1), the video subsystem performs a vertical retrace. The host processor can update the video memory without generating displayed distortion.

7.5.2.6 Bits 8 and 9 / Operation Class Definition – These bits select the bit and word mode operations the subsystem performs during update modifications to the video memory. The following are the bits and word mode selected operations.

Bits 9	Bits 8	Selected Operation
0	0	Bit transfers shifted left to right
0	1	Bit transfers shifted top to bottom
1	0	Word transfers shifted left to right
1	1	Word transfers shifted right to left

7.5.2.7 Bit 10 / Color Map Enable Definition – When this bit is reset (0), the color map is disabled and the video subsystem operates in the nonmapped mode. When this bit is set (1), the color map is enabled and the subsystem operates in the mapped mode.

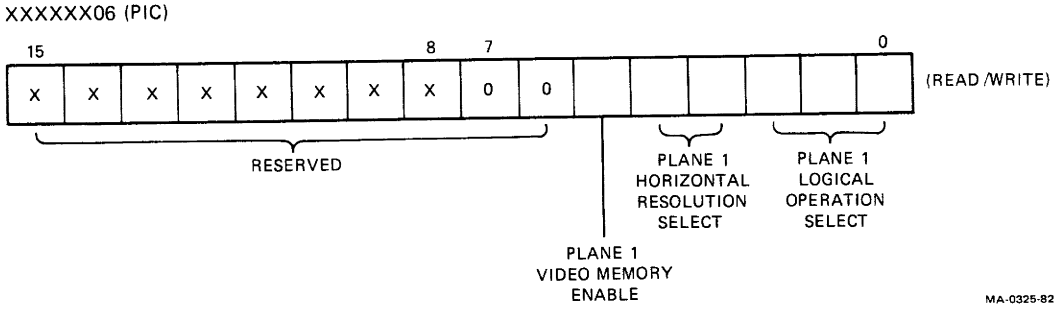
7.5.2.8 Bit 13 / Option Presence Definition – When this bit is reset (0), the extended bit map is present and connected to the bit map video controller. When this bit is set (1), the extended bit map is not present.

7.5.2.9 Bit 14 / Done Interrupt Enable Definition – When this bit is reset (0), the transfer done interrupt to the host processor is disabled. When this bit is set (1), the transfer done interrupt is (IRQB) generated to the host processor when bit 15 goes set.

7.5.2.10 Bit 15 / Transfer Done Definition – When this bit is set, the last host processor commanded transfer is complete (counter register equals 0) and any register may be accessed.

7.5.3 Plane 1 Control Register (P1C)

This register defines a logical operation (update modification) to be performed on the plane 1 video memory. If the subsystem is operating in the nonmapped mode, it selects the resolution mode. This register also enables the plane 1 video memory for logical operations and host processor accesses. The following are the bit definitions for this register.



NOTE

If the color map is enabled (CSR bit 10), the bit map video controller ignores this registers resolution bits (P1C bits 3 and 4) and sets the resolution to 1024.

7.5.3.1 Bits 2, 1, 0 / Plane 1 Logical Operation Select Definition – These bits select the logical operation to be performed on data stored in the plane 1 video memory. Since the CSR bits 8 and 9 select bit or word update modification modes, these bits define the logical operation for either mode. Table 7-9 defines the selected update modification for bit mode operations. Table 7-10 defines the selected update modification for word mode operations.

During bit mode logical operations 1–5, the pattern register is rotated. This is a bit-by-bit rotation of the pattern register starting with the least significant bit. Logic operations 6 and 7 do not use the pattern register.

Word mode logical operations use only the least significant bit of the pattern register. The pattern register does not rotate in word mode.

The shift screen operation shifts all bits in the words specified by the counter register either left or right. Bits shifted from the last word of each scan line are lost. The incoming bits are from the least significant bit of the pattern register.

Table 7-9 Bit Mode Logical Operations

Bits 2	1	0	Selected Operation
0	0	0	No operation
0	0	1	XOR pattern register and screen contents to screen
0	1	0	Move pattern register to screen.
0	1	1	Move complement of pattern register to screen.
1	0	0	Bit set pattern to screen
1	0	1	Bit clear pattern to screen
1	1	0	Clear current bit on screen.
1	1	1	Set current bit on screen.

Table 7-10 Word Mode Logical Operations

Bits 2	1	0	Selected Operation
0	0	0	No operation
0	0	1	Complement screen
0	1	0	Move pattern register to screen.
0	1	1	Move pattern complement to screen.
1	0	0	Reserved
1	0	1	Shift screen 1 bit (see CSR for shift direction).
1	1	0	Shift screen 2 bits (see CSR for shift direction).
1	1	1	Shift screen 4 bits (see CSR for shift direction).

7.5.3.2 Bits 4, 3 / Plane 1 Horizontal Resolution Select Definition – These bits select the horizontal resolution the plane 1 video generator operates in if the video subsystem is operating in the nonmapped mode. During an initialization, these bits are reset (0) to select 1024 single bit resolution. These resolutions are selected as follows.

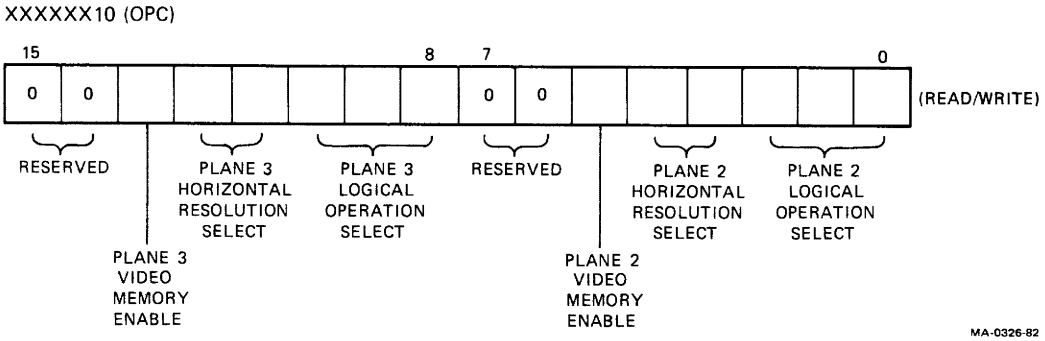
Bits 4	3	Selected Resolution
0	0	1024 single bit resolution (2 levels of intensity)
0	1	512 two bit resolution (4 levels of intensity)
1	0	256 four bit resolution (16 levels of intensity)
1	1	Display off (black)

7.5.3.3 Bit 5 / Plane 1 Video Memory Enable Definition – When this bit is set the host processor can perform write, read, or read-modify-write operations to the plane 1 video memory. When this bit resets, all host processor accesses and video memory update modifications to the plane 1 video memory are inhibited.

During host processor accesses, write operations occur to all planes that have the video memory enable bit set (also see OPC register); read operations occur from the first video memory that has the video memory enable bit set starting with plane 1 and ending with plane 3. If no video memory plane is enabled, the host processor cannot read and times out.

7.5.4 Plane 2 and 3 Control Register (OPC)

This register defines a logical operation (update modification) to be performed on plane 2 and plane 3 video memories, selects the resolution mode for each plane if the subsystem operates in nonmapped mode, and enables the plane 2 and plane 3 video memories for logical operations and host processor accesses. This register is on the extended bit map module and is accessible when the option presence bit in the CSR is reset. The following are the bit definitions for this register.



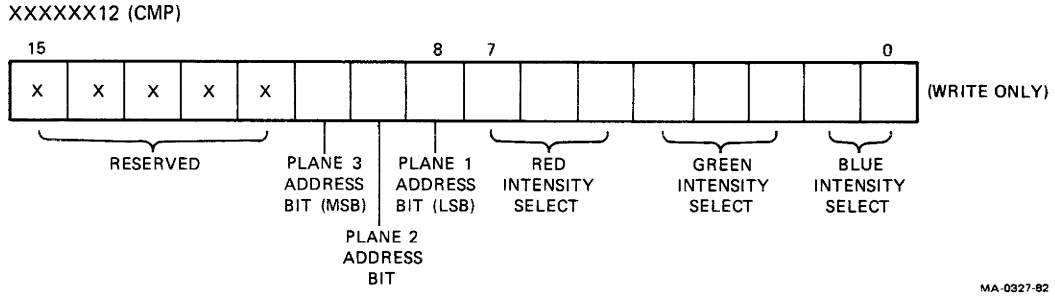
NOTE

If the color map is enabled (CSR bit 10), the bit map video controller ignores resolution bits (OPC bits 3, 4, 11, and 12) and sets the resolution to 1024.

The bit definitions for these register bits are identical to the P1C register except this register controls the plane 2 and plane 3 video memories.

7.5.5 Color Map Register (CMP)

The color map register allows for programming of the color map when the video subsystem operates in the mapped mode. This register contains eight locations, each of which holds eight bits of data. The low byte of this register defines the color intensity each video generator produces. Three bits of the high byte define the address of one of the eight words of the color map register. This is also the address formed from the combined serial outputs of the video memory planes. The RED and GREEN VIDEO signals allow for seven intensity levels. The BLUE VIDEO signal has four intensity levels, however they are in the same range as the red and green. The mono output always contains the sum of all the intensity levels (Section 7.3.1.8). The following is the bit organization of this register.

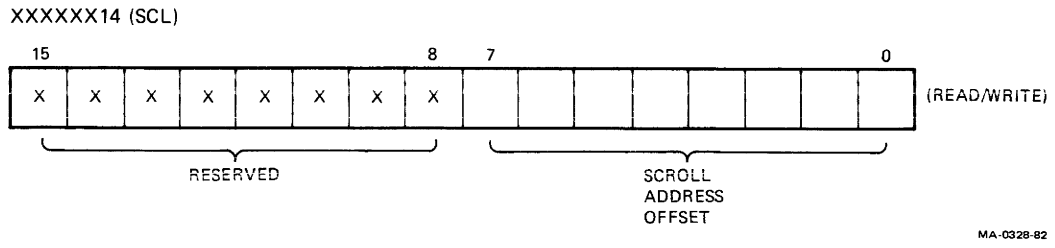


7.5.6 Scroll Register (SCL)

The scroll register controls the addressing of the video memory planes for all operations. This register's contents are always added to the Y coordinate addresses when writing and reading to the bit map. Changing the contents causes a vertical scroll on the screen (increment scrolls up, decrement scrolls down).

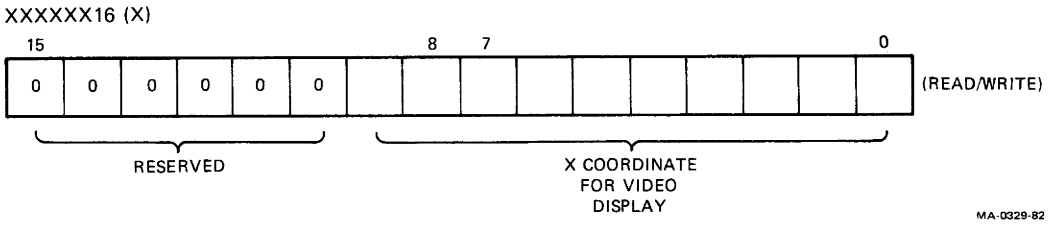
Operations with the scroll register can be absolute. However, the scroll register may have any value when a program starts. Therefore, the register contents must be incremented/decremented or added to/subtracted from.

After writing to the screen, the data is moved up or down by changing the scroll register contents. The following are the bit definitions of the scroll register.

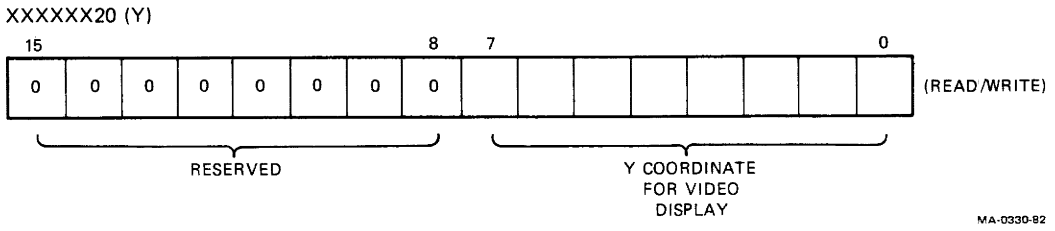


7.5.7 X and Y Registers (X) (Y)

The X register holds the horizontal scan location of all transfers to the video memory planes. It can be modified at any time during an operation with no effect on the operation. For word mode applications, the lower four bits of X register are ignored (bit within the word). For word mode shift right to left operations, the X register defines the coordinate of the rightmost word on the top line to be shifted. For word mode shift left to right operations, the X register defines the coordinate of the leftmost word. The following is the bit organization for this register.



The Y register holds the starting screen location of all video operations defined in the P1C or OPC registers to the video memory planes. It can be modified at any time during the operation with no effect on the operation. For 60 Hz operation, the row of words with Y coordinates 239 is always the bottom visible scan line. For 50 Hz operation, the row of words with Y coordinates 255 is the bottom scan line. The register contents are offset as described in the scroll register definition. The following are the bit definitions for this register.

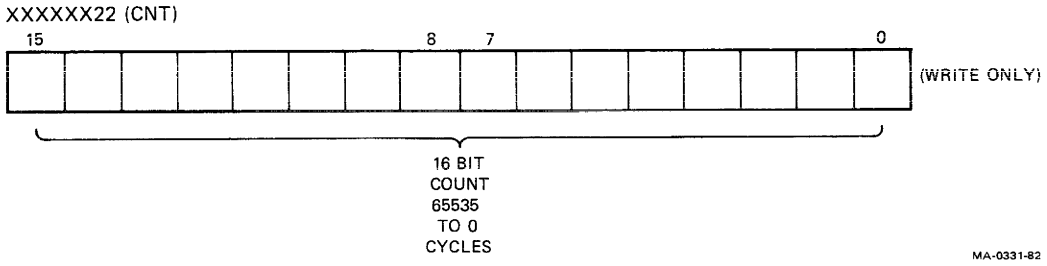


NOTE

Only 240 of the 256 available Y lines are visible at any time in 60 Hz mode.

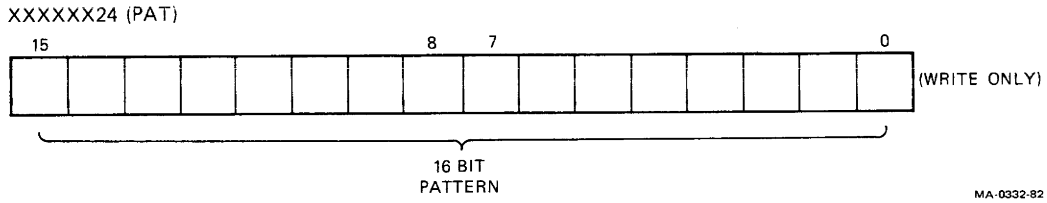
7.5.8 Counter Register (CNT)

When this register is loaded with anything but a 0, a transfer is started. The counter decrements after each cycle (bit or word) until the counter is 0. When 0, the counter is stopped and the transfer done bit (CSR bit 15) is set. If the interrupt is enabled, an interrupt is generated to the host processor. The counter can only be loaded if the transfer done bit is set. Loading the counter register clears the done bit. The following is the bit definition for this register.



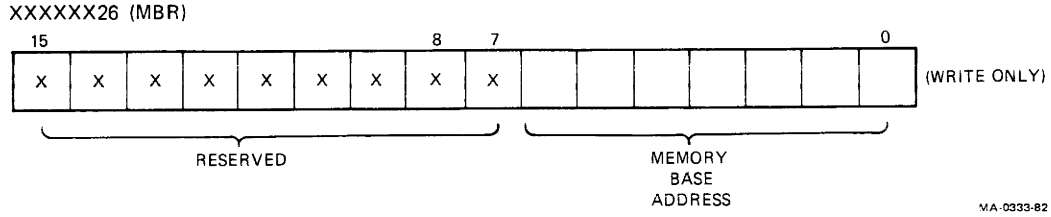
7.5.9 Pattern Register (PAT)

During a transfer, the least significant bit of this register can be used as data during an update modification cycle for each plane. After each cycle in bit mode (see CSR bits 8 and 9), the pattern register contents are rotated right one bit. For example, bit 0 shifts to 15, 1 to 0, 2 to 1, etc. In word mode, only the least significant bit of the pattern register is used, the upper 15 bits are ignored. The pattern register can only be loaded if the done bit (CSR bit 15) is set (the counter register is 0). The following are the bit definitions for this register.



7.5.10 Memory Base Register (MBR)

This register assigns the starting address of the 16K video memories page that the bit map video controller responds to. The starting addresses, as they appear on the CTI Bus, are on any 16K word boundary. The register contents are then compared to the CTI Bus DAL lines <21:15> respectively. The following are the bit definitions for this register.



7.6 SPECIFICATIONS

The following list contains the specifications for the bit map video controller module. Software for self-testing is not resident on the video controller. Any self-test to be used must be resident on some external device. No power-up testing is performed.

Item	**Power**
Bit map video controller	+5 Vdc ± 5% @ 3.3 A +12 Vdc ± 5% @ 55 mA
Extended bit map	+5 Vdc ± 5% @ 2.75 A +12 Vdc ± 5% @ 45 mA
Power Sequencing	No specific sequence is required for operation on this module.
Physical Dimensions (either module)	
Width	13 cm (5.2 in)
Length	30 cm (12 in)
Depth	1.5 cm (0.6 in)

Display Characteristics

The video subsystem is program selectable via the COMMAND/STATUS register (CSR) for 50 or 60 Hz operation and a variety of video timing characteristics.

Display	
Pixels/scan	256
Pixel rate	5 MHz
Pixel period	200 ns
Display	
Pixels/scan	512
Pixel rate	10 MHz
Pixel period	100 ns
Display	
Pixels/scan	1024
Pixel rate	20 MHz
Pixel period	50 ns
Horizontal Frequency	15625 Hz

Vertical Timing

The vertical timing is set to 60 Hz noninterlaced at power-up.

60 Hz noninterlaced/59.411 Hz
526 scan lines 240 displayed lines/page

60 Hz interlaced/59.524 Hz
525 scan lines 240 displayed lines/page

50 Hz noninterlaced/49.920 Hz
626 scan lines 256 displayed lines/frame

50 Hz interlaced/50.000 Hz
625 scan lines 256 displayed lines/frame

CHAPTER 8
VR201 MONOCHROME MONITOR

8.1 GENERAL

This chapter describes the VR201 monochrome monitor shown as the shaded part of the system functional block diagram in Figure 8-1.

The VR201 monochrome monitor is a raster scan device for displaying alphanumeric/graphic video information. It monitors the video display. However, the type of display presented depends on the video input to the monitor from the system box. This is determined by the operator and system software.

8.1.1 Related Documentation

Refer to the following related documentation while reading this chapter.

Title	Document No.
KEF11 Field Maintenance Print Set	MP-01473-00
VR201 Monochrome Monitor Field Maintenance Print Set	MP-01410-00

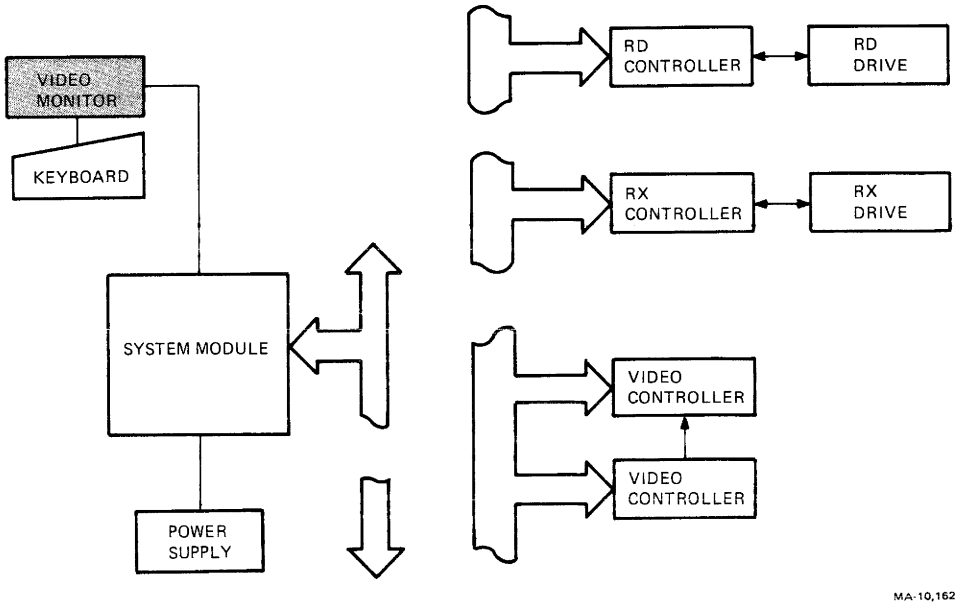


Figure 8-1 System Block Diagram

8.2 PHYSICAL DESCRIPTION

The VR201 monochrome monitor is enclosed in a wedge-shaped cabinet. The CRT face provides a viewing area of 12.7 × 20.3 cm (5 × 8 inches) on a screen that measures 30.5 cm (12 inches) diagonally. A plastic button covers a screw on the rear of the cabinet. This screw holds the cabinet to the internal wire frame. The CRT and the monochrome monitor module mount inside this frame.

The frame has metal finger stock that presses against the screw mounting bracket and a metal shield. To prevent electromagnetic radiation, this shield covers the entire inside of the cabinet. There is a folding carrying handle on the bottom rear of the cabinet.

The glass front of the monitor, the CRT face, is coated with a special chemical to reduce glare to the operator.

The monitor viewing angle is adjustable between +5 to −25 degrees. To adjust the angle, the operator pushes a release on the right side (Figure 8-2). This causes a friction-lock foot to drop down from the bottom of the cabinet housing.

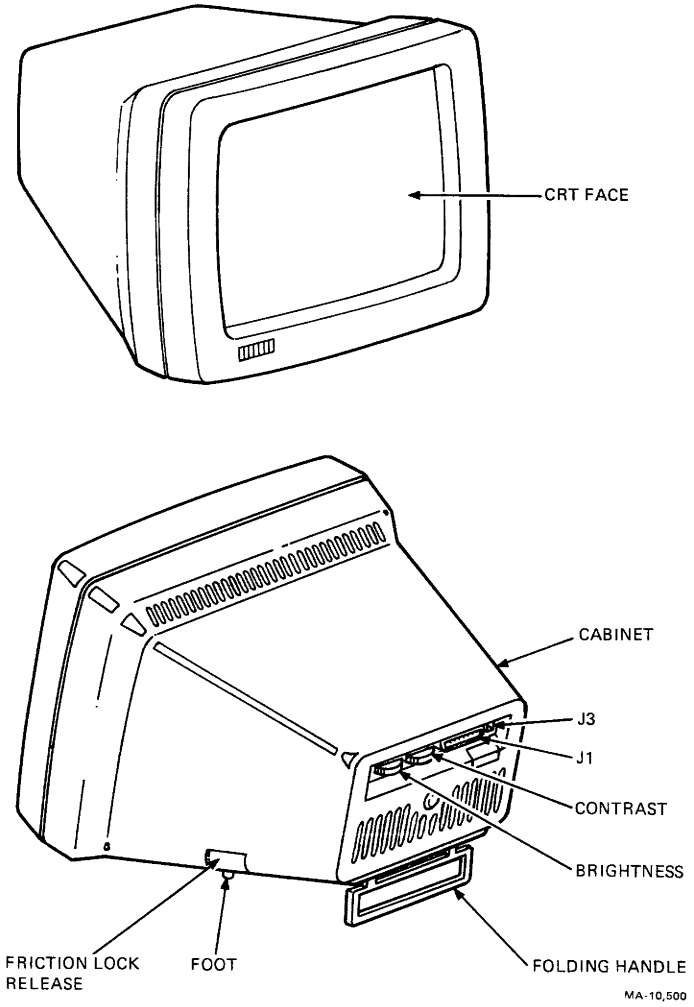


Figure 8-2 Monochrome Monitor Exterior View

The contrast and brightness controls are on the rear panel. There are also two connectors on the rear of the monitor: J1 and J3. J1 is a 15-pin D-type connector that connects to the system box with a cable (PN BCC02) and J3 is a modular telephone jack that connects to the keyboard with another cable (PN BCC02).

The physical dimensions for the monochrome monitor are as follows.

Height	24.8 cm (9.75 in)
Width	29.8 cm (11.73 in)
Depth	30.6 cm (12.23 in)
Weight	6.5 kg (14.5 lb)

8.3 FUNCTIONAL OVERVIEW

The VR201 monochrome monitor consists of two main components: a 12-inch diagonal CRT with a yoke assembly mounted on it and an electronics module (Figure 8-3).

Display activity is the primary function of the monitor. A secondary function is to route information between the system box and the keyboard. The keyboard connects with the monitor via J3 (Figure 8-3). J3 is hardwired on the module to J1, which connects to the system box.

The monitor module controls the CRT and the yoke assembly. A composite video signal is input to the module from the system box (Figure 8-3). This signal consists of two types of information: video data (Section 8.3.1), and sync data (Section 8.3.2).

The monitor module provides the following power to the CRT.

Anode voltage	Grid 4 voltage (focus)
Grid 1 voltage (brightness)	Heater voltage
Grid 2 voltage (cutoff)	Cathode voltage

The control inputs to the CRT refine the electron beam. The anode voltage attracts the beam to the faceplate and provides a single connection between the CRT and the module (Figure 8-3). P1 provides all other CRT inputs. P1 is mounted directly on the CRT and is hardwired to the module. Refer to Section 8.7.7 for more information.

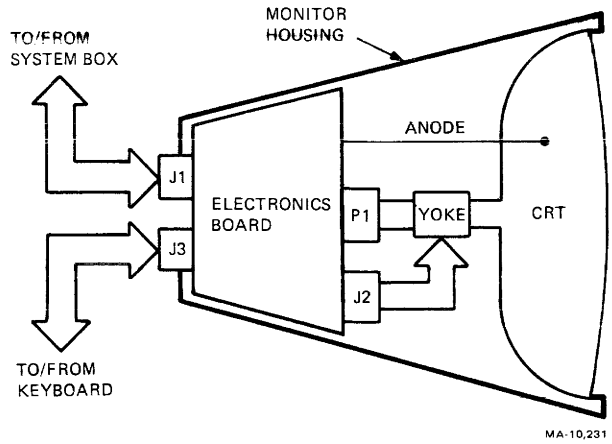


Figure 8-3 Monochrome Monitor Block Diagram

8.3.1 VIDEO Data

The monitor module uses the video portion of the signal to generate outputs to the CRT cathode. The CRT responds to the video by generating various intensities in the electron beam. The intensity of the beam is dependent on the amplitude of the video signal provided.

8.3.2 SYNC Data

The sync portion of the video synchronizes the generation of horizontal and vertical signals to the yoke assembly. The horizontal and vertical processor chips use peak detector circuits to separate the synchronizing signals. The yoke assembly, which connects to the electronics board via J2, consists of electromagnetic coils (Figure 8-3). These coils use the signals output by the module to generate magnetic fields which position the electron beam generated by the CRT. The horizontal signal to the yoke controls the sweep of the electron beam horizontally across the faceplate (each sweep is called a scan line). The vertical signal controls the positioning of the beam to a new scan line for vertical positioning.

8.4 MONOCHROME MONITOR SYSTEM COMMUNICATION

The monochrome monitor connects with both the system box and the keyboard. The system box connects to the monitor via J1, a 15-pin D-type subconnector. The keyboard connects via J3, a modular telephone jack.

J1 has three basic functions: the supply of video input used only at the monitor, the supply of operational voltages used by both the monitor and the keyboard, and the transfer of keyboard data (Figure 8-4). The operational voltage and keyboard data lines are hardwired from J1 to J3 on the electronics board.

Table 8-1 provides a pin-out for J1 with signal identifications and functional descriptions. Table 8-2 provides the same information for J3.

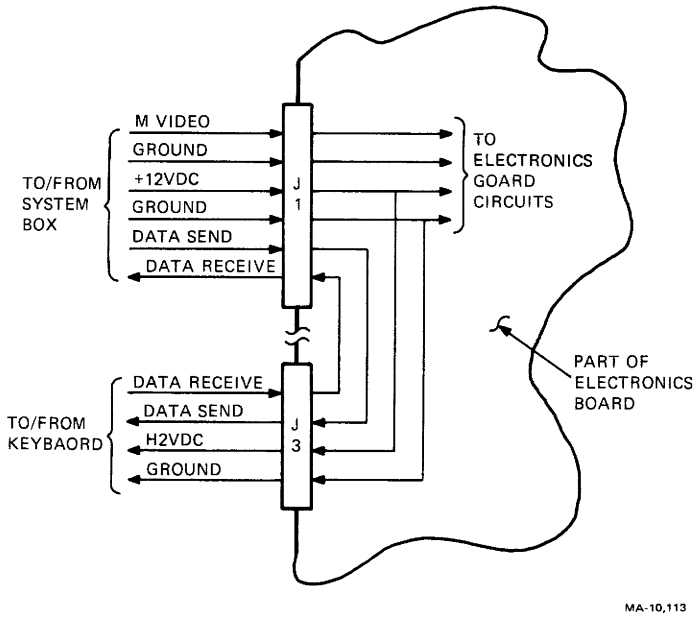


Figure 8-4 Monochrome Monitor System Communications Diagram

Table 8-1 J1 Pin-out

Pin(s)	Signal	Description
1–3	Not used	None
4	Ground	Video signal ground potential
5,6	Ground	Operational voltage ground potential
7,8	+12 Vdc	Operational voltage input
9–11	Not used	None
12	M Video	Composite video (refer to Section 8.3.1)
13	Ground	Tied to pins 5 and 6
14	Data Receive	Serial data line from the keyboard output to the system box (via J3)
15	Data Send	Serial data line from the system box output to the keyboard (via J3)

Table 8-2 J3 Pin-out

Pin	Signal	Description
1	Data Send	Serial data line for output from the system box to the keyboard (via J1, pin 15)
2	+12 Vdc	Output of operational voltage to the keyboard (from J1, pins 7 and 8)
3	Ground	Operational voltage ground potential (from J1, pins 5, 6 and 13)
4	Data Receive	Serial data line for input from the keyboard to the system box (via J1, pin 14)

8.4.1 Composite Video Signal

The video input to the monitor is a composite of two types of signals: video and sync. There are different levels of illumination within the video signal, ranging from totally black to maximum brightness.

Figure 8-5 represents a typical composite video signal and identifies the major terms associated with it. This signal, used with the monochrome monitor, is compatible with EIA RS170 standards. However, it is dc coupled to ground at the monitor module. Table 8-3 provides typical signal values.

Figure 8-6 shows the composite video signal and the sync portion of this signal. Table 8-4 describes the values for the sync components identified.

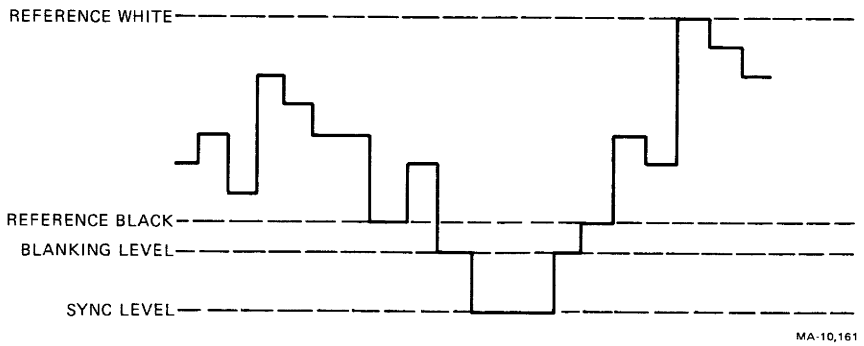


Figure 8-5 Composite Video Signal Representation

Table 8-3 Composite Video Values

Characteristics	Value
Output impedance	75 Ohms, dc coupled to 0 V
Amplitude	1 V peak-to-peak nominal (the monitor accepts signals with peak-to-peak values of 0.9 V through 1.5 V)
Reference black	The low limit of display value. It equals 30% of the peak-to-peak value (0.3 V nom), and is the lowest voltage value to be amplified linearly at the electronics board.
Reference white	The high limit of display value. It equals 100% of the peak-to-peak value (1.0 V nominal), and is the highest voltage value to be amplified linearly at the electronics board.
Blanking level	Voltage value which reduces CRT electron beam current below cutoff
Sync level	Voltage level at which sync actions can take place; 0 V nominal (dc coupled video to ground)
Continuous input	+2 V max (2 V saturates the video amplifier unless the contrast thumbwheel adjustment is reduced)

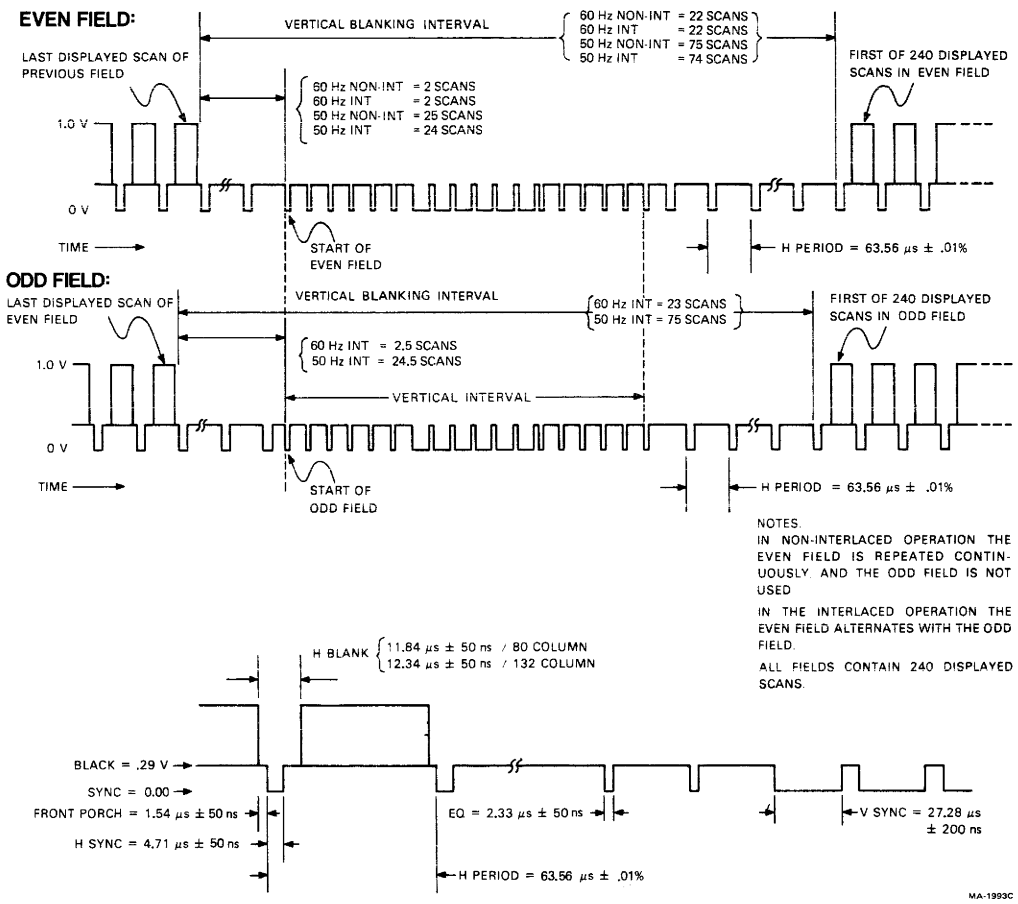


Figure 8-6 Composite Video Sync Timing Diagram

Table 8-4 Composite Video Sync Component

Component	Description
Vertical blanking interval	Period of time screen is blanked for vertical retrace activity; vertical retrace is completed in less than 1 ms, and within an allowed frequency range of 49–61 times per second
V Sync	Period of time in which vertical deflection circuitry on the electronics board is synchronized to the next frame
H Sync	Period of time in which horizontal deflection circuitry on the electronics board is synchronized for retrace
H Period	Period of time for the horizontal scan plus horizontal blanking (63.5 μs)
EQ	Equalizer pulse that synchronizes vertical deflection circuitry on electronics board for vertical retrace activity
Front porch	Delay value between start of blanking and start of sync pulse
Vertical interval	Period of time the actual synchronizing of the vertical deflection circuitry on the electronics board takes place; consists of six EQ pulses, six V sync pulses, and six more EQ pulses

8.5 CRT

The CRT provides the final video output, an electron beam, fired at a phosphor-coated faceplate.

The electron beam generation is controlled directly by the monitor module inputs. The module controls the yoke, which in turn positions the beam at the faceplate.

The CRT contains an electron gun. The gun consists of the heater element, a cathode, three grids (G1, G2, and G4), an anode, and the faceplate, all encased in a vacuum.

The three grids control the beam generated by the gun: G1 for brightness, G2 for beam cutoff, and G4 for focus.

G1 is directly affected by the brightness control thumbwheel. This enables the operator to adjust the background intensity of the display. G2 provides sharpening capabilities of the video. To do this, G2 acts as a gate or valve to the electron beam. A voltage, provided to G2, prevents the electron beam from passing to the faceplate unless the beam is of a specific minimum intensity. G4 focuses the electron beam.

The CRT plugs directly into P1 which is hardwired onto the module. Through P1, the operational voltages for the heater element, the cathode, and the three grids are provided. The anode voltage is provided by a separate connection between the module and the CRT. Its ground goes to the CRT case. This ground reduces shock hazard and consists of three parts: a connection between the module and a terminal block on the yoke, a connection between the block and the CRT case, and a connection between the block and P1.

8.6 YOKE

The yoke is a set of electromagnetic devices mounted on the neck of the CRT. One device is for horizontal deflection of the electron beam, the other is for vertical deflection.

Currents to control the horizontal scan line are applied to the yoke's coil (inductance) through the width inductor and the linearity inductor. The vertical trace control current comes from the vertical processor chip.

The yoke connects to the electronics board through J2: pins 2 and 3 for the horizontal deflection magnetic coils, pins 1 and 4 for the vertical.

8.7 MONITOR MODULE

The monitor module is made of discrete analog components. It can be divided into seven circuits to control the CRT and yoke.

Figure 8-7 is a block diagram of the module showing the seven circuits. The figure also identifies the fuse for the power input (F1), and three connectors (a fourth connector, J3, which routes signals between J1 and the keyboard is not shown). The following paragraphs provide descriptions of each of the items in Figure 8-7.

8.7.1 Dynamic Focus

This circuit creates different focus voltages for different areas of the screen. Output from this circuit is tied to focus biasing circuitry within the grid bias circuit. This output offsets focus biasing based on horizontal and vertical deflection values. The circuit is primarily a single transistor which acts as a mixer for parabolic inputs from the horizontal and vertical deflection circuits. This changes focus biasing as a function of the position of the beam on the tube.

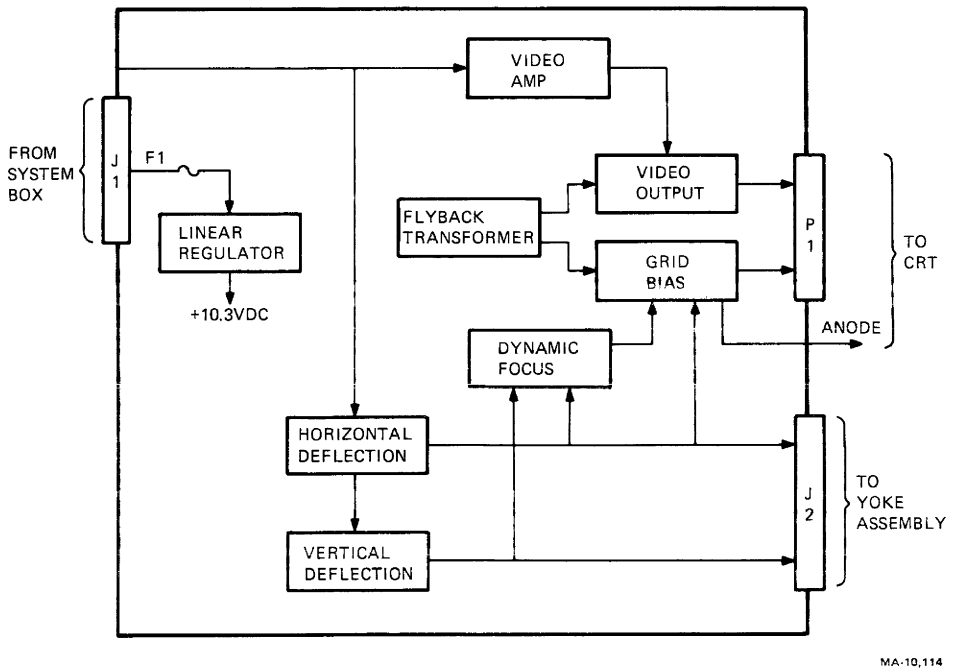


Figure 8-7 Monitor Module Block Diagram

8.7.2 Grid Bias

This circuit generates CRT biasing values: focus (G4), cutoff (G2), and brightness (G1). These voltages are developed from the flyback transformer. Voltages from this transformer are routed to the G4 and G2 circuits. There are resistor networks each containing potentiometers for adjusting the bias in question, R43 for G4 (focus) or R120 for G2 (cutoff). The remaining bias circuit, G1 (brightness), is a resistor network between two voltage sources, +40 Vdc and −150 Vdc. This adjustment allows the operator to adjust the display background intensity. The voltage on G1 is adjustable from approximately 0 to −47 Vdc.

8.7.3 Horizontal Deflection

This circuit drives the CRT beam across the faceplate horizontally. This circuit contains the following elements.

1. A horizontal processor
2. A sync buffer circuit
3. A horizontal driver and output
4. RC networks that bias circuits internal to the horizontal processor
5. A horizontal deflection generator output stage (width and linearity inductors, horizontal output transistor, damper diode, retrace capacitor, and yoke inductor)

An oscillator within the horizontal processor allows the horizontal deflection circuit to run free. The sync pulses then synchronize the operating running rate to the video input.

The sync buffer circuit amplifies the sync pulse and then applies it to the horizontal processor. When the horizontal output turns off, the electron beam flies back, returning the beam to the left of the screen. At the end of retrace, the conducting of the damper diode establishes a ramp of current in the yoke inductor. To make sure the output transistor is turned on at the proper time, the horizontal deflection IC also provides the correct timing on its output pulse. This allows the current ramp to continue after the damper diode stops conducting. The width coil portion of the output stage adjusts the width of the display. Two of the RC networks contain potentiometers for adjusting their biasing values: R211 for hold (horizontal) and R218 for centering (phase).

A secondary output from the generator is provided to the vertical deflection circuitry as a vertical sync signal.

8.7.4 Linear Regulator

This circuit provides power to the flyback transformer during initial power up and also regulates the input voltage. During initial power up, the +12 Vdc voltage is applied to the regulator. The voltage input (rising from 0 V to +12 Vdc) is shunted through a series of 4 diodes and then through the flyback transformer. This generates 40 Vdc at the input of L300 to the regulator field effect transistor (FETs) sources. The FETs are then turned on and conduct the load current instead of the diodes. A precision zener diode plus the regulator transistor's V_{BE} cause the circuit to provide 10.3 Vdc regulated output.

8.7.5 Vertical Deflection

This circuit positions the CRT beam across the faceplate vertically. This ciruit contains the following elements.

1. A vertical processor
2. Various RC networks responsible for biasing of circuits internal to the vertical processor
3. An output filter network

An oscillator within the vertical processor allows the vertical deflection circuit to free run. The sync pulses synchronize the vertical deflection to prevent vertical roll.

Three of the RC networks contain potentiometers for adjusting biasing values: R48 for hold (vertical), R50 for height, and R53 for linearity. At the beginning of each refresh cycle, the vertical processor receives a vertical sync pulse from the horizontal processor circuit. The horizontal processor detects the vertical sync pulse and sends it to the vertical processor. This sync pulse comes from the composite video input to the monitor module. The vertical sync pulse causes the beam to fly back vertically and begin a new frame.

8.7.6 Video Amp

The video amp consists of an input and output stage. The video signal is applied to an input push/pull transistor network which is part of an encapsulated transistor array. The input is provided from R5, the contrast thumbwheel potentiometer. The potentiometer is adjustable by the operator for personal contrast preference. The potentiometer, R119, provides a preamplifier adjustment to preset the range that can be affected by the contrast thumbwheel. Biasing of the input stage affects the biasing of the output stage which is another transistor network. The more positive the input to the input stage, the more positive the output from the transistor network. This output is provided to the video output stage.

The video output stage provides the operational voltage for the CRT beam. The video output stage uses the voltage from the flyback transformer (40 Vdc) to generate its output. The sync pulses (horizontal and vertical) set the video output to or below the cutoff voltage so the operator does not see the retrace lines. Applying increased positive video amp signal decreases the output to the CRT. This also increases the intensity of the CRT display.

8.7.7 Flyback Transformer

The flyback transformer is the high voltage power supply and is synchronized to the horizontal deflection. It generates the voltages used by the grid bias circuit (G1, G2, G4), the anode voltage (12.5 kV nom), and the 40 Vdc voltage used by the linear regulator and video amplifier.

WARNING

The monochrome monitor contains shock hazard voltages. Use extreme caution when servicing the monitor.

There is a high voltage (12 kV NOM) on the anode lead and the anode cup on the side of the CRT.

To avoid shock, use the following procedure when discharging the anode.

1. **Turn off system power and connect the monitor cable.**

2. **Attach the clip lead of the anode discharge tool to the metal frame.**

3. **Hold the tool by its insulated handle. Using one hand, carefully slide the tip of the tool under the plastic anode cap until it touches the anode. Avoid scratching or poking the glass CRT envelope.**

4. **Once discharged, remove the tool and clip lead.**

There is also 700 Vdc on the monitor module near the flyback transformer. Use caution when performing adjustments in this area. This area is covered with a protective shield.

CAUTION

Before removing the system module monitor cable, turn off the system power. Static discharge in the CRT can damage the monitor module and/or keyboard electronics.

Be sure the system power is off before connecting or disconnecting the monitor's cable for service or moving the monitor. When performing adjustments, secure the monitor's cable to the monitor with its thumbscrews so the cable does not loosen.

Failure to follow this procedure can damage monitor and/or keyboard components.

8.7.8 J1

This connector provides the voltage and video signals to the electronics board. Refer to Section 8.4 for the pin-out and signal descriptions for J1.

8.7.9 J2

This connector provides the horizontal and vertical deflection currents between the electronics board and the yoke assembly. It is a 4-pin connector. Pins 1 and 4 are used for vertical deflection, pins 2 and 3 for horizontal deflection.

8.7.10 P1

This connector mounts on the electronics board that the CRT plugs into. Figure 8-8 shows the pin-out for P1.

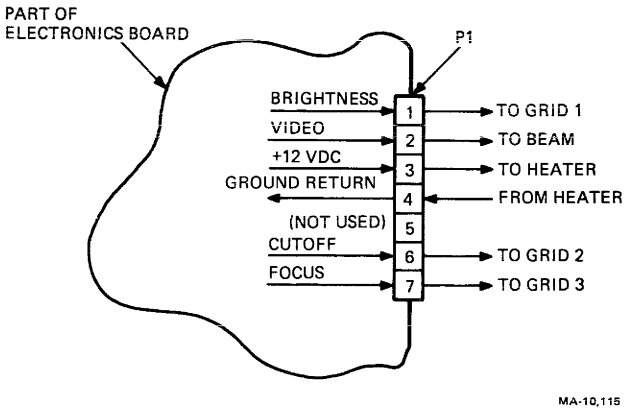


Figure 8-8 Monitor Module P1 Pin-Out

CHAPTER 9
LK201 KEYBOARD

9.1 INTRODUCTION

This chapter describes the LK201 keyboard used on the Professional 300 series of computer system. The shaded part of Figure 9-1 shows its relationship in the system block diagram.

The keyboard is the user interface to the system. It detects keystrokes, encodes them, and transmits the information to the central processor. The keyboard also receives information from the central processor.

Communication between the keyboard and the central processor in the system box is full duplex, serial asynchronous at a speed of 4800 baud. The communication lines conform to EIA Standard RS-423 which applies to unbalanced voltage interfaces.

9.1.1 Related Documentation

Refer to the *LK201 Maintenance Print Set* (MP-01395-00) while reading this chapter.

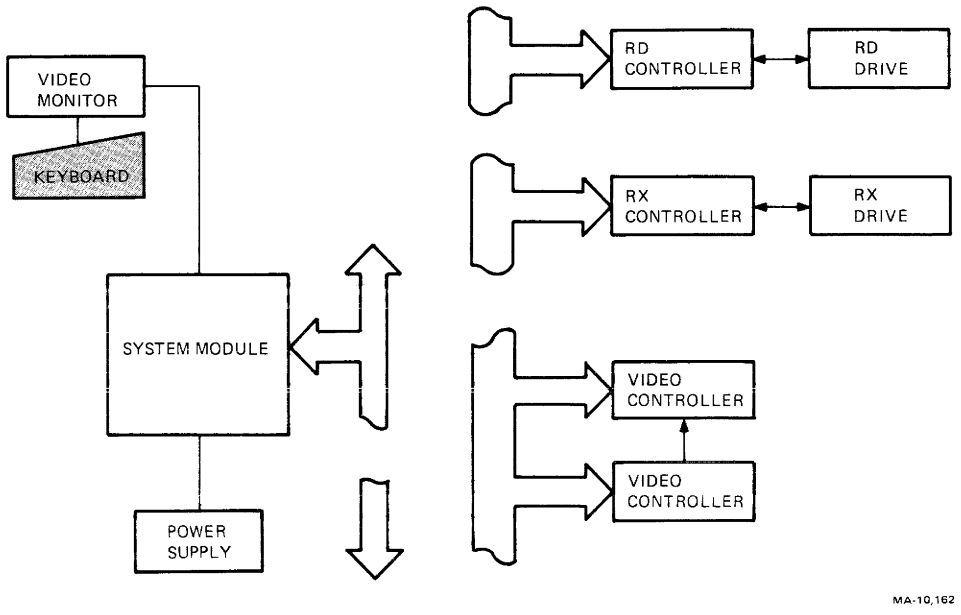


Figure 9-1 System Block Diagram

9.2 PHYSICAL DESCRIPTION

The keyboard used in the Professional 300 Series has 105 keys arranged in the following four groups (Figure 9-2).

Main keypad (57 keys)
Numeric keypad (18 keys)
Special function keypad (20 keys)
Editing keypad (10 keys)

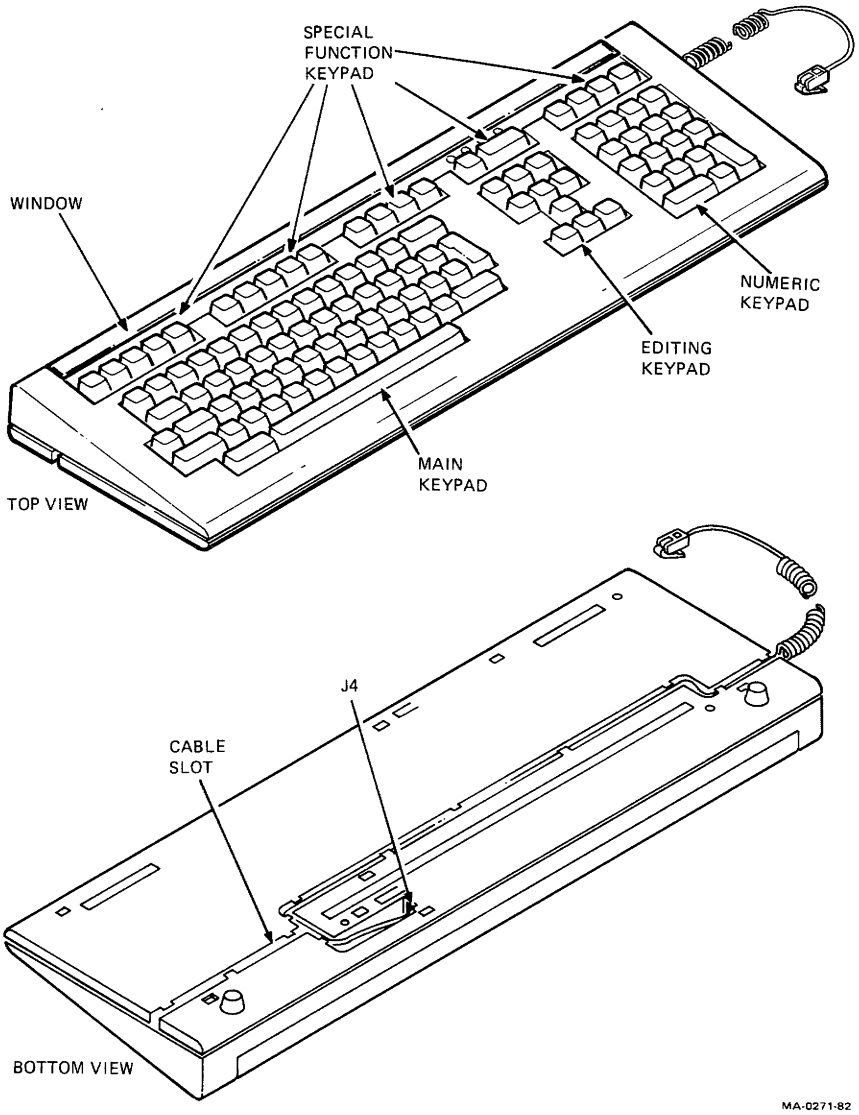


Figure 9-2 LK201 Keyboard

The keycaps can be installed manually, but require a special tool for removal.

The keyboard circuitry is contained in a low profile cabinet that has a 30 mm nominal height from table top to home row. The keyboard case is made of two plastic shells that can be separated with a screwdriver. Non-slip plastic strips along the bottom prevent the keyboard from sliding on a table top. Two feet can be manually inserted in holes to raise the back edge of the keyboard.

A plastic window along the top edge above the special function keys can be lifted to insert a user function label. The label, a thin paper strip, fits into the indented space and varies according to the application program.

A coiled cable (PN BCC01), with a 4-pin modular connector on each end, connects the keyboard to the video monitor. The keyboard transmits four signals to the monitor which pass unchanged to the system box via the video cable (Figure 9-3). The four signals are as follows.

+12 V power to keyboard
ground to keyboard
SERIAL OUT (transmit line from keyboard)
SERIAL IN (receive line to keyboard)

The cable can be placed in a channel in the bottom case and the modular type telephone connector fits into the jack, J4. The cable can be inserted in the channel to either side of the keyboard. Section 9.6 provides the specifications for the keyboard.

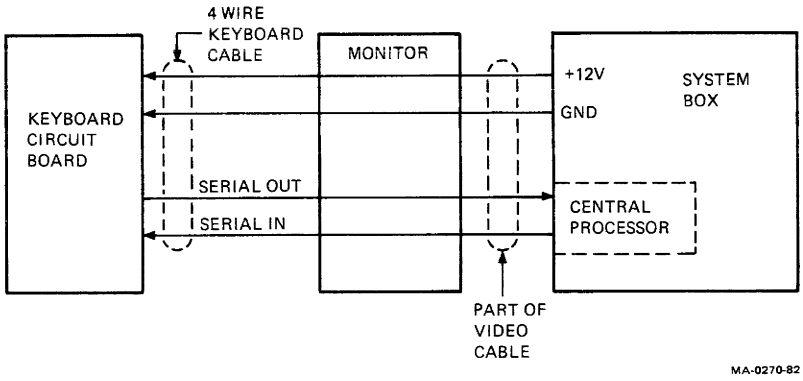


Figure 9-3 Keyboard Cable Connections

9.3 FUNCTIONAL DESCRIPTION

The following sections provide a functional description of the LK201 keyboard.

9.3.1 Overview of Keyboard Operation

Figure 9-4 shows a simplified block diagram of the keyboard circuitry. Everything except the block marked KEYBOARD SWITCH MATRIX is on the printed circuit board. This block represents the connections between the keyboard switches and the signals from the 8051 microprocessor.

The firmware in the 8051 8-bit microprocessor controls three major keyboard operations at the same time.

1. It scans the keyboard to detect changes in the keyboard matrix.
2. It transmits the results of the keyboard scan to the system central processor.
3. It receives information from the system central processor.

9.3.1.1 Keyboard Scanning – The keyboard switches are connected at the intersections of an 18 × 8 line matrix. This provides a fixed position identifier for each key.

The firmware scans the 18-line axis and detects a depressed or newly released key by reading the 8-line axis. The firmware then verifies the detected keystroke and changes this positional information into an 8-bit code that is unique to that key.

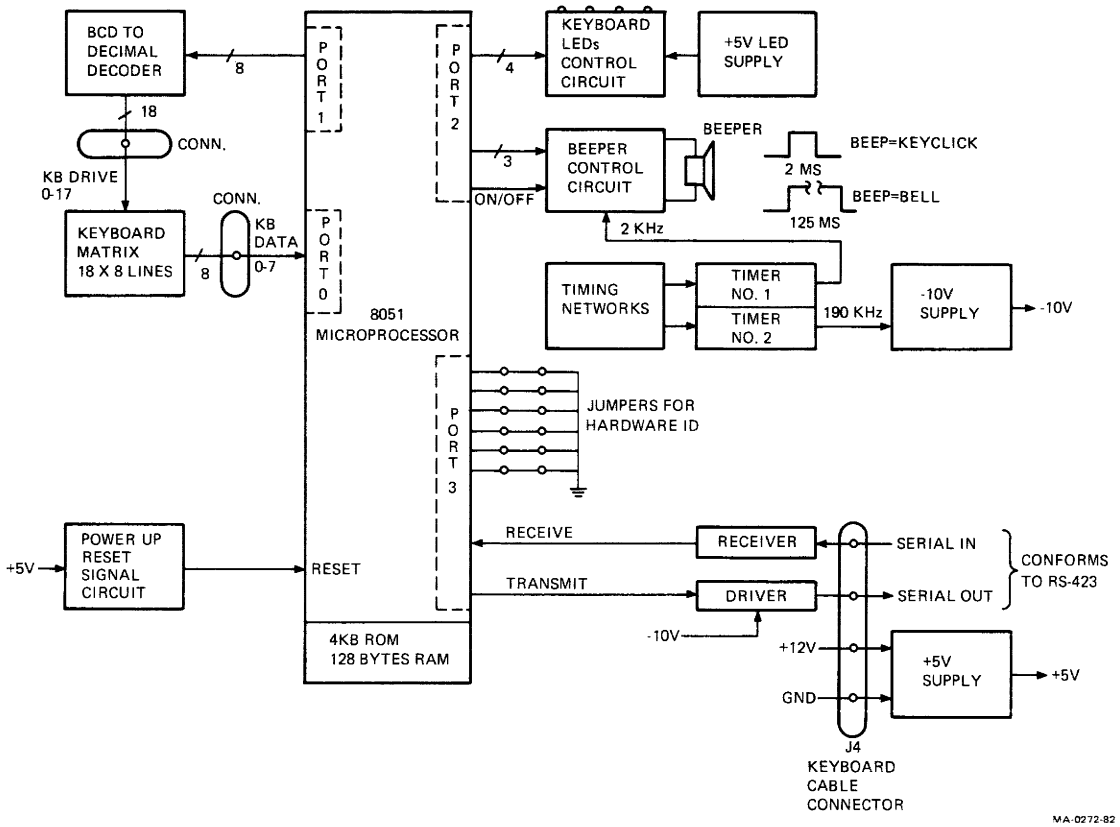


Figure 9-4 Simplified Block Diagram of LK201 Keyboard Circuitry

9.3.1.2 Control of Audio Transducer and Indicators – Two circuits control the audio transducer and the indicators. One circuit receives its inputs from the 8051 and controls the transducer (beeper). A long beep represents the bell and a short beep represents the keyclick.

A separate circuit, controlled by a signal from the 8051, controls each of the four indicators. The firmware, responding to commands received from the system central processor, turns the indicators on or off.

9.3.2 Keyboard Firmware Functions

This section describes the keyboard firmware functions. The functions are divided into two categories: those that cannot be changed by instructions from the system central processor and those that can be changed by instructions from the system central processor.

9.3.2.1 Functions not Changed by System Central Processor Instructions – The following functions cannot be changed by instructions from the system central processor.

Power-up test
Keycodes
Special codes

Power-Up Test

Upon power up, the firmware performs a self-test in less than 70 ms. The test results are transmitted to the system central processor in 4 bytes.

The keyboard indicators light during self-test. The indicators blink once during the self-test routine. The indicators remain lit if the test fails but go off if the test is passed. The system module can also request the self-test at any time.

Keycodes

The keycodes represent fixed positions in the key switch matrix. The key associated with a particular matrix position is always represented by the same keycode.

Special Codes

There are 13 special codes transmitted by the keyboard. Four codes transmit the results of the power-up self-test. The other nine codes are status indicators or command acknowledgements.

9.3.2.2 Functions Changed by System Central Processor Instructions – The system central processor can issue instructions to change some keyboard transmission characteristics and to control the keyboard indicators and beeper.

Upon completion of a successful power-up self-test, the firmware sets certain functions to predetermined conditions. They are referred to as default conditions. The conditions can be changed but they always come up to the default condition after a successful power-up self-test.

9.3.2.3 Firmware Functions that can be Changed – Certain firmware functions can be changed by commands (instructions) from the system central processor. These commands are categorized as transmission commands and peripheral commands. Transmission commands contain a mode set command and an autorepeat rate set command. Peripheral commands contain a variety of commands. Refer to Section 9.5.5.3 for more information on peripheral commands.

9.4 DETAILED KEYBOARD CIRCUIT DESCRIPTION

The following section describes the keyboard circuit. Figure 9-4 shows the LK201 keyboard block diagram.

9.4.1 Keyboard Matrix Scanning

The key locations are arranged in an 18 × 8 line matrix. Each key switch is connected across a matrix intersection. This gives a fixed position for each key connected in the matrix. This matrix accommodates all 105 keys in the LK201 keyboard.

Figure 9-5 is a simplified block diagram of the matrix scanning circuit. Eight lines from PORT 1 of the 8051 microprocessor go to the binary coded decimal (BCD) inputs of two 74LS145 BCD-to-decimal decoders. Ten outputs from one decoder and eight outputs from the other decoder provide the drive lines for the matrix. These 18 lines are called KB DRIVE 0–17.

The other axis of the matrix consists of eight lines tied to +5 V through pull-up resistors. These lines go to PORT 0 of the 8051 microprocessor and are called KB DATA 0–7.

The 8051 scans the 18 drive lines. Key closures are detected by reading the eight data lines. The complete matrix is scanned every 8.33 ms.

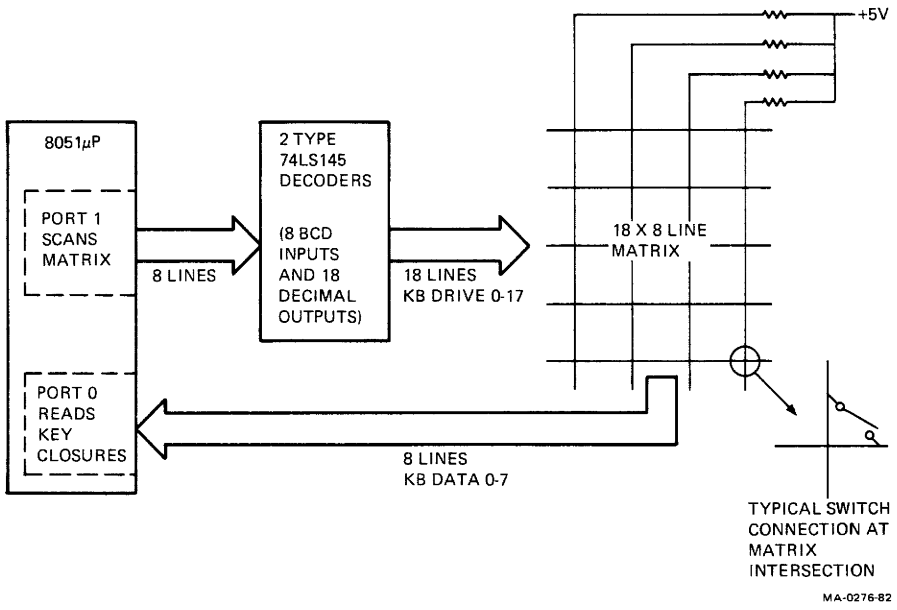


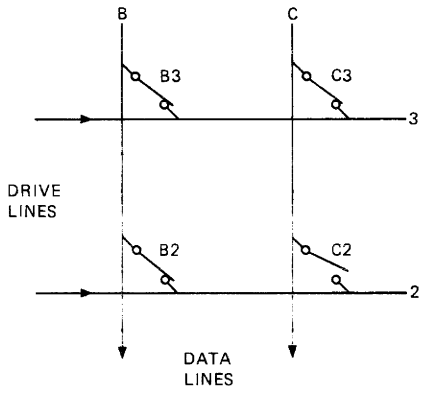
Figure 9-5 Simplified Block Diagram of Matrix Scanning Circuit

When a key closure is detected, it is scanned again to verify that it is really a key closure and not electrical noise.

Once the key closure is verified, the 8051 firmware translates the position information into a key code and transmits it to the system central processor. Transmission is handled by the Universal Asynchronous Receiver Transmitter (UART) in the 8051.

A sneak path or ghost key indication can occur when three of the four corners of a matrix rectangle are closed (Figure 9-6). The key positions in the matrix are arranged to avoid sneak paths. However, if a sneak path does occur, the firmware prevents the keycode for the key (which caused the sneak path) to be transmitted until one of the involved keys is released. This prevents transmission of ghost keys entirely.

Table 9-1 shows the keyboard matrix on the LK201-AA (American) keyboard. Keycap designations are shown for reference only and can be compared to Figures 9-7A and 9-7B.



1. CONDITIONS ARE: SWITCHES B2, B3, AND C3 CLOSED, SWITCH C2 OPEN; LINE 2 IS BEING DRIVEN AND LINE C IS BEING READ.
2. INTERSECTION C2 IS BEING LOOKED AT. IT SHOULD NOT SHOW A KEY CLOSURE BECAUSE SWITCH C2 IS OPEN.
3. HOWEVER A SNEAK PATH IS PRESENT FROM LINE 2 THROUGH SWITCHES B2, B3, AND C3 TO LINE C. A GHOST KEY IS READ AT INTERSECTION C2.

MA-0273-82

Figure 9-6 Example of Ghost Key Generation

Table 9-1 Keyboard Matrix

Refer to Figures 9-7A and 9-7B. They show the international matrix for the LK201 keyboard. The legends provided are from the LK201-AA keyboard and are provided for convenience only.

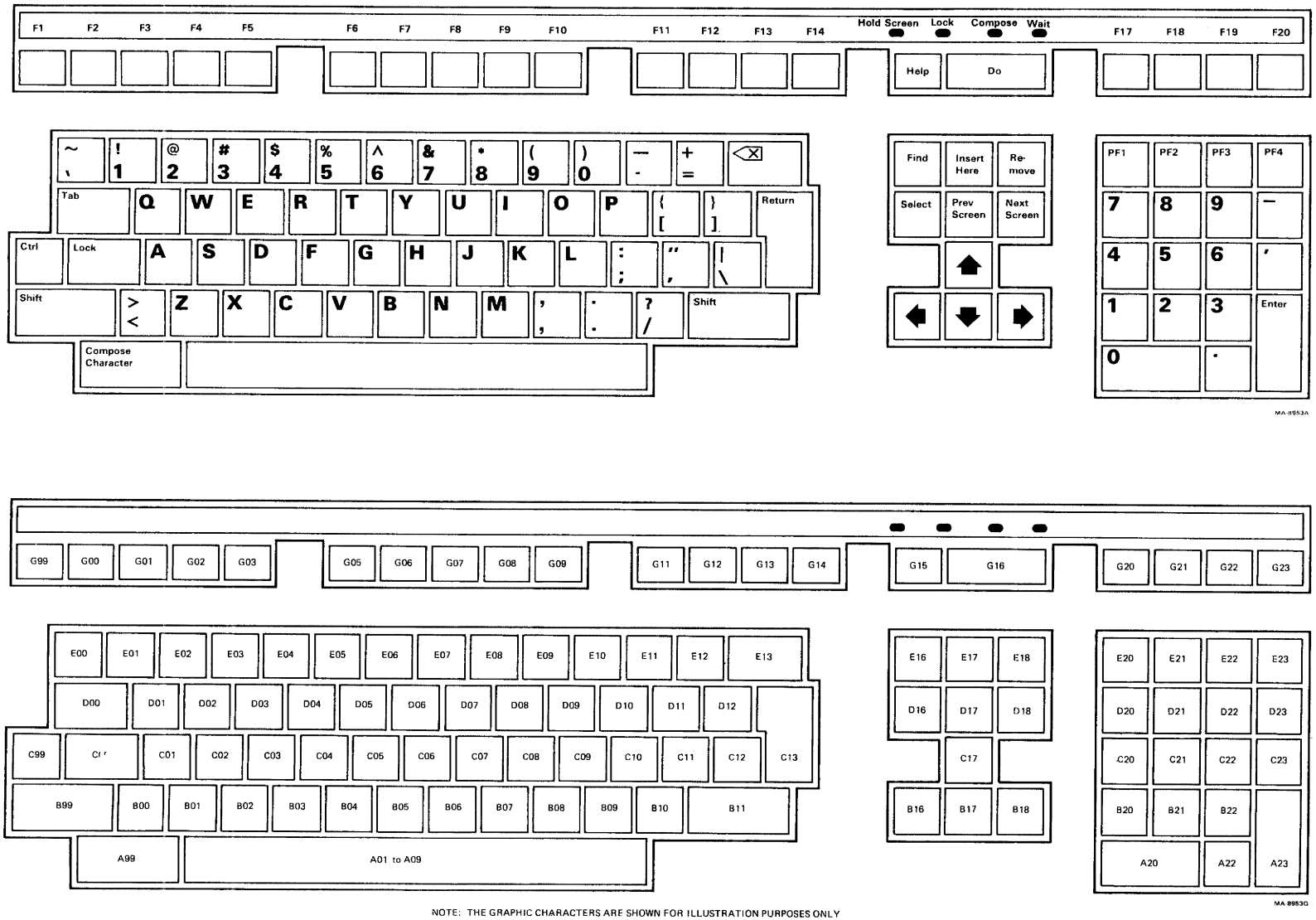
KB DRIVE	KB DATA 7	6	5	4	3	2	1	0
17	Reserved	F19	Reserved	F20	PF4	N_ (Note 1)	N,	ENTER
		G22		G23	E23	D23	C23	A23
16	F18	PF3	Reserved	N9	↓	N6	N3	N.
	G21	E22		D22	B17	C22	B22	A22
15	F17	PF2	Reserved	N8	N5	→	N2	N0 (See
	G20	E21		D21	C21	B18	B21	Note 2)
14	PF1	NEXT SCREEN	REMOVE	↑	N7	N4	N1	N0
	E20	D18	E18	C17	D20	C20	B20	A20
13	INSERT HERE	– -	D0	PREV SCREEN	" [	Reserved	Reserved	
	E17	E11	G16	D17	D11	C11		
12	FIND	+ =	HELP	SELECT	]	RETURN	←	
	E16	E12	G15	D16	D12	C13	B16	C12
11	ADDTNL OPTIONS	X (delete)	Reserved	) 0	P	See Note 3	: ;	? /
	G14	E13		E10	D10		C10	B10
10	Reserved	F12	Reserved	F13	(9	O	L	. .
		G12		G13	E09	D09	C09	B09
9	Reserved	F11	Reserved	Reserved	* 8	I	K	, ,
		G11			E08	D08	C08	B08
8	Reserved	MAIN SCREEN	Reserved	EXIT	& 7	U	J	M
		G08		G09	E07	D07	C07	B07

Table 9-1 Keyboard Matrix (Cont)

KB DRIVE	KB DATA 7	6	5	4	3	2	1	0
7	Reserved	CANCEL	Reserved	RESUME	^ 6	Y	H	N
		G07		G06	E06	D06	C06	B06
6	Reserved	Reserved	Reserved	INTER-RUPT	% 5	T	G	B
				G05	E05	D05	C05	B05
5	SETUP	F5	Reserved	$ 4	R	F	V	SPACE
	G02	G03		E04	D04	C04	B04	A01–A09
4	Reserved	PRINT SCREEN	Reserved	BREAK	# 3	E	D	C
		G00		G01	E03	D03	C03	B03
3	HOLD SCREEN	@ 2	Reserved	TAB	W	S	X	> <
	G99	E02		D00	D02	C02	B02	B00
2	Reserved	Reserved	Reserved	~	! 1	Q	A	Z
				E00	E01	D01	C01	B01
1	CTRL	LOCK	COMPOSE	Reserved				
	C99	C00	A99					
0	SHIFT							
	B99,B11							

NOTES:

1. **Note that N0 – N9, N__, N,, and N. refer to the numeric keypad.**
2. **N0 of the numeric keypad can be divided into two keys. Normally only the N0 keyswitch is implemented as a double size key.**
3. **The RETURN key also can be divided into two keys. The one which is decoded as return is the RETURN (C13) key.**



NOTE: THE GRAPHIC CHARACTERS ARE SHOWN FOR ILLUSTRATION PURPOSES ONLY AND ARE NOT MEANT TO ASSIGN KEYCAP USAGE OR LEGENDS.

Figure 9-7 LK201-AA Keyboard Layout

9.4.2 Audio Transducer Control Circuit

Figure 9-8 shows the audio transducer or beeper control circuit. The beeper is driven by a transistor whose base is connected to a 2 kHz square wave from a 556 timer IC. This signal is biased by a network of four type 74LS05 open collector inverters. The 8051 microprocessor controls all four inverters via the firmware. The on/off inverter connects directly to the transistor base. When the 8051 puts a high on the on/off inverter input, its output goes low and removes the 2 kHz square wave from the transistor base. This cuts off the transistor and disables the beeper.

To turn on the beeper, the 8051 puts a low on the on/off inverter input. Its output goes high and allows the 2 kHz signal to reach the transistor base. This turns on the beeper. The firmware generates a keyclick (on for 2 ms) or a bell tone (on for 125 ms). The 8051 sets up the three level control inverters by putting one of eight binary combinations on the inverter inputs. All highs give the softest sound and all lows give the loudest sound.

The firmware controls the keyclick and the bell tone independently. The bell tone is sounded only upon request from the system control processor. The keyclick is sounded (unless disabled) under the following three conditions.

1. When a key is depressed
2. When a metronome code is sent
3. When a command to sound the keyclick is received from the system control processor

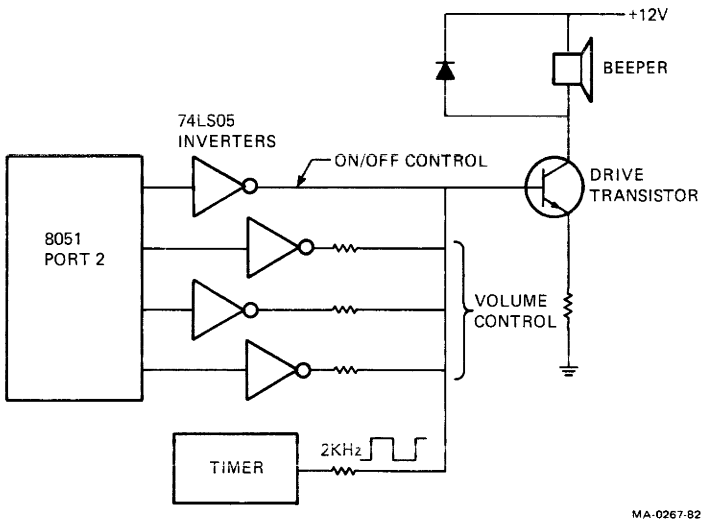


Figure 9-8 Beeper Control Circuit

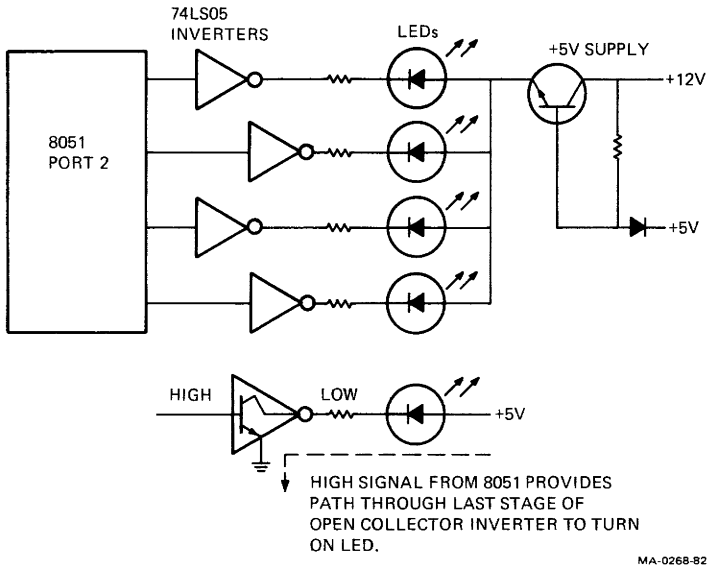


Figure 9-9 Indicator (LED) Control Circuit

9.4.3 Indicator (LED) Control Circuit

Figure 9-9 shows the LED indicator control circuit.

The control signal for each LED comes from PORT 2 of the 8051 to the input of a type 74LS05 open collector inverter. The inverter output goes to the LED cathode. Its anode is connected to +5 V. A separate +5 V source relieves the LEDs load on the main +5 V supply.

A low signal from the 8051 drives the inverter output high which cuts off the LED. A high signal from the 8051 drives the inverter output low. This provides a path to ground from the +5 V through the LED. The LED then turns on.

9.4.4 Keyboard Communication

The following sections describe the keyboard communication.

9.4.4.1 Keyboard Transmit Mode – The keyboard codes and a few other special codes are transmitted via a serial line output in PORT 3 of the 8051. The transmitted signal goes from the 8051 to a driver, through the keyboard cable, monitor, and video cable to the system central processor. A UART within the 8051 controls the transmission.

Transmitted characters conform to a specific format. Each character is 10 bits long. The first bit is the START bit. It is always a logical 0 (space). The next eight bits represent the encoded data. The last bit is the STOP bit. It is always a logical 1 (mark). Figure 9-10 shows the character format.

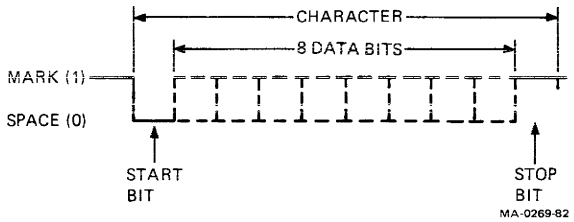


Figure 9-10 Keyboard Transmit and Receive Character Format

9.4.4.2 Keyboard Receive Mode – The firmware contains features that can be enabled by commands from the system central processor. There are two categories of features: one sets keyboard transmission characteristics and the other controls the keyboard peripherals. A peripheral command covers indicator control, bell and keyclick loudness, keyboard ID code, and reinstate keyboard. The commands come from the system central processor, through the video cable, monitor, and keyboard cable to the receiver and into the 8051 via PORT 3. They go to the UART in the 8051.

Received characters conform to the same 10-bit format used for transmitted characters. The 8 data bits are arranged in a specified protocol depending on the command type.

9.4.5 Reset Signal for 8051 Microprocessor

Whenever the system is turned on, the 8051 microprocessor in the keyboard must be reset. This allows the 8051 to start operating.

The reset signal generator is active only during the power-up sequence. The input is +5 V. The output is connected to the RESET input of the 8051. When power is turned on, the +5 voltage starts to rise from 0. The reset signal circuit output follows it and drops off when a steady state of +5 V is reached. This circuit holds the 8051 RESET input high (+3.5 V to +5 V) long enough to enable the reset action in the 8051. This action occurs only during powerup.

9.4.6 Hardware Keyboard Identification (ID)

At power up, the keyboard performs a self-test and sends the results to the system central processor. One piece of information to be sent is the keyboard hardware ID which is read from hardwired jumpers.

There are six jumpers. Each jumper line goes from an input in PORT 3 of the 8051 to ground. All jumpers are installed so the keyboard hardware ID is 0.

9.4.7 Voltage Supplies

The only voltage sent to the keyboard is +12 V. However, +5 V and −10 V are also required. These voltages are derived from the +12 V.

There is a +5 V supply that handles most of the requirements for this voltage. The four keyboard LEDs have their own +5 V supply. A −10 V supply provides voltage for the driver in the SERIAL OUT line.

9.5 KEYBOARD PROGRAMMING

This section describes the functions that the keyboard performs under system central processor control. It also describes keyboard programming machine language. High level user programming is not described here.

9.5.1 Keyboard Layout and Key Identification

Each keyboard key has a unique location. Each location is scanned, and when closure or release is detected, the location is verified. This is then decoded to an 8-bit keycode. Figure 9-7 shows the keyswitch locations. Table 9-2 shows the 14 functional divisions of the keyboard. Table 9-3 shows the divisions, keycaps, and keycodes.

Table 9-2 Keyboard Functional Divisions

Division	Description	Representation
1	48 graphic keys, spacebar	0001
2	Numeric keypad	0010
3	Delete Character (E12)	0011
4	Return (C13) Tab (D00)	0100
5	Lock (C00) Compose (A99)	0101
6	Shift (B99 and B11), Ctrl (C99)	0110
7	Horizontal cursors (B16 and B18)	0111
8	Vertical cursors (B17 and C17)	1000
9	Six keys directly above the cursor keys (D16–D18 and E16–E18)	1001
10	Function keys (G99–G03)	1010
11	Function keys (G05–GO9)	1011
12	Function keys (G11–G14)	1100
13	Function keys (G15–G16)	1101
14	Function keys (G20–G23)	1110

Table 9-3 Keycode Translation Table

Division	Position	Keycap	Keycode (dec)	Keycode (hex)
Function Keys				
10	G99	Hold screen	086	56
	G00	Print screen	087	57
	G01	Break	088	58
	G02	Setup	089	59
	G03	F5	090	5A
		Reserved	091–098	5B–62
11		Reserved	099	63
	G05	Interrupt	100	64
	G06	Resume	101	65
	G07	Cancel	102	66
	G08	Main screen	103	67
	G09	Exit	104	68
		Reserved	105–110	69–6E
12			111	6F
		Reserved	112	70
	G11	F11 (ESC)	113	71
	G12	F12 (BS)	114	72
	G13	F13 (LF)	115	73
	G14	Addtnl opt's	116	74
		Reserved	117–122	75–7A
13		Reserved	123	7B
	G15	Help	124	7C
	G16	D0	125	7D
14		Reserved	126–127	7E–7F
	G20	F17	128	80
	G21	F18	129	81
	G22	F19	130	82
	G23	F20	131	83
		Reserved	132–135	84–87
6 Basic Editing Keys				
9		Reserved	136–137	88–89
	E16	Find	138	8A
	E17	Insert here	139	8B
	E18	Remove	140	8C
	D16	Select	141	8D
	D17	Prev screen	142	8E
	D18	Next screen	143	8F
		Reserved	144	90

Table 9-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode (dec)	Keycode (hex)
Keypad				
2		Reserved	145	91
	A20	0	146	92
		Reserved	147	93
	A22	.	148	94
	A23	Enter	149	95
	B20	1	150	96
	B21	2	151	97
	B22	3	152	98
	C20	4	153	99
	C21	5	154	9A
	C22	6	155	9B
	C23	,	156	9C
	D20	7	157	9D
	D21	8	158	9E
	D22	9	159	9F
	D23	-	160	A0
	E20	PF1	161	A1
	E21	PF2	162	A2
	E22	PF3	163	A3
	E23	PF4	164	A4
		Reserved	165	A5
Cursor Keys				
7		Reserved	166	A6
	B16	Left	167	A7
	B18	Right	168	A8
8	B17	Down	169	A9
	C17	Up	170	AA
		Reserved	171–172	AB–AC
Shift, Lock CTRL, A99 and A10				
6		Reserved	173	AD
	B99,B11	Shift	174	AE
	C99	CTRL	175	AF
5	C00	Lock	176	B0
	A99	Compose	177	B1
		Reserved	178	B2

Table 9-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode (dec)	Keycode (hex)
Special Codes				
		All Ups	179	B3
		Metronome	180	B4
		Output error	181	B5
		Input error	182	B6
		KBD LOCKED acknowledge	183	B7
		TEST MODE acknowledge	184	B8
		PREFIX to keys down	185	B9
		MODE CHANGE acknowledge	186	BA
		Reserved	187	BB
Delete				
3	E13	Delete (X)	188	BC
Return and Tab				
4	C13	Return	189	BD
	D00	Tab	190	BE
48 Graphics Keys and Space Bar				
1	E00	Tilde	191	BF
	E01	!1	192	D0
	D01	Q	193	C1
	C01	A	194	C2
	B01	Z	195	C3
		Reserved	196	C4
	E02	@2	197	C5
	D02	W	198	C6
	C02	S	199	C7
	B02	X	200	C8
	B00	><	201	C9
		Reserved	202	CA
	E03	#3	203	CB
	D03	E	204	CC
	C03	D	205	CD
	B03	C	206	CE
		Reserved	207	CF
	E04	$4	208	D0
	D04	R	209	D1
	C04	F	210	D2
	B04	V	211	D3

Table 9-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode (dec)	Keycode (hex)
	A01–A09	Space	212	D4
		Reserved	213	D5
	E05	%5	214	D6
	D05	T	215	D7
	C05	G	216	D8
	B05	B	217	D9
		Reserved	218	DA
	E06	•6	219	DB
	D06	Y	220	DC
	C06	H	221	DD
	B06	N	222	DE
		Reserved	223	DF
	E07	&7	224	E0
	D07	U	225	E1
	C07	J	226	E2
	B07	M	227	E3
		Reserved	228	E4
	C08	*8	229	E5
	D08	I	230	E6
	C08	K	231	E7
	B08	“”	232	E8
		Reserved	233	E9
	E09	(9	234	EA
	D09	0	235	EB
	C09	L	236	EC
	B09	. .	237	ED
		Reserved	238	EE
	E10	)0	239	EF
	D10	P	240	F0
		Reserved	241	F1
	C10	: ;	242	F2
	B10	? /	243	F3
		Reserved	244	F4
	E12	+ =	245	F5
	D12	} }]	246	F6
	C12	| \	247	F7
		Reserved	248	F8
	E11	__ -	249	F9
	D11	{ [	250	FA
	C11	. ,	251	FB
		Reserved	252–255	FC–FF

NOTE
The legends under “keycap” are taken from the keycap legends of the LK201-AA (American).

Keycodes 00 through 64 are reserved. Keycodes 65 through 85 are unused.

9.5.2 Modes

This section describes the function of the keycode transmission modes. The mode set command allows any one of the 14 keyboard divisions to be set to any one of the following three modes. (Refer to Section 9.5.7 for division defaults.)

1. **Down-only mode** – The keyboard transmits a keycode when the key is depressed.

2. **Autorepeat** – The keyboard transmits a keycode when the key is first depressed. If the key is held down past the specified timeout period (usually 300 to 500 ms), a fixed metronome code is sent at the specified rate until the key is released.

3. **Down/Up** – The keyboard transmits a keycode when the key is depressed and an "up code" when the key is released. If any other keys are depressed, the "up code" is a repeat of the "down code." If no other keys are depressed, the keyboard sends an ALL UPS code.

9.5.2.1 Special Considerations Regarding Autorepeat – The Autorepeat Rate Set command allows the following changes in the autorepeat mode.

1. Autorepeat rate buffer association – The buffer association can be changed for the selected keyboard division.

2. The timeout and interval values can be changed in any one of the four autorepeat rate buffers.

3. If multiple autorepeating keys are held down, metronome codes are still generated. The metronome codes apply to the keycode transmitted most recently. If the last key pressed down is released, and other key(s) is (are) still down, the keycode(s) of the key(s) still down is (are) retransmitted.

Example: The **a** key is held down.

This produces the following transmission.

a metronome metronome

Now the **b** key is depressed. This produces the following transmission.

a metronome metronome b metronome metronome

Now the **b** key is released. This produces the following transmission.

a metronome metronome b metronome metronome a metronome met . . .

While metronome codes are being generated for an autorepeating key, a non-autorepeating keycode or special code may be transmitted. The keyboard transmits this special code instead of the next metronome code and then returns to the autorepeated code. The keycode to be autorepeated is always the last byte transmitted.

Example: The **a** key is held down.

This produces the following transmission.

a metronome metronome

Now the **Shift** key is depressed. This produces the following transmission.

a metronome metronome shift a metronome

Now the **Shift** key is released. This produces the following transmission.

a metronome metronome shift a metronome ALL UPS a metronome . . .

If an autorepeating key is not to autorepeat (for example, **Ctrl C**), the system module must issue a Temporary Inhibit Autorepeat command. This halts the transmission of any metronome codes or keyclicks for that key only. Metronome codes continue when another key is depressed. The command must be issued after the keycode for the autorepeating key is received.

Autorepeat can be enabled and disabled independently of the division settings by using the Enable/Disable Autorepeat commands. These commands apply to all keys on the keyboard. When autorepeat is disabled, internally the keyboard continues to autorepeat characters. However, it does not transmit metronome codes or keyclicks. When autorepeat is enabled, the keyboard transmits the metronome codes from the point they were before autorepeat was disabled. This may be within either the timeout or interval period, depending upon the time elapsed since key depression.

If the keyboard receives a request to change a division mode to autorepeat while a key is depressed, the keyboard makes the change immediately. After the specified timeout period, the keyboard transmits metronome codes for the depressed key. In place of the first metronome code, the keyboard transmits the keycode of the autorepeating key.

All autorepeating division modes can be changed to down only with one command. This and other autorepeat commands are grouped with the peripheral commands (Section 9.5.5.3).

9.5.2.2 Special Considerations Regarding Down/Up Mode – If two keys are released simultaneously (within the same scan), and there are no other keys pressed on the keyboard, only one ALL UPS code is generated.

9.5.2.3 Autorepeat Rates – There are four buffers in the keyboard to store autorepeat rates. They are numbered 0 through 3. Each buffer stores the following two values. These values can be changed by the system module.

1. Timeout value
2. Interval value

The timeout value is the amount of time between the detection of a down key and the transmission of the first metronome code (defaults range from 300 to 500 ms). The interval value is the number of metronome codes per second (defaults to 30).

Each division is associated with one of the four buffers. Rates are taken from the associated buffer each time the autorepeat timers are loaded. This buffer-to-division association can be changed by the system module or left to default.

9.5.3 Keyboard Peripherals

This section describes the peripherals available on the keyboard. The keyclick, bell, and LEDs are all considered keyboard peripherals. Refer to Section 9.5.5.3 for information on system module control of these peripherals.

9.5.3.1 Audio – The keyclick is a 2 ms beep and the bell is a 125 ms beep. The bell is sounded only upon request from the system module. The keyclick (if not disabled by the system module) is sounded under the following three conditions.

1. When a key is depressed
2. When a metronome code is sent
3. When the system module receives a sound keyclick command.

If either the **B11** or **B99** keys (the left and right **Shift** keys on the LK201) or the **C99** key (the **Ctrl** key on the LK201) are depressed, the keyclick is not generated. However, if a command is sent from the system module to enable the keyclick on the **C99** key, the keyclick is generated (Section 9.5.5.3). Figure 9-7 shows the positions of these keys.

The keyclick or bell (or both) may be disabled. When the keyclick or bell is disabled, it does not sound. If the system module requests sound (Section 9.5.5.3), the keyclick or the bell does not sound.

Both the keyclick and bell may be set independently to one of the following eight volume levels.

000 – highest
001
010 – default
011
100
101
110
111 – lowest

9.5.3.2 Indicators (LEDs) – The system module normally transmits indicator control commands. However the following are exceptions.

1. Upon power up, the keyboard turns all LEDs off.

2. After receiving the Inhibit Transmission command, the keyboard turns on the keyboard locked LED. The LED is turned off after the keyboard receives a Resume Transmission command.

9.5.4 Keyboard-to-System Module Protocol

The following paragraphs describe the keyboard-to-system module protocol.

9.5.4.1 Keycode Transmission – The keyboard transmits single byte keycodes that reflect the keyboard matrix status. The 8-bit codes above 64_{10} are used for keycodes. Every key is identified by a unique keycode. There are no special codes for shifted or control keys.

NOTE
Keycodes 00_{10}–64_{10} are reserved. Refer to Table 9-3 for keycode translation.

Refer to Figure 9-7 and Tables 9-1 and 9-2 for the complete keycode matrix translation table.

9.5.4.2 Special Code Transmission – There are 13 special codes: nine codes with values above 64_{10} and four codes below.

The following are the nine special codes above 64_{10} (keycode value range).

ALL UPS	Keycode 179 (dec), B3 (hex)
METRONOME CODE	Keycode 180 (dec), B4 (hex)
OUTPUT ERROR	keycode 181 (dec), B5 (hex)
INPUT ERROR	Keycode 182 (dec), B6 (hex)
KBD LOCKED ACK	Keycode 183 (dec), B7 (hex)
TEST MODE ACK	Keycode 184 (dec), B8 (hex)
PREFIX TO KEYS DOWN	Keycode 185 (dec), B9 (hex)
MODE CHANGE ACK	Keycode 186 (dec), BA (hex)
RESERVED	Keycode 127 (dec), 7F (hex)

ALL UPS – indicates to the system module that a key was just released and no other keys are depressed.

METRONOME CODE – indicates to the system module that an interval has passed, a keyclick has been generated, and the last key received by the system module is still depressed.

OUTPUT ERROR – indicates an output buffer overflow to the system module. The overflow occurred after receiving a Keyboard Inhibit command from the system module and, as a result, some keystrokes may be lost.

INPUT ERROR CODE – indicates to the system module that the keyboard received a meaningless command or one with too many or too few parameters.

KEYBOARD LOCKED CONFIRMATION – indicates to the system module that the keyboard received an Inhibit Transmission command (Section 9.5.5.3).

TEST MODE ACKNOWLEDGE – indicates that the keyboard has entered test mode. This is a special mode used during the production test. If the system module receives this acknowledge, it sends 80 hex. This terminates the test mode and jumps to power up.

PREFIX TO KEYS DOWN – indicates that the next byte is a keycode for a key already down in a division which has been changed to Down/Up (Section 9.5.5.4).

MODE CHANGE ACKNOWLEDGE – indicates that the keyboard has received and processed a mode change command (Section 9.5.5.4).

RESERVED – keycode 7F is reserved for internal use.

The following four special codes are below 64_{10} value range.

KEYBOARD ID - FIRMWARE	Keycode 01 (dec), 01 (hex)
KEYBOARD ID - HARDWARE	Keycode 00 (dec), 00 (hex)
KEY DOWN ON POWER UP ERROR CODE	Keycode 61 (dec), 3D (hex)
POWER UP SELF-TEST ERROR CODE	Keycode 62 (dec), 3E (hex)

KEYBOARD ID - This is a 2 byte identification code, transmitted after the power-up self-test (Section 9.5.4.3). It is also sent on request from the system module (Section 9.5.5.3).

KEY DOWN ON POWER UP ERROR CODE - indicates that a key was depressed on power up.

POWER UP SELF-TEST ERROR CODE - indicates to the system module that the ROM or RAM self-test of the system module failed (Section 9.5.4.3).

9.5.4.3 Power Up Transmission - Upon power up, the keyboard performs a self-test in less than 70 ms. It transmits the self-test results to the system module in 4 bytes.

Byte 1	KBID (firmware) - This is the keyboard identification (ID) that is stored in the firmware.
Byte 2	KBID (hardware) - This is the keyboard ID that is read from hardware jumpers.
Byte 3	ERROR - Two error codes indicate either failure of the ROM or RAM self-test within the processor (3E hex), or keydown on power up (3D hex). No error is indicated by 00.
Byte 4	KEYCODE - This byte contains the first keycode detected if there was a key down on power up. No error is indicated by 00.

If the ROM self-test (CHECKSUM) fails and the error is critical, the keyboard is unable to transmit. Noncritical errors permit the keyboard to continue operation.

If the keyboard finds a key down on the first scan, it continues to look for an ALL UP condition. The keyboard sends the corrected 4-byte power-up sequence when the depressed key is released. This avoids a fatal error condition if a key is pressed by mistake while powering up.

The keyboard LEDs light during the power-up self-test. If the self-test passes, the keyboard turns the LEDs off. If a bell is selected on power up, the system module can transmit a Sound Bell command to the keyboard. However, this should not be done until the system module receives the last byte of the 4-byte sequence. The request for self-test tests the serial line and system module connection. The power-up self-test takes 70 ms or less.

The system module can request a jump to power up at any time. This causes the LEDs on the keyboard to blink on and off (for the power-up self-test).

9.5.5 System Module to Keyboard Protocol

The system module controls both the peripherals associated with the keyboard and the keyboard transmit characteristics. Figure 9-11 shows the protocol for the transmission of commands and parameters from the system module to the keyboard.

9.5.5.1 Commands – There are two kinds of commands: those that control keyboard transmission characteristics and those that control keyboard peripherals. The low bit of the command is the TYPE flag. It is clear if the command is a *transmission* command. It is set if the command is a *peripheral* command.

Transmission Commands	**Peripheral Commands**
Mode set	Flow control
Autorepeat rate set	Indicator
	Audio
	Keyboard ID
	Reinitiate keyboard
	Some autorepeat control
	Jump to test mode
	Reinstate defaults

The high order bit of every command is the PARAMS flag. If there are any parameters to follow, this flag is clear. If there are no parameters, this flag is set.

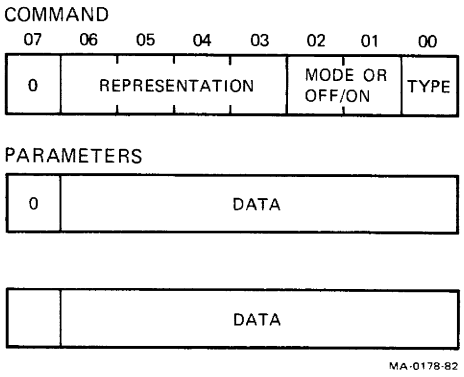


Figure 9-11 System Module to Keyboard Protocol

9.5.5.2 Parameters – The high order bit of every parameter is the PARAMS flag. It is clear if there are parameters to follow. It is set on the last parameter. The remaining seven bits of the parameter are for data.

9.5.5.3 Peripheral Commands – Two commands can turn the data flow from the keyboard off and on.

1. **Inhibit Keyboard Transmission** – This command shuts off or locks the keyboard and turns on the Keyboard Locked LED. After receiving the Inhibit command, the keyboard sends a special command to the system central processor. If the system central processor receives this code without requesting it, this indicates that noise on the line was interpreted as the Inhibit command. The central processor then responds immediately with the Resume Keyboard Transmission command.

2. **Resume Keyboard Transmission** – This command turns on or unlocks the keyboard and turns off the Keyboard Locked LED. If any keystrokes are lost, the keyboard responds with an error code.

Each keyboard LED can be turned on and off.

Eight commands control the keyclick and bell sounds.

Disable Keyclick
Enable Keyclick and Set Volume
Disable Ctrl Keyclick
Enable Ctrl Keyclick
Sound Keyclick
Disable Bell
Enable Bell and Set Volume
Sound Bell

The following four commands are related to the control of the autorepeat mode.

1. **Temporary Autorepeat Inhibit** – Autorepeat is stopped for a specific key only. It resumes automatically when another key is depressed.

2. **Enable Autorepeat Across the Board** – This command starts transmission of metronome codes without affecting autorepeat timing or keyboard division.

3. **Disable Autorepeat Across the Board** – This command stops transmission of metronome codes without affecting autorepeat timing or keyboard division.

4. **Change All Autorepeat to Down Only** – This command changes all keyboard autorepeating divisions to down-only mode.

The following are three other miscellaneous commands.

1. **Request Keyboard ID** – The keyboard sends the two byte ID (firmware and hardware). The keyboard does not jump to the power-up sequence.

2. **Reinitiate Keyboard** – The keyboard jumps to the power-up sequence. Transmission to the keyboard should be held until the host processor receives the last byte of the power-up self-test.

3. **Reinstate Defaults** – This sets the following functions back to the default settings after a successful completion of the power-up self-test.

   Division mode settings
   Autorepeat interval and timeout rates
   Autorepeat buffer selections
   Audio volume
   Control key keyclick

To send a peripheral command, set the TYPE flag (low order bit). Bits 6–3 contain a COMMAND representation from the chart below. Bits 2 and 1 specify on (01), off (00), or sound (11). Bit 7 should be set if there are no parameters to follow.

See Table 9-4 for the peripheral commands (in hex).

Command	**Representation**
Flow Control	0001
Indicator (LEDs)	0010
Keyclick	0011
Bell	0100
Keyboard ID	0101
Keyclick For Ctrl Key	0111
Temporarily Inhibit Autorepeat	1000
Jump to Test Mode	1001
Change All Autorepeat Characters To Down-Only	1010
Enable/Disable Autorepeat	1100

The Jump To Power-Up command is FD hex.

The following are some of the peripheral commands.

1. **Flow Control** – The system module can lock the keyboard with the Inhibit Keyboard Transmission command. When the keyboard is unlocked, it responds with an error code if any keystrokes were missed (Section 9.5.6.2).

2. **Indicators (LEDs)** – Figure 9-12 shows the LED parameter. Figure 9-13 shows the LED layout on the LK201 keyboard.

3. **Audio** – Figure 9-14 shows the audio volume parameter.

Table 9-4 Peripheral Commands in Hex

Function	Hex	Parameters
Flow control		
Resume keyboard transmission	8B	None
Inhibit keyboard transmission	89	None
Indicators		
Light LEDs	13	Bit pattern
Turn off LEDs	11	Bit pattern
Audio		
Disable keyclick	99	None
Enable click, set volume	1B	Volume
Disable Ctrl keyclock	B9	None
Enable Ctrl keyclick	BB	None
Sound keyclick	9F	None
Disable bell	A1	None
Enable bell, set volume	23	Volume
Sound bell	A7	None
Autorepeat		
Temporary autorepeat inhibit	C1	None
Enable autorepeat across keyboard	E3	None
Disable autorepeat across keyboard	E1	None
Change all autorepeat to down only	D9	None
Other		
Request keyboard ID	AB	None
Jump to power-up	FD	None
Jump to test mode	CB	None
Reinstate defaults	D3	None

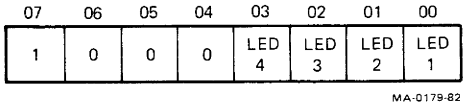


Figure 9-12 Indicator (LED) Parameter

Figure 9-13 Indicator (LED) Layout

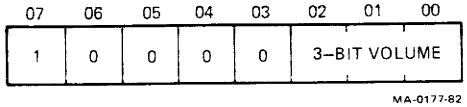


Figure 9-14 Audio Volume Parameter

The volume levels for the audio are as follows.

000 – highest
001
010
011
100
101
110
111 – lowest

Either keyclick or bell (or both) can be disabled. When the keyclick or bell is disabled, it does not sound, even if the system module requests it.

The following are additional peripheral commands.

1. **Temporary Autorepeat Inhibit** – This stops autorepeat for this key only. Autorepeat automatically continues when another key is depressed.

2. **Disable/enable Autorepeat Across Keyboard** – This stop(s)/start(s) transmission of metronome codes without affecting autorepeat timing or division settings

3. **Change All Autorepeat To Down Only** – This changes division settings for all autorepeating divisions to down only

4. **Request Keyboard ID** – The keyboard sends a 2-byte keyboard ID. Keyboard does not jump to power up.

5. **Reinitiate Keyboard** – The keyboard jumps to its power-up routine. The system module should not try to transmit anything to the keyboard until the last byte of the power-up sequence is received.

6. **Jump To Test Mode** – This is a special test mode for the production test.

7. **Reinstate Defaults** – These set the following functions back to the default settings after a successful completion of the power-up self-test.

   Division mode settings
   Autorepeat interval and timeout rates
   Autorepeat buffer selections
   Audio volume
   Control key keyclick

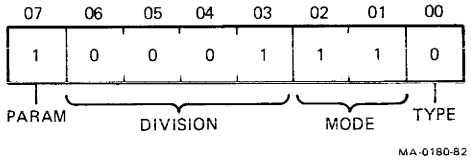
9.5.5.4 Mode Set Commands – The following describe the mode set commands.

Division mode settings – Refer to Section 9.5.2 for an explanation of transmission modes and rates. Each division on the keyboard has a unique 4-bit representation (Section 9.5.1). Table 9-2 describes these representations.

Modes	**Representation**
Down-only	00
Autorepeat	01
Down/Up	11

To set the key transmission mode on a particular keyboard division, the system module must send the PARAMS flag, then the keyboard division representation with the mode code, and then followed by the TYPE flag (cleared).

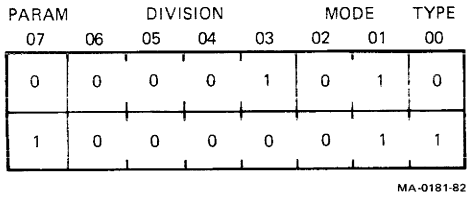
Example: Set main array to Down/Up.



The PARAMS flag is set to 1 if there are no parameters. The PARAMS flag is clear if there are parameters.

Autorepeat Rate Buffer Association – If the autorepeat mode is selected, the system module can transmit a parameter to change the buffer association of the selected division. Refer to Section 9.5.2.3 for autorepeat rates and Section 9.5.7 for default values.

Example: Set main array to autorepeat, change buffer association to buffer 3.

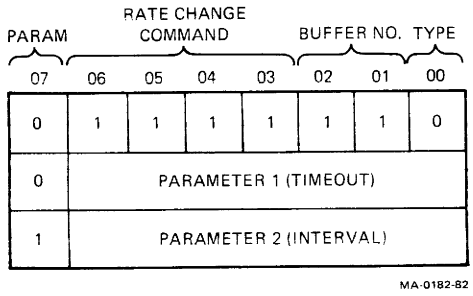


Autorepeat Rate Buffer Values – At keyboard power-up time, the four autorepeat rate buffers contain default values (see Section 9.5.2.3 for autorepeat rates and Section 9.5.7 for defaults). The system module may change these values.

In the command byte, bit 7 (PARAMS flag) should be clear, bits 6–3 are 1111 (to indicate that this is a Rate Set command), bits 2 and 1 should be the buffer number (0 to 3), bit 0 (TYPE flag) is clear.

There should be two parameters carrying the rate set data.

Example: Change rates in buffer 3.



The first parameter specifies the timeout to the store in the selected buffer. The second parameter specifies the interval. Refer to Section 9.5.2.1 for definitions of these parameters.

For example, to set the autorepeat rate in buffer 1, the system module firmware transmits 00000011 followed by two bytes of numeric parameters.

The autorepeat timeout is the transmitted number times 5 ms. To specify a rate of 5 ms delay, the first parameter received is 00000001. The maximum allowable time is 630 ms (01111110). The system module must not send 635 (01111111).

NOTE
This code is reserved for internal keyboard use. 00 is an illegal value.

Autorepeat timeout is implemented as a multiple of 8.33 ms, the keyboard's internal scan rate. Timeout rates can vary ± 4.15 ms.

The autorepeat interval is the number of metronome codes per second. In order to specify a speed of 16 Hz, the second parameter received is 10010000. Note that the high order bit is set because it is the last parameter. The highest value which may be sent is 124 (11111100).

The lowest rate which can be implemented by the keyboard is 12 Hz. Values as low as 1 can be transmitted, but are translated to 12 Hz.

NOTE
The system module must not send 125 – or 11111101. This code is the Power-up command.

9.5.6 Special Considerations

The following paragraphs describe the special codes and their considerations.

9.5.6.1 Error Handling – There are four error codes. The first two are sent at power up if the self-test fails (Section 9.5.4.3). The other two codes are the INPUT ERROR code and the OUTPUT ERROR code.

The OUTPUT ERROR (B5 hex) is sent after the keyboard receives a Resume Transmission command, if the output buffer overflowed while the keyboard was locked.

The INPUT ERROR (B6 hex) is sent when the keyboard detects noise (unidentified command or parameter) on the line. B6 is also sent if the keyboard detects a delay of more than 100 ms when expecting a parameter.

9.5.6.2 Keyboard Locked Condition – When the keyboard receives an Inhibit Transmission command, it lights the LOCKED LED and transmits one more byte. This is a special code indicating that the keyboard is locked (KEYBOARD LOCKED ACKNOWLEDGE). If the system module receives this code without a request, it indicates that noise on the line was interpreted as an Inhibit Transmission command. The system module should immediately send the Resume Transmission command to unlock the keyboard.

The output first in first out (FIFO) buffer in RAM is four bytes. When the keyboard is locked it attempts to store characters received from the keyboard. The keyboard stops scanning its matrix. When the keyboard is unlocked by the system module, it transmits all 4 bytes in the output buffer. If any keystrokes have been missed due to buffer overflow, the keyboard transmits an error code as the fifth byte (OUTPUT ERROR). Any keys which were not transmitted and are being held down when the keyboard is unlocked are processed as new keys. An error code upon unlocking the keyboard indicates a possible loss of keystrokes to the system module.

The keyboard stops scanning its matrix when its buffer is full. However, it processes all incoming commands.

9.5.6.3 Reserved Code – The number 7F (hex) is reserved for the internal keyboard input and output buffers handling routines.

9.5.6.4 Test Mode – The keyboard jumps into a test mode by command during production test. It transmits a special code to the system module to confirm the test mode. If the system module receives this code, it should send the byte 80 (hex) to continue. This causes a jump to power-up.

9.5.6.5 Future Expansion – Some keycodes are reserved for future use as special codes or keycodes. Table 9-5 lists these reserved codes.

Table 9-5 Keyboard Division Default Modes

Keyboard Division	Mode	AR Buffer
Main array	autorepeat	0
Keypad	autorepeat	0
Delete	autorepeat	1
Cursor keys	autorepeat	1
Return and Tab	down-only	
Lock and Compose	down-only	
Shift and Control	down/up	
Six basic editing keys	down/up	

Table 9-6 Default Rates in Autorepeat Buffers

Buffer No.	Timeout (ms)	Internal (Hz)
0	500	30
1	300	30
2	500	40
3	300	40

9.5.7 Default Conditions

- Certain keyboard divisions have specific default modes. Some divisions default to the autorepeat mode; therefore, they have an associated buffer that contains the default values for timeout and interval. Timeout is the amount of time that the keyboard waits before starting to autorepeat a character. The rate of autorepeating a character is called the interval. Table 9-5 shows the default modes and Table 9-6 shows the default rates in the four keyboard division autorepeat rate buffers.

- The volume level for the keyclick and bell has an eight step range. The default volume level for the keyclick and bell is the third loudest.

- For the LK201 keyboard, the **Ctrl** (control) key defaults to the no keyclick state.

9.5.7.1 Audio Volume – Both keyclick and bell volumes are 2 decimal (010 binary) by default. The key in position C99 of the keyboard (the **Ctrl** key in the LK201) does not generate a click unless enabled by the system module. The keys in position B99 and B11 (**Shift** keys on the LK201) never generate a keyclick.

9.6 SPECIFICATIONS

Functional

Electronics	8-bit microprocessor, 4 kilobytes of ROM, 256 bytes of RAM, 4 LEDs, transducer
Cord	1.9 m (6 ft), coiled, 4-pin telephone-type modular connectors, plugs into display monitor (PN BCC01)
Keypad	Sculptured key array
Home row key height	30 mm above desk top
Keys 105 matte textured-finish keys	
Main keypad	57 keys
Numeric keypad	18 keys
Special function keypad	20 keys; firmware and software driven
Editing keypad	10 keys

Spacing	1.9 cm (0.75 in) center to center (single width keys)
Wobble	Less than 0.5 cm (0.020 in)
Diagnostics	Power-up self-test, generates identification upon passing test

Physical

Height	5 cm (2.0 in) at highest point
Length	53.3 cm (21 in)
Width	17.1 cm (6.75 in)
Weight	2 kg (4.5 lb)

CHAPTER 10
H7862 POWER SUPPLY

10.1 INTRODUCTION

This chapter describes the operation of the power supply in the Professional 300 Series Computer System. The shaded area in Figure 10-1 represents the relationship of the power supply to the other components.

The H7862 switching power supply converts line mains ac voltage to dc. The power supply also monitors voltage input and output. Figure 10-2 shows the functional block diagram for the power supply.

The power supply asserts two status signals to the CPU on the system module. These signals tell the CPU that ac and dc power have reached correct values. After receiving these signals, the CPU starts executing a boot program.

Section 10.6 provides the physical and electrical specifications for the power supply.

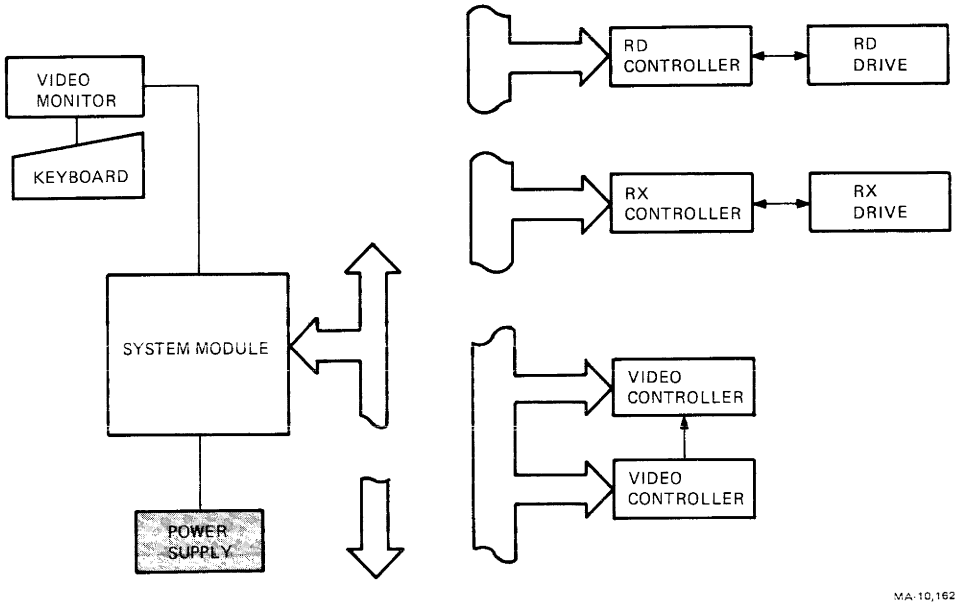


Figure 10-1 System Functional Block Diagram

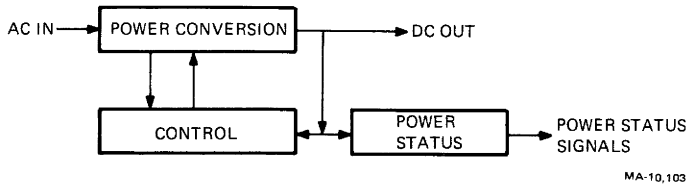


Figure 10-2 Power Supply Functional Block Diagram

10.2 PHYSICAL DESCRIPTION

The power supply connects to the system module with a cable (PN 17-00280) from J2 of the power supply. It connects to the RX diskette drive with a 6 inch cable (PN 17-00342-02) from P1 of the power supply, and to the RD hard disk drive with a 4 inch cable (PN 17-00342-01) from P2.

The power supply box mounts inside, on the top left of the Professional computer's chassis. Two slide-lock connectors hold the four studs on the bottom of the power supply chassis. Figure 10-3 shows the power supply. A rocker switch on the front panel turns system power on and off.

The exhaust fan on the left side cools the supply by pulling air across heat sinks and internal components. The air is drawn through the power supply chassis from the right side (which is all ventilating holes) and across the entire system chassis. This air movement cools the system components, option modules, and disk drive motor(s).

The rear panel has a connector for the ac power cable. The connector is polarized and allows the cable to be inserted in only one way. A circuit breaker protects internal wiring from component failure.

Before applying power for the first time, the user must ensure the voltage select slide switch is set for the nominal ac mains operating voltage (line voltage) in your area. See Table 10-1 for the correct switch setting for your nominal voltage.

The power supply contains three jacks. The rear jack connects to the system module circuit board. The two on the right side connect to the diskette motors and the optional hard disk drive.

Section 10.6 provides the physical and electrical specifications for the power supply.

10.3 FUNCTIONAL DESCRIPTION

The power supply converts ac to dc. The user sets the voltage selection slide switch on the rear panel, plugs the ac power cable into the power supply and ac source, and turns on the front panel switch. Table 10-1 shows the possible combinations of settings for the voltage selection switch and the actual ac input. A separate rectifier and regulator on the circuit board power the internal circuits. These circuits control regulation, protection, and the power status signals that are sent to the CPU.

WARNING

Check the ac select switch setting. A setting for 120 Vac operation in a 240 Vac environment causes the internal fuse to blow. If the power switch is immediately turned off, it is possible to reset the switch correctly and then use the computer. However, the power supply must be repaired before using the computer in a 120 Vac environment. If the circuit breaker trips within 3 to 8 seconds, the primary capacitors and possibly more components are destroyed.

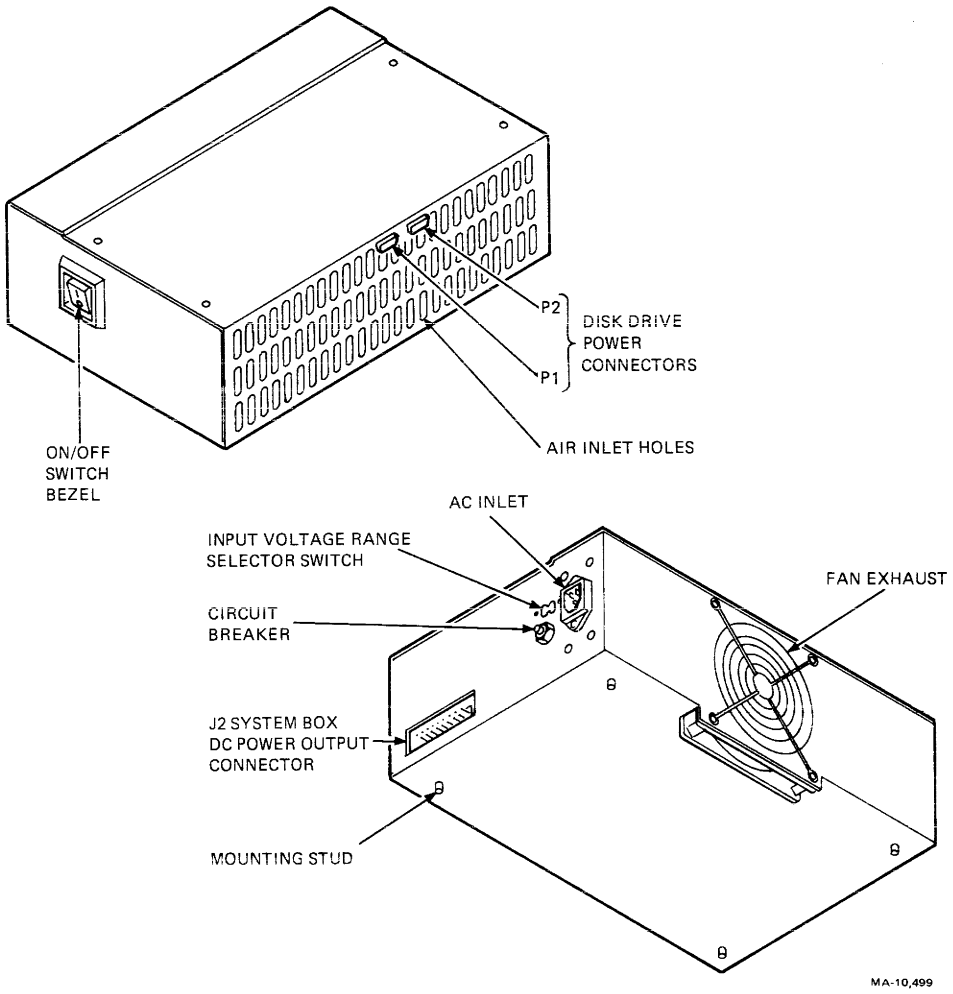


Figure 10-3 H7862 Power Supply

Table 10-1 AC Voltage Switch Settings

Switch Setting	Voltage	Operation
120	120	OK
240	240	OK
120	240	Internal fuse blows, protecting the transformer and fan. Refer to Section 10.3. Damage to switching transistors may occur.
240	120	Fan turns at 1/2 speed. Green indicator on rear of system box does not light. Switching transistors do not turn on. No power is provided to rest of system.

10.3.1 Power Conversion

Mains ac voltage is first filtered and then rectified to produce a dc voltage. The dc is then switched by two switching transistors that present high voltage dc pulses to the power switching transformer primary. The transformer's output, dc pulses, are rectified and filtered again to produce smooth dc. This permits the regulator to control the amount of energy transferred to the rest of the computer.

The transistors' switching is controlled by a driver transistor. The switch control signal, SWCON, controls the driver transistor. A crowbar protection circuit grounds the +5 and +12 Vdc outputs in the event of component failure. This prevents excessive voltages from getting out to the system devices. A diode in the −12 Vdc output serves the same purpose.

WARNING

The input capacitors hold high voltages for up to 5 minutes after system power is turned off. Refer to Section 10.4.1 for high voltage testing instructions.

10.3.2 Control Circuits

When power is first applied, the start-up regulator provides power for the internal control circuits and reference voltages used in protection circuits. The regulation circuit controls the duration of the switch pulse.

The two types of control circuits, regulation and protection, are discussed in the following paragraphs (Figure 10-4).

10.3.2.1 Regulation – Regulation circuits, using pulse width modulation, maintain the voltage levels. This is done by adjusting the pulse width of SWCON. As current demand increases, or main ac voltage decreases, the current sensing circuit holds SWCON high, making its pulses longer. The longer pulse permits the switching transistors to stay on for a longer time, permitting additional energy transfer and output power.

10.3.2.2 Protection – Protection circuits prevent damage from incorrect voltages. There are three protection circuits: overvoltage, start-up undervoltage, and overcurrent. These are exclusive of the circuit breaker and fuse. The circuits are ANDed so that any fault condition stops the switching transistors (Figure 10-5). The circuit names indicate the kind of protection given by each circuit. Table 10-2 shows the threshold values for the protection circuits.

The −12 Vdc regulator chip has an internal overcurrent protection circuit. A diode protects the chip from reverse voltages.

10.3.3 Power Status Signals

There are two power status signals sent to the CPU from the power supply: DCOK and POK. DCOK indicates that the dc levels are at specified voltages. POK tells the CPU that ac has been applied long enough to charge the primary capacitors so the emergency power loss program can be executed.

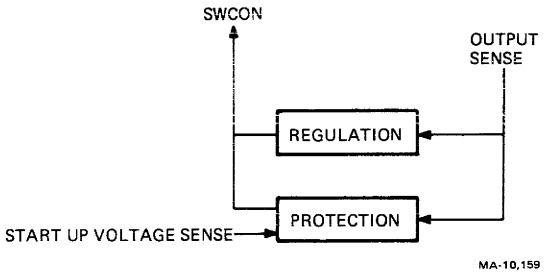


Figure 10-4 Control Block Diagram

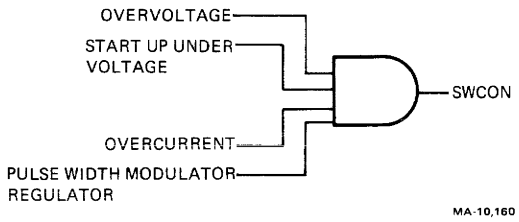


Figure 10-5 Protection

Table 10-2 Voltage Protection Thresholds

Output	Over Voltage	Over Current
+5	7 V maximum	21 – 33 A
+12	14.5 V maximum	11.5 – 17 A
−12	−14 V maximum	1.5 – 2.5 A

10.4 DETAILED DESCRIPTION

This section describes how each circuit group works.

10.4.1 Power Conversion

Incoming ac first passes through a line filter. This prevents computer-generated noise pulses from being coupled into the ac mains (line voltage). A full wave bridge then converts the ac to dc. If the ac mains is 120 Vac, then the full wave bridge serves as a voltage doubler and rectifier. This provides 250–350 Vdc to the two input capacitors. The capacitors store the energy for the switching cycles (Figure 10-6).

The regulation circuits, using the signal SWCON, make the switch driver transistor pulse on and off. This places a voltage across the control winding of the base power transformer and turns the two switching transistors on and off. Section 10.4.2 describes the circuits that control SWCON.

The switching transistors place a dc pulse on the primary of the switching transformer. The pulse has high voltage (about 360 Vdc) at low current and the transformer converts this to low voltage at high current. The switching frequency stays constant at 50 kHz. However, the pulse width changes to control the amount of power the transformer couples to the power supply output.

There are three secondaries to the transformer, one for each of the output voltages. Each ac output is rectified. The dc passes through low pass filters to smooth the pulsing dc output. Inductors and capacitors work together to smooth the pulses and steady the dc.

Crowbar protection circuits on the outputs of the +5 and +12 Vdc lines protect the computer in the event of component failure in the power supply. These circuits short the outputs to ground. A diode in the −12 Vdc output protects the 3-pin regulator chip and its output devices from positive voltages in the same way.

WARNING

The input capacitors hold high voltages for 5 minutes after system power is turned off. Before removing the power supply cover, turn off the power supply. Wait 5 minutes. Then measure the dc voltage from the case of Q2 (TO-3 transistor closest to the open side of the case) to the end of bleeder resistor R4 (also closest to the open side of the case). First set the meter to at least 500 Vdc full scale and reduce it as needed. If the voltage is 20 V or less, proceed with caution.

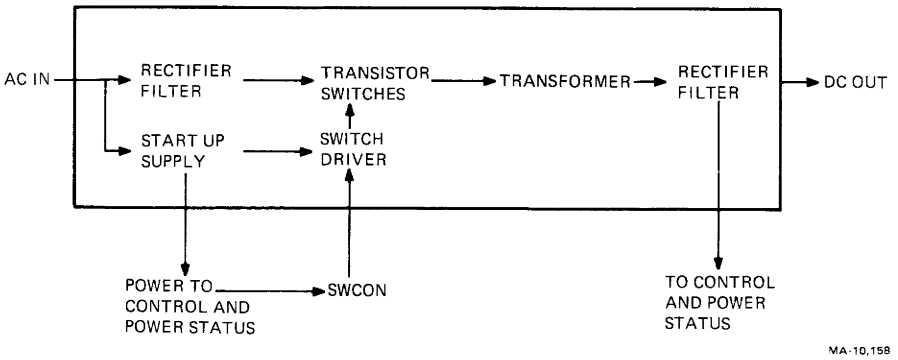


Figure 10-6 Power Conversion

10.4.2 Control

The signal, SWCON, controls the pulse width of the switched dc output from the power supply. Its sources are the regulation and protection circuits. When SWCON is high, it turns off a pre-driver transistor which turns off the driver transistor. The driver transistor controls the switching transistors by opening the control winding in the base power transformer. When the driver is off, the switching transistors are on.

The following sections describe the regulation and protection circuits.

10.4.2.1 Pulse Width Modulation Regulation – The +5 and +12 Vdc voltages are compared by a divider network and comparator circuit that provide a constant input to a regulator IC. When current demand is high, a drop in voltage occurs. The regulator senses the voltage drop and increases the pulse width (duty cycle). This permits additional energy transfer during the extended switch pulse.

The regulator's control signal is ANDed with the output of the protection circuits before going to the predriver transistor.

The −12 Vdc output has its own 3-pin regulator chip.

Soft Start – On power-up or when recovering from an overcurrent condition, the pulse width modulator goes through a soft start routine. This means the pulse width increases slowly from zero to operating width. The width is controlled by the charging of the output soft start capacitor. This prevents voltage surges on the output. If an output shorts, this gives the overcurrent circuit time to act before damage occurs.

10.4.2.2 Protection – The overvoltage, start-up undervoltage, and overcurrent circuits prevent internal damage to the power supply and the computer it is installed in. They are ANDed with the regulator's output so that any change from normal operation pulls SWCON low. This halts the switching transistors' control circuits (Figure 10-7) and prevents the switching transistors from applying input to the power transformer primary.

Overvoltage – Each output voltage is compared to internally generated reference voltages. These reference voltages come from the voltage across a precision zener diode. If any of the three output voltages exceed specified parameters, a latch circuit is tripped. The latch turns the switching transistors off and prevents further dc output. Since this latch is electrical, the operator must remove system power for at least 5 minutes (turn it off) before power can flow again.

If the −12 Vdc circuit has a positive voltage applied to it, a diode protects the regulator chip by grounding the output.

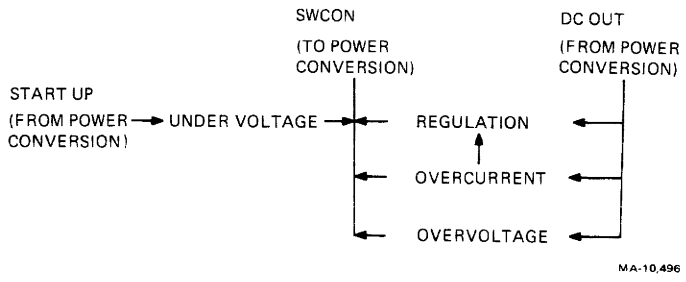


Figure 10-7 Protection Block Diagram

Start-Up Undervoltage – This circuit checks the power supply's start-up supply. If the voltage drops to 8.75 volts or less, it turns off the switching transistors. When voltage rises to normal, switching can start again.

Overcurrent – This circuit checks the current drain on the +5 and +12 volt lines. Divider networks compare the voltage drop across a current sense resistor. When the voltage across the sense resistor rises above the threshold value, a timing capacitor is discharged. SWCON is then held low, stopping the switching action. At the same time, the soft start capacitor begins discharging.

When the overcurrent condition clears, the timing capacitor starts charging. This begins a delay period. When the timing capacitor has charged enough, the overcurrent circuit releases SWCON so that switching can start again. However, the soft start capacitor discharge creates a slow restart. This helps prevent damage by detecting the fault, if it is still on the output, before the supply delivers full power.

The overcurrent sense capacitor requires 1 ms to charge up again. This allows the voltages and current to stabilize (soft start) before SWCON cycles again.

The −12 Vdc regulator chip has an internal overcurrent protection circuit.

10.4.3 Power Status Monitor

NOTE

In this section, ac and dc refer to mains alternating current and the direct current output. The signal names, AC and DC, refer to specific signals used in the power status monitor circuits.

The power supply control circuits assert two signals to the CPU on the main system board. There is a specific sequence for the two signals on power up and power down; DCOK is asserted before POK on power up and POK is cleared before DCOK on power down (Figure 10-8).

The dc detector looks for minimum values for the +5, +12, and −12 Vdc outputs. DCOK indicates that the power supply voltages from the power supply to the system module are within tolerance.

The ac detector measures ac at the switching transformer's secondary and is related to the energy stored in the input filter capacitors. POK H tells the CPU that ac has been applied long enough to charge the primary capacitors so an emergency power loss program may be executed. The signal change from a low to a high state initiates the boot program in the CPU (DCOK is high also). The change from high to low may initiate an emergency power loss program.

The following sections describe how the signals are generated. Refer to Figures 10-8 and 10-9 while reading these sections.

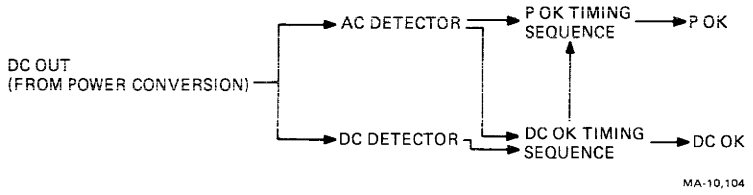


Figure 10-8 Power Status

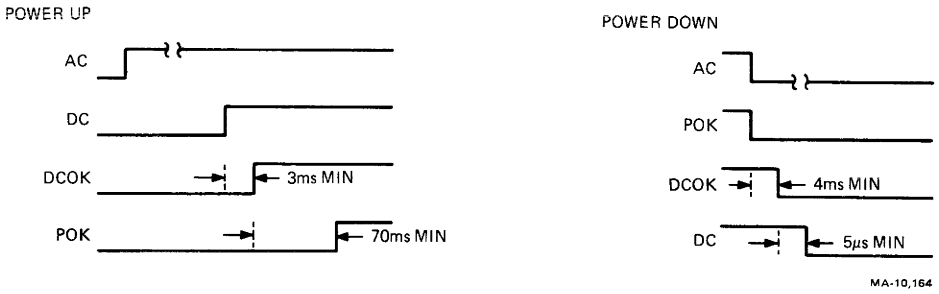


Figure 10-9 Power Status Signal Timing

10.4.3.1 DCOK – When all voltages have reached their minimum values, the protection circuit asserts dc. DC and AC (ac is present long enough to produce a +5 Vdc output) are asserted at the beginning of a timing chain. AC and DC clock a one-shot timer. DCOK is asserted to the CPU a minimum of 3 ms later.

The DCOK timing circuits also receive input from the ac detector (which asserts POK). The ac detect information permits the DCOK signal to time out through a capacitor if ac source voltage stops. On power down, the falling edge of AC removes POK. This starts timing out DCOK. A minimum of 4 ms after AC is removed, DCOK is removed and the CPU may execute an emergency power loss program.

The monitor circuits indicate an output is in regulation if the voltage is greater than the following voltages.

+5.1 Vdc +4.7 ±0.2 V
+12.1 Vdc +11.1 ±0.3 V
−12 Vdc +10.8 ±0.3 V

10.4.3.2 POK – On power up, the +12 Vdc asserts AC and sets a one-shot timer. This is ANDed with a signal that indicates the DCOK signal is asserted. A one-shot timer asserts POK a minimum of 70 ms later.

On power down, the falling edge of AC removes POK.

Table 10-3 System Module Connector, J2

Pin	Voltage/Signal
1	DCOK
2	reserved
3	POK
4	−12 Vdc
5	+12 Vdc
6–9	+ 5 Vdc
10–16	Ground

Table 10-4 Disk Motor(s) Connectors, P1 and P2

Pin	Voltage/Signal
1	+12 Vdc
2–3	Ground
4	+5 Vdc

10.5 CONNECTORS

Table 10-3 shows the pinning for J2, the system module connector on the rear panel.

Table 10-4 shows the pinning for P1 and P2, the disk motor(s) connectors on the side panel.

10.6 SPECIFICATIONS

The following paragraphs provide the specifications for the power supply.

10.6.1 Physical

Height	10.8 cm (4.25 in)
Width	21.0 cm (8.25 in)
Depth	33.0 cm (13.0 in)
Weight	4.54 kg (10 lb)

10.6.2 Electrical

Line voltage	87 – 132 Vac (for 120 Vac operation) 174 – 264 Vac (for 240 Vac operation)
Line frequency	47 – 63 Hz (for either voltage range)
Input line current (at full rated output)	6 A rms (for 120 Vac operation) 4 A rms (for 240 Vac operation)
Real input power (at full rated output)	320 W
Output regulation	+ 5.1 Vdc ±5% +12.1 Vdc ±5% −12 Vdc ±5%
Rated output voltage and current specifications	+ 5.1 Vdc at 5 A minimim, 20 A maximum +12.1 Vdc at 1 A minimum, 8 A maximum −12 Vdc at 100 mA minimum, 1 A maximum

CHAPTER 11
SYSTEM MEMORY AND MEMORY DAUGHTER MODULES

11.1 INTRODUCTION

The Professional 300 Series computer system contains random access memory (RAM) and additional circuitry to support memory option modules. This chapter describes the RAM used for the Professional 300 Series computer system.

11.2 PROFESSIONAL 325/350 SYSTEM MEMORY AND MEMORY OPTIONS

The following paragraphs describe the Professional 325 and 350 system memory hardware and available memory hardware options.

11.2.1 System Memory

System memory consists of two memory daughter modules. Each RAM daughter module consists of sixteen 64K × 1 dynamic MOS memory chips. Each daughter module provides 128 kilobytes of memory. The Professional 350 can address up to 512 kilobytes per daughter module.

There are two 40-pin connectors on the system module to accept the memory daughter modules. Installing either module in either connector informs the CPU of available address space. Bank 0 is the connector physically farther from the CPU chip set, bank 1 is the connector that is closer. Figure 11-1 shows the position of the system memory daughter modules.

The system control and status register (17773700) is read to determine the memory configuration. Bits 03–00 are defined in Table 11-1.

NOTE

Refer to Volume I, Sections 5.3.9 and 5.4.9 for detailed information on RAM hardware and program register information for the Professional 350 computer system.

When both connectors contain memory option modules, the module in bank 0 always starts at 00000000. The module in bank 1 starts where the module in bank 0 ends. Refer to Table 11-2.

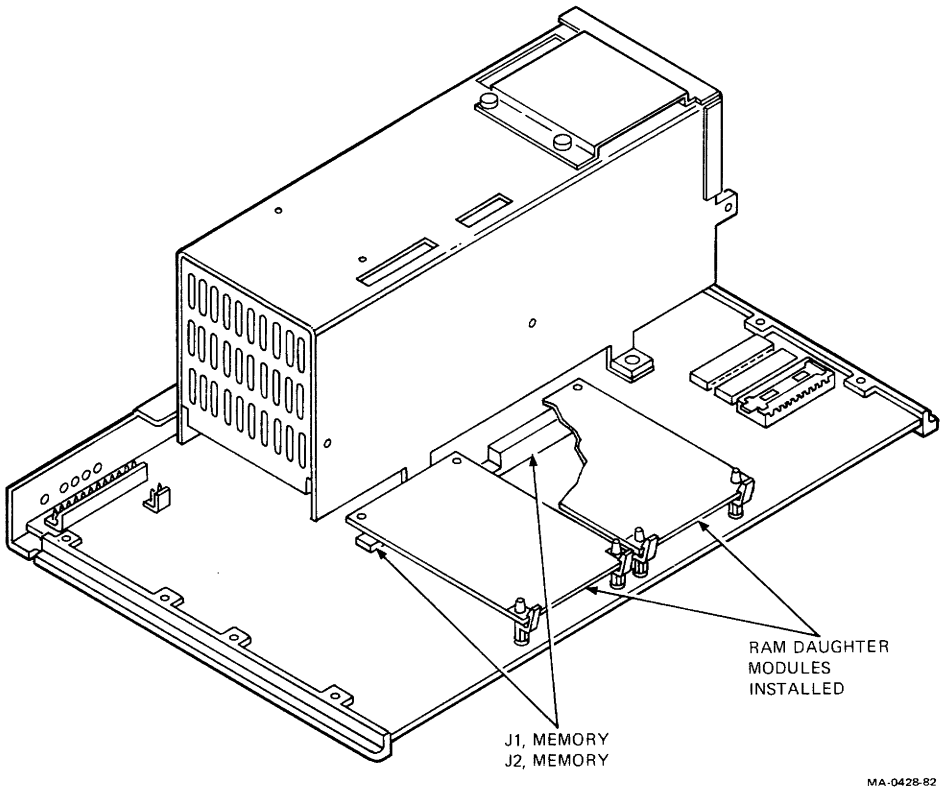


Figure 11-1 System Memory Daughter Modules

Table 11-1 Professional 350 System Control/Status Register

Bit	State	Definition
00	0	No memory module present in memory slot 0.
00	1	Memory slot 0 contains a memory module.
01	0	The memory module in slot 0 is 128 kilobytes.
01	1	The memory module in slot 0 is 512 kilobytes.
02	0	No memory module present in memory slot 1.
02	1	Memory slot 1 contains a memory module.
03	0	The memory module in slot 1 is 128 kilobytes.
03	1	The memory module in slot 1 is 512 kilobytes.

Table 11-2 Memory Option Module Address Range

Bank 0	Bank 1	Memory	Address Range
128 kilobytes	0	128 kilobytes	00000000–00377777
0	128 kilobytes	128 kilobytes	00000000–00377777
128 kilobytes	128 kilobytes	256 kilobytes	00000000–00777777

11.2.2 Memory Options

Additional memory can be installed in the CTI Bus cardcage. The Professional 350 backplane memory option module provides 256 kilobytes of RAM using 32 64K × 1 dynamic RAMs. It can provide up to 1 megabyte using 32 256K × 1 dynamic RAMs. More than one option module can be installed in the card cage.

11.2.3 Professional 350 System Memory Map

Table 11-3 is the memory map for the Professional 350 computer system.

Table 11-3 Professional 350 Memory Map

Address	Destination
00000000–????????*	RAM – system memory
17730000–17767776	16 Kb ROM – diagnostic/boot
17772300–17772316	MMU – kernel PDRs
17772340–17772356	MMU – kernel PARs
–17772516	MMU – SR3
17773000–17773032	Clock registers
17773034–17773176	Battery backed-up RAM – 50 bytes
17773200–17773212	Interrupt controller registers
17773300–17773314	Communication port registers
17773400–17773406	Printer port registers
17773500–17773506	Keyboard registers
17773600–17773676	ID Professional
–17773700	System CSR
–17773702	Option module present register
–17773704	Indicator (LED) display register
17774000–17774176	Option module slot 0
17774200–17774376	Option module slot 1
17774400–17774576	Option module slot 2
17774600–17774776	Option module slot 3
17775000–17775176	Option module slot 4
17775200–17775376	Option module slot 5
17777560–17777566	Maintenance terminal registers
17777572–17777576	MMU – SR0, SR1, SR2
17777600–17777616	MMU – user PDRs
17777640–17777656	MMU – user PARs
–17777750	Processor maintenance register
–17777776	Processor PSW

* Upper address limit depends on the amount of RAM with which the system is configured. All addresses are in 22-bit octal format.

11.3 PROFESSIONAL 380 SYSTEM MEMORY AND MEMORY OPTIONS

The following paragraphs describe the Professional 380 system memory hardware and available memory hardware options.

11.3.1 System Memory and Memory Options

The Professional 380 system module implements two groups of local RAM (see Figure 11-2), module-resident RAM and a RAM daughter module that connects onto the Professional 380 system module.

System Module-Resident RAM – The Professional 380 contains 512 kilobytes of system module-resident RAM. The on-board RAM is made up of 64 64K × 1 dynamic RAM integrated circuit chips.

RAM Daughter Module – The RAM daughter module plugs into a 48-pin connector on the system module. The daughter module uses 40 pins on the connector. The remaining eight pins are used for memory size information for future memory expansion. (There is no commitment by Digital to supply this.)

Memory Options – The Professional 380 computer system comes with 512 kilobytes of RAM as standard equipment. The 512 kilobyte daughter module (MSC11-B) and the CTI Bus memory option module are memory options for the Professional 380.

A private address/data bus channels data between the DC365 controller gate array and RAM. The DC365 controller gate array can support up to 3 megabytes of system memory.

NOTE

Refer to Volume 1, Chapter 6, Section 6.3.5 for detailed RAM hardware information and Sections 6.4.1.4 and 6.4.2 for program register information.

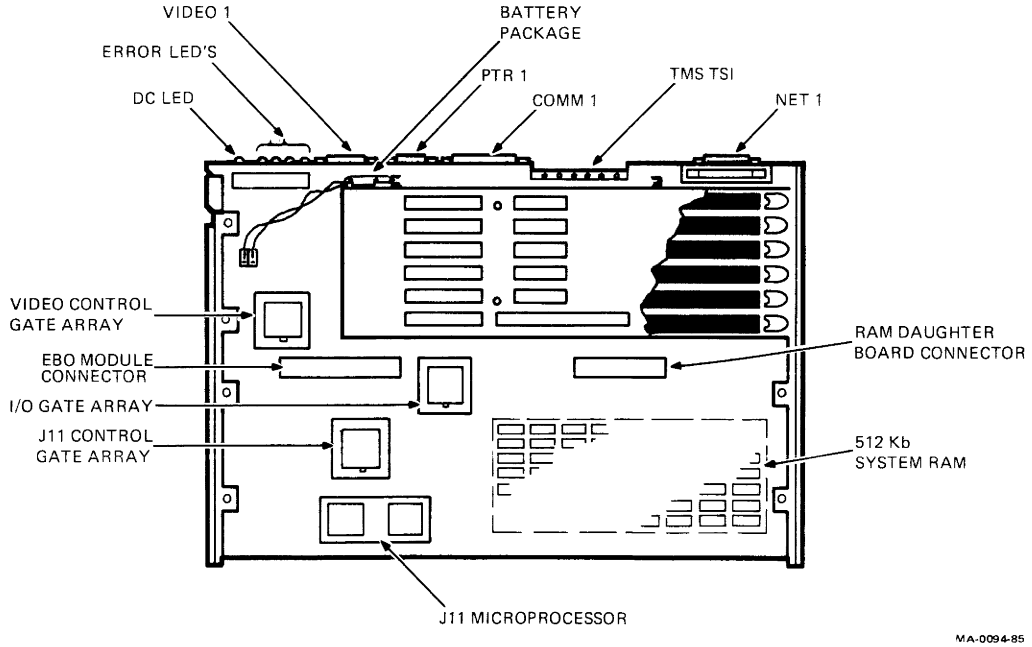


Figure 11-2 Professional 380 System Memory

11.3.2 Professional 380 System Memory Map

Table 11-4 is the memory map for the Professional 380 computer system. For more detailed information, refer to Volume 1, Chapter 6.

Table 11-4 Professional 380 Memory Map

Address	Destination
14000000–14377777	Video memory
17700000–17727777	Reserved for future expansion
17730000–17757777	Base system ROM
17760000–17767777	Base system ROM
17767700	Continue boot address
17767730	Reboot/software crash address
17770000–17770037	Reserved for manufacturing
17772200–17772216	R/W supervisor I space PDRs
17772220–17772236	R/W supervisor D space PDRs
17772240–17772256	R/W supervisor I space PDRs
17772260–17772276	R/W supervisor D space PDRs
17772300–17772316	R/W kernel I space PDRs
17772320–17772336	R/W kernel D space PDRs
17772340–17772356	R/W kernel I space PDRs
17772360–17772376	R/W kernel D space PDRs
17772516	Memory management register #3
17773000–17773032	TOD clock registers
17773024	Control/status register 0
17773026	Control/status register 1
17773030	Control/status register 2
17773032	Control/status register 1
17773034–17773176	Battery-backed up RAM
17773200–17773212	Interrupt controller registers
17773300–17773314	Communications port registers
17773400–17773406	Printer port registers
17773500–17773506	Keyboard port registers
17773600–17773676	ID – 32 bytes
17773700	System CSR
17773702	Option module present register
17773704	LED and MODE register
17773706	μODT single stepping register
17774000–17774176	Slot 0 addresses
17774200–17774376	Slot 1 addresses
17774400–17774576	Slot 2 addresses
17774600–17774776	Slot 3 addresses
17775000–17775176	Slot 4 addresses
17775200–17775376	Slot 5 addresses

Table 11-4 Professional 380 Memory Map (Cont)

Address	Destination
17775400–17775426	Video registers
17775430–17775576	Reserved registers in video slot
17777560–17777566	Maintenance terminal DL register
17777560	Receive control/status register
17777562	Receive data buffer register
17777564	Transmit control/status register
17777566	Transmit data buffer register
17777572	Memory management register 0
17777574	Memory management register 1
17777576	Memory management register 2
17777600–17777616	R/W user I space PDRs
17777620–17777636	R/W user D space PDRs
17777640–17777656	R/W user I space PDRs
17777660–17777676	R/W user D space PDRs
17777740–17777750	System I/O addresses
17777746	Cache control register
17777750	Processor maintenance register
17777752	Hit/miss register
17777766	CPU error register
17777772	Programmable interrupt register
17777776	Processor status register

11.4 PROFESSIONAL 350/380 CTI BUS MEMORY OPTION MODULE

The Professional 350 and 380 accepts a CTI Bus memory option module (MSC11-CK). The module enlarges the amount of available RAM. The option module is a single 5.2 × 12 inch field replaceable unit (PN 54-15488) which mounts in any slot of the CTI Bus card cage. A zero insertion force (ZIF) 60-pin connector at the bottom of the module connects the option module to the CTI Bus card cage.

The octal ID code, 000034, is on the ZIF handle. More than one RAM option module may be inserted into the CTI Bus card cage. The maximum quantity of RAM option modules depends on the memory capacity of each option module and the maximum addressable memory space of each Professional computer system's configuration.

NOTE

Refer to the CTI Bus Technical Manual and the 256K RAM schematic, (PN CS 5415488-0-DBP) for the following discussion.

11.4.1 Functional Description

The CTI Bus memory option module use a CTI Bus interface circuit to perform all bidirectional transfer for data, commands, and status under control of the CPU (see Figure 11-3). A diagnostic ROM directs a self-test diagnostic upon power up. Commands and status are combined in one programmable register.

The following provides a general description of a host processor-to-CTI Bus memory option transaction.

A host central processor reads and writes to a program register group and RAM through a CTI Bus interface circuit. The central processor also does a read to the program ROM and a status register for configuration and self-testing information.

The lower boundary of the RAM address range is programmmed during system initialization. The lower boundary value is written into a RAM base-address register. The boundary is selected from 16 kiloword (32 kilobyte) boundaries.

Table 11-5 shows an example of RAM lower boundary value determination.

The upper boundary of the RAM address range is determined by memory size and software.

Additional memory option modules can be installed in the CTI Bus card cage. A RAM base address register is configured during initialization. Up to two banks of memory are read and written to. Memory refresh circuits service the RAM components cyclically. Parity circuits generate and detect memory parity storage. Optionally, parity circuits may be disabled.

Memory words of any bank are 18 bits long. The lower 8-bit byte has a ninth bit representing odd parity. The upper byte has a stored parity bit, similar to the lower byte, using even parity.

Table 11-5 RAM Lower Boundary Value Determination

Decimal 16K Word Boundary	Octal Starting Address	Octal Write-byte to RAM Base Address Register
0	00 000 000	0
1	00 100 000	1
2	00 200 000	2
.	.	.
.	.	.
7	00 700 000	7
8	01 000 000	10
.	.	.
65	10 100 000	101

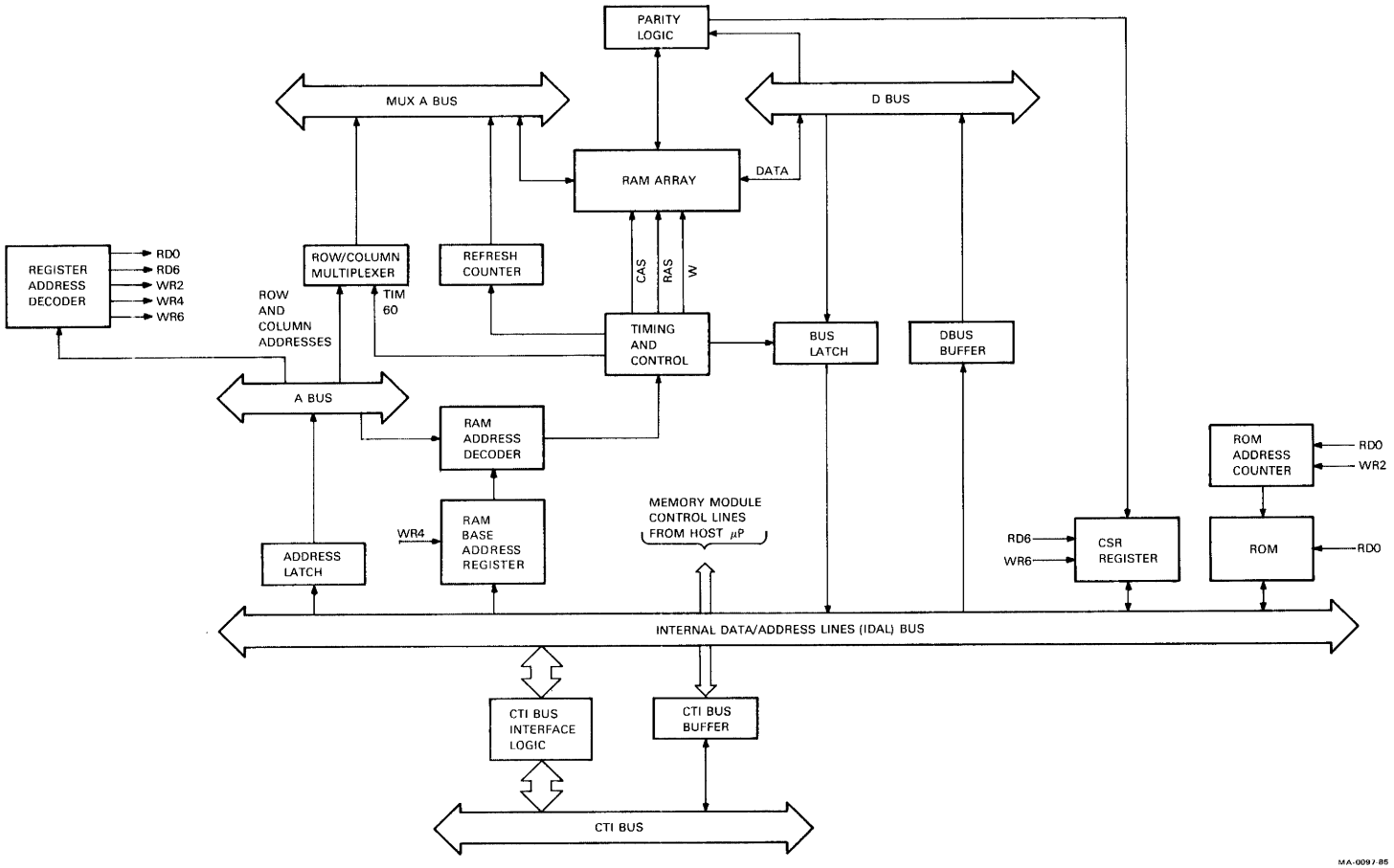


Figure 11-3 CTI Bus Memory Option Module Block Diagram

11.4.2 Detailed Description

The CTI Bus memory option module contains the following circuits. Refer to Figure 11-3.

CTI Bus interface
Timing circuits
Diagnostic ROM
RAM memory banks
RAM refresh circuits
RAM parity circuits
RAM base-address register
Control/status register

CTI Bus Interface Circuits – The CTI Bus interface circuits propagate bidirectional signals between this slave module and the system module. Refer to the connector signal description section for the assortment of signals pertinent to this module's functions and to the predetermined power up condition of the board.

Timing Circuits – The timing circuits phase signals for accessing the ROM and RAM memory. The access time is defined as the time from AS (Address Strobe) assertion to RPLY (Reply) assertion. The access times are shown in Table 11-6.

Diagnostic ROM – Diagnostic ROM resident on this option module is read by the system module CPU during the system power-up sequence of diagnostic and initialization processes. The board's ROM address counter is preset to 0 upon power up and/or upon any write operation to the ROM address counter. The ROM address counter advances upward through successive ROM addresses with each read operation. The diagnostic directions check the write and read operations to the entire RAM array, the parity circuits, the refresh circuits, and the RAM base address register by using the control/status register. The RAM capacity is checked and configured into the system RAM map.

Table 11-6 Memory Access Time

Bus Cycle Type	Typical Access Time	Maximum Access Time
Read	515 ns	600 ns
Write	725 ns	770 ns

Table 11-7 RAM Memory Bank Jumper Scheme

Jumper	Indication if Inserted	Indication if Removed
W1	The module is half populated.	The module is fully populated.
W4	Reserved. A future IC size is present	Chips of 64 × 1 size are present.

RAM Memory Banks – The RAM option module has up to two banks populated with dynamic RAM IC chips. Each bank has 18 IC chips, including two for parity bit storage. Jumpers on the board identify chip size and IC population. The jumper information is conveyed to the software via the status bits of the control/status register. Table 11-7 defines the RAM memory bank jumpers.

Data words or data bytes are passed to and from RAM via an internal data bus (D Bus). The internal data bus communicates to the internal data-and-address bus (Dal Bus), which simultaneously communicates to the CTI Bus.

The output of a RAM address comparator drives the RAM address decoding circuits to the appropriate memory bank. The address output of the refresh row counter is substituted for the comparator output for presentation to the RAM address decoder. The RAM address on the CTI Bus is passed to an address latch via the internal Dal Bus. The output of the address latch drives the address comparator. The comparator compares the 7 most significant bits of the requested RAM address with the 7 bits stored in the configured RAM base-address register.

NOTE

Address binary bit 17 determines which bank from among two banks is accessed when a 256 kilobyte board is fully populated with 64K × 1 RAM ICs. Bank 0 containing the lower half of addresses is accessed when bit 17 is cleared; bank 1 containing the upper half of addresses is accessed when bit 17 is set.

RAM Refresh Circuits – Each storage cell (1 bit) is refreshed at least once every 3.3 milliseconds. The 65,535 cells of each IC chip (64K × 1) are organized into 256 rows of 256 bits each. All bits of a given chip row are refreshed within a 515 nanosecond read minor-cycle.

A refresh of a row is triggered approximately every 13 microseconds. The corresponding chip row of each or both banks is refreshed simultaneously. The refresh counter sequences thru all chip rows in a cycle time of 3.3 milliseconds.

RAM Parity Circuits – Parity is generated for both the low byte and high byte of any word. A control bit in the control/status register enables and disables parity sensing. The same bit enables and disables the BMER signal. The BMER signal produces a memory error trap to the CPU via the CTI Bus. Another control bit in the control/status register provides for the election of correct or incorrect parity generation enabling the self-test diagnostics to perform a validity check of the memory sense circuits.

RAM Base Address Register – The data written to this register determines the range of RAM addresses between a lower boundary and an upper boundary. The CTI Bus memory option module does not respond to addresses above 13 777 777 regardless of the content of this register.

Control/Status Register – Status bits in this register inform the configuration software of the available RAM capacity. Control bits of the register enable RAM access, select parity polarity, and enable memory error traps to the CPU. Another status bit points to the bank having memory errors.

11.4.3 Programming Information

The operating system software manipulates following registers.

ROM data register
ROM address counter
RAM base-address register
Control/status register

The access addresses of the above registers are slot dependent. The value of an access address for the writing to or reading of one of these registers consists of the sum of a BASE value and an OFFSET value, shown in the two lists below.

The BASE value is slot dependent. The values of BASE are as shown.

Backplane Slot	**Base Value**
0	17774000
1	17774200
2	17774400
3	17774600
4	17775000
5	17775200
6	17775400
7	17775600

The value the of access address is the sum of the above listed BASE values, plus the OFFSET values listed below.

	Value of Access Address		
Programming Register	**BASE**	**+**	**OFFSET**
ROM data register	BASE	+	0
ROM address counter	BASE	+	2
RAM base address register	BASE	+	4
Control/status register	BASE	+	6

ROM Data Register – This is a low byte read-only register. A read to the high byte sees 0s. The ROM array is addressed when the ROM address counter generates an address strobe on the internal Dal Bus. The address strobe causes the address location of the ROM array to be placed on the CTI Bus.

Table 11-8 ROM Jumpers

Jumper	Inserted	Removed
W2	A 2K × 8-bit ROM is present.	A 4K × 8-bit ROM is present.
W3	A 4K × 8-bit ROM is present.	A 2K × 8-bit ROM is present.

ROM Address Counter – The CTI Bus INIT signal clears this counter to 0. The output of the counter addresses the complete ROM address range. A read to this counter sees 0s. A write operation to this counter resets the counter to 0. The counter is incremented by a read operation to the ROM data register. An increment beyond address 7 777 recycles the counter to 0 000. Factory installed jumpers accommodate the following two optional ROM sizes. Table 11-8 defines which jumper is used for each optional size.

RAM Base-Address Register – The RAM base-address register configures the starting address of RAM to any 32K byte boundary in the system address space. The operating system software and the diagnostic ROM calculate a lower limit boundary to be written to this register. The lower limit boundary serves as the starting address of the contiguous addresses through the entire RAM module address range.

The slot select signal, in conjunction with the 22-bit DAL signals of the CTI Bus, channel write/read functions to the appropriate RAM module programming registers. The effective lower limit boundary represents the 7 most significant bits of a 22-bit address field. Those 7 bits are written into the RAM base-address register using a low-byte-only transfer. RAM access is enabled by setting the MEMEN bit (bit 00) in the control/status register. Any read operation to the RAM base address register sees all 0s.

Control/Status Register – The functions of control and feedback status are split between bits of this register. The convenience of a common address for access to the low-byte-only register for both functions is implemented. Writing to the high byte has no effect. Reading the high byte sees all 0s. Table 11-9 defines each bit of the control/status register.

Maintenance Displays – Table 11-10 shows all the possible error indications that are displayed at the completion of a self-diagnostic cycle.

Table 11-9 CTI Bus Memory Option Module Control/Status Register

Bit	Bit Mnemonic	Bit Function
07	PERR	Parity Error is a read/write bit that means a parity error occured on a memory read operation when set. No parity error occured on a memory read operation when cleared. The bit may be cleared by writing a 0 to this register during a write low byte operation. Assertion of the CTI Bus INIT signal also clears this bit.
06	BERR	Bank Error is a read-only bit that functions regardless of whether the parity circuits are enabled. The bit is updated upon any occurrence of a parity error. It indicates that the parity error occured while reading bank 1 (chips E71–E88) when set; that the parity error occurred while reading bank 0 (chips E53–E70) when cleared.
05	FPOP	Fully Populated is a read-only bit. It means the board is fully populated with RAM chips in both banks when the bit is set. The board is half populated, bank 0 only, when the bit is cleared. The bit, in conjunction with bit 04 (SIZE), is used by the software to determine memory capacity of the board.
04	SIZE	This is a read-only bit that refers to RAM IC chip size. When cleared, it indicates that 64K size IC chips are resident. The set state is reserved for a future IC chip size.
03	Not used	This read-only bit is always seen as 0.
02	WROP	Diagnostic Write Opposite is a read/write bit. Software verifies that the parity circuits function correctly with the use of this control bit. The bit functions regardless of whether or not parity sensing is enabled. Opposite parity is generated on write to RAM memory operations when the bit is set. Correct parity is generated when the bit is cleared. The bit is also cleared by the CTI Bus INIT signal.
01	PTEN	Parity Trap Enable is a read/write bit. The BMER (Memory Parity Trap Error) signal on the CTI Bus is enabled by this slave module upon the occurrence of a parity error, providing this control bit is set. Thus, a parity trap to the CPU is enabled. Parity generation and parity sensing functions normally when this control bit is cleared, but does not assert a BMER signal; hence the memory parity trap to the CPU is disabled. The bit is also cleared by the CTI Bus INIT signal.
00	MEMEN	This is a read/write bit. The bit is preset to the cleared state upon power up so that access to ram memory is prohibited. The bit should be programmmed to the set state only after the lower boundary value for the board's RAM memory has been written into the RAM base address register in order to prevent conflict within the map of addressable system memory space. The set state permits access to the board's memory locations.

Table 11-10 CTI Bus Self-Diagnostic Error Code Listing

Error Number	Error Definition
0	No errors were detected.
1	The control/status register initialized improperly.
2	Illegal configuration; this memory module cannot be configured because the cumulative system RAM already exceeds 3 megabytes.
3	A memory error trap failed to occur when addresses higher than the 3 megabyte limit were attempted on a system configuration exceeding that limit by including this module's memory capacity.
4	The parity circuits failed to detect the incorrect parity written.
5	Bad data was read from memory.
6	An unexpected nonexistent memory trap occurred.
7	An unexpected memory parity trap occurred.
10	The control/status register bits do not match those associated with the CTI Bus BMER signal of a memory parity trap condition.

11.4.4 Hardware Specifications

The CTI Bus option module meets the following electrical, environmental, and mechanical tolerances.

Electrical Specifications – The following list shows the dc power requirements for full and half RAM chip populations.

Category	Minimum	Nominal	Maximum
Voltage	4.75	5	5.25
Current		1.50	1.75
Power		7.50	

The nominal value of amperage current given above includes the 200 milliampere current drawn during the fastest access rates. The current drawn decreases as the rate of access decreases. The current drawn when no read or write accesses are being made is 200 milliampere less or 1.3 ampere for a fully populated board.

Environmental Specifications – The following list shows the CTI Bus option module environmental specifications.

Parameter	Minimum	Maximum
Storage Temperature	−40°C (−40°F)	66°C (151°F)
Operating Temperature	5°C (41°F)	60°C (140°F)
Storage Humidity	10% relative	95% relative
Operating Humidity	10% relative	95% relative
Storage Altitude		50,000 ft (90 mm mercury)
Operating Altitude		50,000 ft (90 mm mercury)

Physical Characteristics – The following list shows the physical specifications for the CTI Bus memory option module.

Parameter	Dimension
Length	30.48 cm (12 in)
Width	13.20 cm (5.2 in)
Height	0.060 cm (0.515 in)
Weight	342 grams (12 oz)

11.4.5 Connector Signal Descriptions

Table 11-11 lists all pins and signals for the CTI Bus memory option module. The signal pins which do not list a transceiver type are not used.

Table 11-11 CTI Bus Memory Option Module Pin Listing

Option Module Transceiver Type				
Pin	**Signal**	**Bus Driver**	**Bus Receiver**	**Termination**
1	BDCOK H		74LS125	
2	+5 V			
3				
4	GND			
5	BINIT L		74LS125	T
6				
7	BDAL 15L	8307	8307	T
8	BDAL 13L	8307	8307	T
9	BDAL 14L	8307	8307	T
10	BDAL 12L	8307	8307	T
11				
12	BDAL 11L	8307	8307	T
13	BRPLY L	74S03		T
14	BDAL 10L	8307	8307	T
15	GND			

Table 11-11 CTI Bus Memory Option Module Pin Listing (Cont)

Option Module Transceiver Type				
Pin	**Signal**	**Bus Driver**	**Bus Receiver**	**Termination**
16	BDAL 09L	8307	8307	T
17	BMDEN L		74S240	T
18	BDAL 08L	8307	8307	T
19	BWRITE L		74S240	T
20	BDAL 07L	8307	8307	T
21	BWLB L		74S240	T
22	BDAL 06L	8307	8307	T
23	BWHB L		74S240	T
24	BDAL 05L	8307	8307	T
25	BSDEN L		74S240	T
26	BDAL 04L	8307	8307	T
27	GND			
28	BDAL 03L	8307	8307	T
29	SSx L		74LS138, 74S04	
30	BDAL 02L	8307	8307	T
31				
32	BDAL 01L	8307	8307	T
33				
34	BDAL 00L	8307	8307	T
35	OPRES L	GND		K
36	GND			
37	BDS L		74S240	T
38	+5 V			
39	BAS L		74S240	T
40				
41				
42				
43	BIOSEL L		74S240	T
44	BDAL 21L		8307	T
45				
46	BDAL 20L		8307	T
47				
48	BDAL 19L		8307	T
49				
50	BDAL 18L		8307	T
51	GND			
52	BDAL 17L		8307	T
53	BMER L	74S03		T
54	BDAL 16L		8307	T
55				
56				
57				
58	+5 V			
59				
60	GND			

APPENDIX A
DIAGNOSTIC, ERROR, AND DEVICE CODES

The following table lists the diagnostic errors that may occur on system power up. The error number column is in the following format.

sseeeee
iiiiii

Where "s" is a slot number, "e" is an error code number, and "i" is an ID number. The error codes for each ID code are listed below.

Table A-1 System Error Numbers

ID Number	Error Number	Description
000000	177777	Device not present (not displayed).
1	60	Keyboard is not functioning properly.
	75	Keyboard has a stuck key.
14	1	Unexpected interrupt or trap occurred with manual input device interface.
	200	Time out occurred during loopback testing of manual input device interface.
	201	Time out occurred while waiting for character to be received from manual input device interface.
	202	Overrun or framing error with manual input device interface.
	203	Data compare error with manual input device interface.
17	1	Unexpected interrupt or trap occurred with printer interface.
	200	Time out occurred during loopback testing of printer interface.
	201	Time out occurred while waiting for character to be received from printer interface.
	202	Overrun or framing error with printer interface.
	203	Data compare error with printer interface.

Table A-1 System Error Numbers (Cont)

ID Number	Error Number	Description
21	12	Time out occurred during data loopback testing of communication interface.
	13	Unexpected interrupt or trap occurred during communication interface testing.
	14	Unexpected external/status interrupt from communication interface
	15	Special receive condition interrupt from communication interface
	16	Data compare error with communication interface
	17	Undefined interrupt from communication interface
	20	Time out occurred during modem loopback testing of communication interface testing.
	21	Bad modem signals detected in communication interface.
23	21	Clock did not interrupt in proper time.
	25	Unexpected interrupt or trap occurred during clock testing.
24	22	Data compare error with battery backed up RAM
	23	Unexpected interrupt or trap occurred during battery backed up RAM testing.
25	1	No interrupts generated from interrupt controller.
	2	Unexpected interrupt or trap occurred during clock interface testing.
401	1	RD50 – Bad operation ended bit on power up.
	2	RD50 – Internal power-up self-test error
	3	RD50 – Bad bit/register sector, cylinder, or head registers
	4	RD50 – Busy bit did not go away.
	5	RD50 – Drive is not ready or seek incomplete.
	6	RD50 – Restore command did not cause an "A" interrupt.
	7	RD50 – Restore command did not set operation end bit.
	10	RD50 – Error bit set Restore command.
	11	RD50 – Incomplete read
	12	RD50 – Restore did not reach home during read test.
	13	RD50 – Error bit set on operation end.
	20	RD50 – Bad operation ended bit on power up.
	21	RD50 – Seek incomplete, write fault, or drive not ready
	22	RD50 – Bad bit/register sector, cylinder, or head registers
	23	RD50 – Read command time out
	24	RD50 – Unexpected interrupt or trap
	25	RD50 – Data mark not found.
	26	RD50 – Track 0 error.
	27	RD50 – Illegal/aborted command
	30	RD50 – ID not found.
	31	RD50 – CRC error, ID field
	32	RD50 – CRC error, data field
	33	RD50 – Unexpected operation end interrupt
	34	RD50 – Invalid operation end interrupt
	35	RD50 – Unexpected DRQ interrupt
	36	RD50 – Invalid DRQ interrupt
	37	RD50 – Restore command time out

Table A-1 System Error Numbers (Cont)

ID Number	Error Number	Description
2004	1	RX50 – Internal self-test time out
	2	RX50 – Unexpected interrupt or trap
	3	RX50 – Bad sector buffer
	10	RX50 – Bad drive 0 track 00 sensor
	20	RX50 – Bad drive 1 track 00 sensor
	30	RX50 – Both drives failed to respond.
	40	RX50 – Tried to access an unspecified track number.
	50	RX50 – Drive fails to see home.
	60	RX50 – Data record not found.
	70	RX50 – ID record not found.
	100	RX50 – Time out for FD command done.
	120	RX50 – Selected diskette is not ready.
	130	RX50 – Diskette not installed correctly.
	140	RX50 – ID CRC error
	150	RX50 – Seek error
	160	RX50 – Data ready signal (DRQ) did not respond in 32 ms.
	170	RX50 – Soft ID read error
	200	RX50 – Data CRC error
	210	RX50 – Lost data (8051 did not respond to DRQ within 23 μs).
	220	RX50 – Tried to access an unavailable diskette.
	230	RX50 – Drive not ready during write command.
	240	RX50 – Drive not ready during read command.
	250	RX50 – No sector matches the specified sector.
	260	RX50 – Diskette write protected on a write command.
	270	RX50 – Tried to access a nonspecified sector number.
	300	RX50 – The lower nibble of RAM failed to pass memory test.
	310	RX50 – The higher nibble of RAM failed to pass memory test.
	320	RX50 – No index pulse detected.
	330	RX50 – Drive speed not in limit.
	340	RX50 – Bad format or a blank disk.
	350	RX50 – Stepping error
	354	RX50 – Tried to set unsupported disk parameters.
	360	RX50 – Phase Lock Loop (PLL) frequency not in limit.
	364	RX50 – Tried to read a sector with a deleted data mark.
	370	RX50 – Data buffer is bad.
	374	RX50 – Tried to write a non-RX50 formatted disk.
50	2	PC380 video – Register failure
	3	PC380 video – Plane 1 memory failure
	4	PC380 video – Vertical retrace failure
	5	PC380 video – Counter register failure
	6	PC380 video – Plane 1 control, X, Y, or pattern register failure
	7	PC380 video – Plane 1 scroll register failure

Table A-1 System Error Numbers (Cont)

ID Number	Error Number	Description
1002	2	PC350 video – Register failure
	3	PC350 video – Plane 1 memory failure
	4	PC350 video – Vertical retrace failure
	5	PC350 video – Counter register failure
	6	PC350 video – Plane 1 control, X, Y, or pattern register failure
	7	PC350 video – Plane 1 scroll register failure
	103	PC350 EBO – Plane 2 memory failure
	106	PC350 EBO – Plane 2 control failure
	107	PC350 EBO – Plane 2 scroll register failure
	203	PC350 EBO – Plane 3 memory failure
	206	PC350 EBO – Plane 3 control failure
	207	PC350 EBO – Plane 3 scroll register failure
1403	2	PC350 video – Register failure
	3	PC350 video – Plane 1 memory failure
	4	PC350 video – Vertical retrace failure
	5	PC350 video – Counter register failure
	6	PC350 video – Plane 1 control, X, Y, or pattern register failure
	7	PC350 video – Plane 1 scroll register failure
	103	PC350 EBO – Plane 2 memory failure
	106	PC350 EBO – Plane 2 control failure
	107	PC350 EBO – Plane 2 scroll register failure
	203	PC350 EBO – Plane 3 memory failure
	206	PC350 EBO – Plane 3 control failure
	207	PC350 EBO – Plane 3 scroll register failure
10050	2	PC380 video – Register failure
	3	PC380 video – Plane 1 memory failure
	4	PC380 video – Vertical retrace failure
	5	PC380 video – Counter register failure
	6	PC380 video – Plane 1 control, X, Y, or pattern register failure
	7	PC380 video – Plane 1 scroll register failure
	103	PC380 EBO – Plane 2 memory failure
	106	PC380 EBO – Plane 2 control failure
	107	PC380 EBO – Plane 2 scroll register failure
	203	PC380 EBO – Plane 3 memory failure
	206	PC380 EBO – Plane 3 control failure
	207	PC380 EBO – Plane 3 scroll register failure

Table A-1 System Error Numbers (Cont)

ID Number	Error Number	Description
20050	2	PC380 video – Register failure
	3	PC380 video – Plane 1 memory failure
	4	PC380 video – Vertical retrace failure
	5	PC380 video – Counter register failure
	6	PC380 video – Plane 1 control, X, Y, or pattern register failure
	7	PC380 video – Plane 1 scroll register failure
	103	PC380 EBO – Plane 2 memory failure
	106	PC380 EBO – Plane 2 control failure
	107	PC380 EBO – Plane 2 scroll register failure
	203	PC380 EBO – Plane 3 memory failure
	206	PC380 EBO – Plane 3 control failure
	207	PC380 EBO – Plane 3 scroll register failure
30050	2	PC380 video – Register failure
	3	PC380 video – Plane 1 memory failure
	4	PC380 video – Vertical retrace failure
	5	PC380 video – Counter register failure
	6	PC380 video – Plane 1 control, X, Y, or pattern register failure
	7	PC380 video – Plane 1 scroll register failure
	103	PC380 EBO – Plane 2 memory failure
	106	PC380 EBO – Plane 2 control failure
	107	PC380 EBO – Plane 2 scroll register failure
	203	PC380 EBO – Plane 3 memory failure
	206	PC380 EBO – Plane 3 control failure
	207	PC380 EBO – Plane 3 scroll register failure
177776	375	Zero identification number occurred for longer than 20 seconds.
177776	377	Non-existent memory trap occurred for longer than 20 seconds.
Any ID	177777	Slot option untested (not displayed).
Any ID	374	Slot option generated identification number, but slot option detection hardware indicates that option is not present.
Any ID	376	Slot option has a bad ROM.

The following table defines the Professional 380 LED display during BSR execution in customer, console, or service mode. Please note that they are displayed in chronological order.

Table A-2 LED Display 1

LED	Definition
○ ○ ○ ○	System module
○ ○ ○ ●	Memory daughterboard
○ ○ ○ ○	System module
○ ○ ● ○	EBO daughterboard
● ● ● ○	Slot 1
● ● ○ ●	Slot 2
● ● ○ ○	Slot 3
● ○ ● ●	Slot 4
● ○ ● ○	Slot 5
● ○ ○ ●	Slot 6
● ● ● ●	Power-up self-test complete

● means the light is off.
○ means the light is on.

The following table defines the Professional 380 light display during BSR execution in manufacturing mode. Please note that they are displayed in chronological order.

Table A-3 LED Display 2

LED	Definition
○ ○ ○ ○	J11
○ ○ ○ ●	Onboad memory
○ ○ ● ○	Memory daughterboard
○ ○ ● ●	Interrupts
○ ● ○ ○	Clock and battery backed-up RAM
○ ● ○ ●	Communication interface
○ ● ● ○	Manual input device interface
○ ● ● ●	Printer interface
● ○ ○ ●	Plane memory
● ○ ● ○	Video gate array
● ○ ● ●	Plane 2 memory
● ● ○ ○	EBO 1 gate array
● ● ○ ●	Plane 3 memory
● ● ● ○	EBO 2 gate array
● ○ ○ ○	Slots (excluding on board video)
● ● ● ●	Power-up self-test complete

● means the light is off.
○ means the light is on.

The following table defines the Professional 380 light display after BSR execution in customer or console mode. Please note that they are displayed in a prioritized order where the most significant error takes precedence.

Table A-4 LED Display 3

LED	Definition
○ ○ ○ ○	System module
○ ○ ● ●	Unexpected interrupt or trap
○ ○ ○ ●	Memory daughterboard
○ ○ ● ○	EBO daughterboard
● ● ● ○	Slot 1
● ● ○ ●	Slot 2
● ● ○ ○	Slot 3
● ○ ● ●	Slot 4
● ○ ● ○	Slot 5
● ○ ○ ●	Slot 6
○ ● ● ○	Manual input device failure
○ ● ○ ●	No boot found
○ ● ○ ○	Video monitor not detected
● ○ ○ ○	Reserved
○ ● ● ●	Reserved
● ● ● ●	No errors detected

● means the light is off.
○ means the light is on.

The following is a table of bugcheck codes defined for P/OS V2.0. A bugcheck occurs after the system is booted and is recognizable by the picture of the Professional computer system with nothing highlighted and two numbers (the Professional 380 has eight numbers) on the right side of the screen.

Table A-5 Bugcheck Codes

Code	Code Number	Definition
BF.PKS	000100/??????	P/OS keyboard handler
BF.TTD	000200/??????	Terminal driver
BF.PTS	1004??/??????	P/OS terminal subsystem
BF.EXE	000300/??????	Exec – SSTSR, general
BE.IOT	000300/000000	IOT in system state
BE.STK	000300/000001	Stack overflow
BE.BPT	000300/000002	Trace trap or breakpoint
BE.ILI	000300/000003	Illegal instruction trap
BE.ODD	000300/000004	Odd address or other trap 4
BE.SGF	000300/000005	Segment fault
BE.NPA	000300/000006	A task on P/OS without a parent (aborted)
BE.EMT	000300/000007	EMT trap
BE.TRP	000300/000010	TRAP trap
BF.UP	000400/??????	System startup processing
BE.IN1	000400/000001	Can't install task CBOOT
BE.SP1	000400/000002	Can't spawn task CBOOT
BE.SP2	000400/000003	Can't spawn task CMAIN
BE.FNF	000400/000007	Required file not found
Professional/DECnet startup failure codes		
BE.DSC	000400/000010	DSR corrupt
BE.BDP	000400/000011	Bad dispatch
BE.NWB	000400/000012	No way to boot via DECNA
BE.DAF	000400/000013	DSR allocation failure
BE.VIU	000400/000014	DDM vector in use
BE.NPD	000400/000015	Required PDV not found
BE.NSD	000400/000016	Required hardware not present

The following table is a list of the device ID's for the Professional 300 Series Computer System.

Table A-6 Device Identification Codes

ID (octal)	Device Name
000000	Nothing present
000001	LK201 keyboard
000011	Professional 350 base processor (F11, MMU)
000012	Professional 350 floating point processor (FPP)
000013	Reserved by Digital
000014	Reserved by Digital
000015	Reserved by Digital
000016	Reserved by Digital
000017	Professional 350, 380 printer port
000020	Professional 350, 380 speaker control
000021	Professional 350, 380 communication port
000022	Reserved by Digital
000023	Professional 350, 380 time/date clock
000024	Professional 350, 380 nonvolatile RAM (NVR)
000025	Professional 350 interrupt controller
000026	Professional 350 DIAG/ROM version 1.0 (first release)
000027	Professional 350, 380 maintenance console port
000030	Professional 350, 380 option present register
000031	Professional 350, 380 serial number ROM
000032	Professional 350, 380 monitor attachment
000033	Professional 350, 380 primary RAM
000034	CTI Bus option RAM (256 Kbytes)
000035	Professional 380 base processor (J11, MMU)
000036	Professional 380 interrupt controller
000037	Professional 380 base system ROM version 1.0 (BSR) (first release)
000040	Reserved by Digital
000041	CTI telephone management service (TMS)
000042	CTI Ethernet controller (DECNA)
000043	CTI Z80/CPM option
000044	Reserved by Digital
000045	Professional 380 IVIS base module set
000046	IDLDR IEEE option
000047	KANJI font module
000050	Professional 380 bit map controller (integrated on system module)
000051	DRC11-AA parallel interface

Table A-6 Device Identification Codes (Cont)

ID (octal)	Device Name
000052	DLC11-AA serial interface
000053	ARC11-AA analog interface
000054	MRC11-AA ROM option
000056	Reserved
000060	DECtouch module (DTM)
000061	Reserved
000064	CTI Bus quad serial line option
000066	Reserved
000074	Reserved
000075	Professional 380 IVIS 2000 controller board
000076	Reserved by Digital
000101	Reserved
000104	Reserved
000401	CTI Bus 5 1/4" Winchester disk controller
001002	Professional 350 CTI Bus video bit map controller
001403	Professional 350 CTI Bus extended bit map (EBO – color option)
002004	CTI Bus RX50 5 1/4" floppy diskette controller
002405	Reserved by Digital
003006	Professional 350 IVIS system module
010012	Professional 380 floating point (integrated in the J11)
010026	Professional 350 DIAG/ROM version 2.0 (IVIS)
010050	Professional 350 extended bit map (EBO – color daughter module)
011002	Professional 350 IVIS bit map base module
011403	Professional 350 IVIS extended bit map (color)
030050	Reserved by Digital
040001	Tempest keyboard (shielded)
176775	Experimental ID (with identical bytes)
177376	Experimental ID (with identical bytes)
177775	Experimental ID
177776	Option present but could not read ID
177777	Escape ID (will be used after all IDs are exhausted)

NOTE

Consult price list for option availability. The options listed above indicate used ID codes, but is not a commitment by Digital to sell the options.

The following table contains the I/O and DSW codes.

Table A-7 I/O and DSW Codes

Signal	Decimal	Octal	Definition
IE.BAD	−01	177777	Bad parameters
IE.IFC	−02	177776	Invalid function code
IE.DNR	−03	177775	Device not ready
IE.VER	−04	177774	Parity error on device
IE.ONP	−05	177773	Hardware option not present
IE.SPC	−06	177772	Illegal user buffer
IE.DNA	−07	177771	Device not attached
IE.DAA	−08	177770	Device already attached
IE.DUN	−09	177767	Device not attachable
IE.EOF	−10	177766	End of file detected
IE.EOV	−11	177765	End of volume detected
IE.WLK	−12	177764	Write attempted to locked unit
IE.DAO	−13	177763	Data overrun
IE.SRE	−14	177762	Send/receive failure
IE.ABO	−15	177761	Request terminated (see table at end)
IE.PRI	−16	177760	Privilege violation
IE.RSU	−17	177757	Sharable resource in use
IE.OVR	−18	177756	Illegal overlay request
IE.BYT	−19	177755	Odd byte count (or virtual address)
IE.BLK	−20	177754	Logical block number too large
IE.MOD	−21	177753	Invalid UDC module #
IE.CON	−22	177752	UDC connect error
IE.NOD	−23	177751	Caller's nodes exhausted
IE.DFU	−24	177750	Device full
IE.IFU	−25	177747	Index file full
IE.NSF	−26	177746	No such file
IE.LCK	−27	177745	Locked from read/write access
IE.HFU	−28	177744	File header full
IE.WAC	−29	177743	Accessed for write
IE.CKS	−30	177742	File header checksum failure
IE.WAT	−31	177741	Attribute control list format error
IE.RER	−32	177740	File processor device read error
IE.WER	−33	177737	File processor device write error
IE.ALN	−34	177736	File already accessed on LUN
IE.SNC	−35	177735	File ID, file number check
IE.SQC	−36	177734	File ID, sequence number check
IE.NLN	−37	177733	No file accessed on LUN
IE.CLO	−38	177732	File was not properly closed
IE.NBF	−39	177731	OPEN – no buffer space available for file
IE.RBG	−40	177730	Illegal record size

Table A-7 I/O and DSW Codes (Cont)

Signal	Decimal	Octal	Definition
IE.NBK	−41	177727	File exceeds space allocated, no blocks
IE.ILL	−42	177726	Illegal operation on file descriptor block
IE.BTP	−43	177725	Bad record type
IE.RAC	−44	177724	Illegal record access bits set
IE.RAT	−45	177723	Illegal record attributes bits set
IE.RCN	−46	177722	Illegal record number - too large
IE.ICE	−47	177721	Internal consistancy error
IE.2DV	−48	177720	Rename - 2 different devices
IE.FEX	−49	177717	Rename - new file name already in use
IE.BDR	−50	177716	Bad directory file
IE.RNM	−51	177715	Can't rename old file system
IE.BDI	−52	177714	Bad directory syntax
IE.FOP	−53	177713	File already open
IE.BNM	−54	177712	Bad file name
IE.BDV	−55	177711	Bad device name
IE.BBE	−56	177710	Bad block on device
IE.DUP	−57	177707	ENTER – duplicate entry in directory
IE.STK	−58	177706	Not enough stack space (FCS or FCP)
IE.FHE	−59	177705	Fatal hardware error on device
IE.NFI	−60	177704	File ID was not specified
IE.ISQ	−61	177703	Illegal sequential operation
IE.EOT	−62	177702	End of tape detected
IE.BVR	−63	177701	Bad version number
IE.BHD	−64	177700	Bad file header
IE.OFL	−65	177677	Device off line
IE.BCC	−66	177676	Block check, CRC, or framing error
IE.ONL	−67	177675	Device online
IE.NNN	−68	177674	No such node
IE.NFW	−69	177673	Path lost to partner, this code must be odd
IE.DIS	−69	177673	Path lost to partner, disconnected (Same as NFW)
IE.BLB	−70	177672	Bad logical buffer
IE.TMM	−71	177671	Too many outstanding messages
IE.NDR	−72	177670	No dynamic space available, see also IE.UPN
IE.URJ	−73	177667	Connection rejected by user
IE.NRJ	−74	177666	Connection rejected by network
IE.EXP	−75	177665	File expiration date not reached
IE.BTF	−76	177664	Bad tape format
IE.NNC	−77	177663	Not ANSI 'D' format byte count
IE.NDA	−78	177662	No data available
IE.NLK	−79	177661	Task not linked to specified ICS/ICR interrupts

Table A-7 I/O and DSW Codes (Cont)

Signal	Decimal	Octal	Definition
IE.NST	−80	177660	Specified task not installed
IE.FLN	−81	177657	Device offline when offline request was issued
IE.IES	−82	177656	Invalid escape sequence
IE.PES	−83	177655	Partial escape sequence
IE.ALC	−84	177654	Allocation failure
IE.ULK	−85	177653	Unlock error
IE.WCK	−86	177652	Write check failure
IE.NTR	−87	177651	Task not triggered
IE.REJ	−88	177650	Transfer rejected by receiving CPU
IE.FLG	−89	177647	Event flag already specified
IE.DSQ	−90	177646	Disk quota exceeded
IE.IQU	−91	177645	Inconsistent qualifier usage
IE.RES	−92	177644	Circuit reset during operation
IE.TML	−93	177643	Too many links to task
IE.NNT	−94	177642	Not a network task
IE.TMO	−95	177641	Timeout on request, see also IS.TMO
IE.CNR	−96	177640	Connection rejected
IE.UKN	−97	177637	Unknown name
IE.SZE	−98	177636	Unable to size device
IE.MII	−99	177635	Media inserted incorrectly
IE.SPI	−100	177634	Spindown ignored
IS.PND	+00	0	Operation pending
IS.SUC	+01	1	Operation complete, success
IS.TNC	+02	2	Successful transfer but message truncated (receive buffer too small)
IS.DAO	+02	2	Successful but with data overrun (not to be confused with IE.DAO)
TTY success codes Low order byte is IS.SUC, high order byte is the termination character			
IS.CR	+3329	006401	Carriage return was terminator
IS.ESC	+6913	015401	Escape (altmode) was terminator
IS.CC	+769	001401	Control-C was terminator
IS.ESQ	−25855	115401	Escape sequence was terminator
IS.PES	−32767	100001	Partial escape sequence terminator
IS.EOT	+1025	002001	EOT was terminator (block mode input)
IS.TAB	+2305	004401	Tab was terminator (forms mode input)
IS.TMO	+2	000002	Request timed out

Table A-7 I/O and DSW Codes (Cont)

Signal	Decimal	Octal	Definition
IE.ABO related codes for mount/dismount failures			
AE.SYN	+07	000007	Syntax error
AE.NHM	+10	000012	Home block not found
AE.WRV	+11	000013	Wrong volume
AE.CHK	+12	000014	Checkpoint file still active
AE.SHA	+13	000015	Shadow recording still active
AE.MDM	+14	000016	Volume already marked for dismount
AE.MNT	+15	000017	Volume not mounted
AE.F11	+16	000020	Volume already mounted FILES-11
AE.FOR	+17	000021	Volume already mounted foreign
Directive Error Codes			
IE.UPN	−01	177777	Insufficient dynamic storage, see also IE.NDR
IE.INS	−02	177776	Specified task not installed
IE.PTS	−03	177775	Partition too small for task
IE.UNS	−04	177774	Insufficient dynamic storage for send
IE.ULN	−05	177773	Unassigned LUN
IE.HWR	−06	177772	Device handler not resident
IE.ACT	−07	177771	Task not active
IE.ITS	−08	177770	Directive inconsistent with task state
IE.FIX	−09	177767	Task already fixed/unfixed
IE.CKP	−10	177766	Issuing task not checkpointable
IE.TCH	−11	177765	Task is checkpointable
IE.RBS	−15	177761	Receive buffer is too small
IE.PRI	−16	177760	Privilege violation
IE.RSU	−17	177757	Resource in use
IE.NSW	−18	177756	No swap space available
IE.ILV	−19	177755	Illegal vector specified
IE.ITN	−20	177754	Invalid table number
IE.LNF	−21	177753	Logical name not found

Table A-7 I/O and DSW Codes (Cont)

Signal	Decimal	Octal	Definition
Codes −22 through −79 are reserved.			
IE.AST	−80	177660	Directive issued/not issued from AST
IE.MAP	−81	177657	Illegal mapping specified
IE.IOP	−83	177655	Window has I/O in progress
IE.ALG	−84	177654	Alignment error
IE.WOV	−85	177653	Address window allocation overflow
IE.NVR	−86	177652	Invalid region ID
IE.NVW	−87	177651	Invalid address window ID
IE.ITP	−88	177650	Invalid TI parameter
IE.IBS	−89	177647	Invalid send buffer size (.GT. 255.)
IE.LNL	−90	177646	LUN locked in use
IE.IUI	−91	177645	Invalid UIC
IE.IDU	−92	177644	Invalid device or unit
IE.ITI	−93	177643	Invalid time parameters
IE.PNS	−94	177642	Partition/region not in system
IE.IPR	−95	177641	Invalid priority (.GT. 250.)
IE.ILU	−96	177640	Invalid LUN
IE.IEF	−97	177637	Invalid event flag (.GT. 64.)
IE.ADP	−98	177636	Part of DPB out of user's space
IE.SDP	−99	177635	DIC or DPB size invalid
Success codes from directives – placed in the directive status word.			
IS.CLR	0	0	Event flag was clear
IS.SET	2	2	Event flag was set
IS.SPD	2	2	Task was suspended
IS.SUP	3	3	Logical name superseded

These are the errors from POSSUM. These codes are returned in word 1 of the status block upon return from a POSSUM call.

Table A-8 POSSUM Error Codes

Code	Code Number	Definition
+1	000001	Success
−1	177777	Directive error (word 2 contains $DSW)
−2	177776	I/O status error (word 2 = IOSB, word 3 = IOSB+2)
−3	177775	RMS error (word 2 contains STS, word 3 contains = STV)
−4	177774	Server specific error, codes returned in words 2 through 7
−5	177773	Interface error, specific error in word 2

Interface error subcodes are returned in word 2 and are as follows.

−1	177777	Feature not supported
−2	177776	Impure area invalid, missing
−3	177775	Invalid number of parameters (too few/too many)
−4	177774	Server not installed (server name in words 2 and 3)
−5	177773	Illegal device specification
−6	177772	User buffer too small for returned data
−7	177771	POSSUM/task incompatibility error – relink task

NOTE
PROATR and PRODIR have no server specific error codes.

These are the server specific error codes from PROFBI.

+ 1	000001	Success
− 1	177777	Illegal device
− 2	177776	Device not in system
− 3	177775	Failed to attach device
− 4	177774	Block 0 bad - disk unusable
− 5	177773	At least one of LBNs 0-25 is bad. Can't initialize.
− 6	177772	Bad block file overflow
− 7	177771	Unrecoverable error
− 8	177770	Device write locked
− 9	177767	Device not ready
−10	177766	Failed to write bad block file
−11	177765	Privilege violation
−12	177764	Device is an alignment cartridge
−13	177763	Fatal hardware error
−14	177762	Allocation failure

Table A-8 POSSUM Error Codes (Cont)

Code	Code Number	Definition
−15	177761	I/O error sizing device
−16	177760	Allocation for sys file exceeds volume limit
−17	177757	Homeblock allocate write error
−18	177756	Bootblock write error – disk unusable
−19	177755	Index file bitmap I/O error
−20	177754	Bad block header I/O error
−21	177753	MFD file header I/O error
−22	177752	Null file header I/O error
−23	177751	Checkpoint file header I/O error
−24	177750	MFD write error
−25	177747	Storage bitmap file header I/O error
−26	177746	Failed to read bad block descriptor file
−27	177745	Volume name too long
−28	177744	Unrecognized disk type
−29	177743	Preallocation insufficient to fill first index file header
−30	177742	Preallocated too many headers for single header index file
−31	177741	Preallocation insufficient to fill 1st, 2nd index file headers
−32	177740	Bad block limit exceeded for device
−33	177737	Driver not resident
−34	177736	Bitmap too large - increase cluster factor
−35	177735	Storage bitmap I/O error
−36	177734	Homeblock I/O error
−37	177733	Index file header I/O error
−38	177732	Dismount of device failed
−39	177731	Cannot mount device foreign
−40	177730	Cannot mount device FILES-11
−41	177727	Cannot format DZ - no software support
−42	177726	Cannot detach device
−43	177725	Checkpoint file header overflow,specify smaller checkpoint file
−44	177724	Illegal character(s) in volume name
−45	177723	Cannot format DZ – no hardware support
−46	177722	Cannot format DZ – speed out of range
These are the server specific error codes from PROLOG.		
−1	177777	Error in parsing the SET DEFAULT string.
−2	177776	Cannot determine type of service requested.

Table A-8 POSSUM Error Codes (Cont)

Code	Code Number	Definition
These are the server specific error codes from PROTSK.		
+ 1	000001	Successful install
− 1	177777	Task name in use
− 2	177776	File not found
− 3	177775	Specified partition too small
− 4	177774	Task and partition base mismatch
− 7	177771	Length mismatch common block
− 8	177770	Base mismatch common block
− 9	177767	Too many common block requests
−11	177765	Checkpoint area too small
−13	177763	Not enough APRs for task image
−14	177762	File not task image
−15	177761	Base address must be on 4k boundary
−16	177760	Illegal first APR
−18	177756	Common block parameter mismatch
−20	177754	Common block not loaded
−22	177752	Task image virtual address overlaps common block
−23	177751	Task image already installed
−24	177750	Address extensions not supported
−26	177746	Checkpoint space too small, using checkpoint file
−27	177745	No checkpoint space, assuming not checkpointable
−29	177743	Illegal UIC
−30	177742	No pool space
−31	177741	Illegal use of partition or region
−32	177740	Access to common block denied
−33	177737	Task image I/O error
−34	177736	Too many LUNs
−35	177735	Illegal device
−36	177734	Task may not be run
−37	177733	Task active
−39	177731	Task fixed
−40	177730	Task being fixed
−41	177727	Partition busy
−43	177725	Common/task not in system
−44	177724	Region or common fixed
−45	177723	Can't do receive from requestor

Table A-8 POSSUM Error Codes (Cont)

Code	Code Number	Definition
−46	177722	Can't attach to requestor
−47	177721	Invalid request
−48	177720	Can't return result parameter
−49	177717	Error encountered on file open operation
−50	177716	Error encountered on file close operation
−51	177715	Can't get file LBN to process label blocks
−52	177714	No taskname specified in batch request, no name in label block
−53	177713	Unable to create or map to region
PROVOL has the following server specific error codes.		
−1	177777	File is not a system image
−2	177776	Invalid boot device

The following table shows the MS-DOS power up error codes.

Table A-9 MS-DOS Error Codes

Error Codes (octal)	
Code Number	**Definition**
1	Diag is too big or loaded too high
2	Diag exited without setting status
3	Unexpected NXM trap
4	NXM trap referencing CSR's
5	NXM trap referencing 8086 memory
6	Can't load 8086 program in reset vector
7	Program changed by running it
10	Program didn't run or change memory
11	Bad 8086 memory
12	Program killed by memory test
Error codes defined by the base system module.	
374	Device not in "option present" register
375	ID read as 0
376	Error check failed on contents of ROM on device
377	Bus time out trap reading device ID

Printed in U.S.A.
EK-PC300-VI-001