UP1100
Technical Reference Manual

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SAMSUNG ELECTRONICS

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Revision History

Date	Rev	Description
05/31/00	**51-0049-1A**	**UP1100 Technical Reference Manual first product release. This document supports the UP1100-600-A product.**

Table of Contents

List of Figures

List of Tables

Preface

Overview

This manual describes the Alpha Processor, Inc. UP1100 product, including Alpha 21264A Processor, the AMD-751 System Controller and the ALI M1535D PCI-ISA Bridge.

Audience

This manual is intended for system designers and others who use the UP1100 to design or evaluate computer systems based on the Alpha 21264A Processor, AMD-751 System Controller and M1535D PCI-ISA Bridge controller chips.

Scope

This manual describes the features, configuration, functional operation, and interfaces of the UP1100. This manual does not include specific details on industry standards (for example, on PCI or ISA bus specifications). Additional information is available in the appropriate vendor and IEEE specifications. See Appendix B for information on how to order related documentation and obtain additional technical support.

Manual Organization

The UP1100 Technical Reference Manual is organized as follows:

- A functional description of the UP1100 is provided in Chapter 1, “Functional Description.” This includes a description of the subsystem designs for the UP1100.
- Chapter 2, “Firmware Platform,” provides a description of the UP1100 firmware platform.
- Chapter 3, “System Memory and Address Mapping,” describes the memory subsystem and address mapping for the UP1100.
- A description of all signals used in the UP1100, organized by function, are provided in Appendix A, “Signal Descriptions.”
- Appendix B, “Support, Products and Documentation,” describes how to obtain technical information and support for the UP1100, and where to order parts and accessories for the UP1100. It includes information

on how to obtain Alpha Processor, Inc. products and supporting literature.

Conventions and Definitions

This section defines product-specific terminology, abbreviations, and other conventions used throughout this manual.

Typographic Conventions

This manual uses the following type conventions:

- Variable information and document titles appear in *italic* type.
- Text that you type is shown in **`bold Courier font`**.
- Type that appears on a screen, such as an example of computer output, is shown in `Courier font`.
- Two key names joined with a forward slash are simultaneous keystrokes. Press down the first key while you type the second key, as in press Ctrl/S.

Signals and Bits

- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by Alpha Processor, Inc. for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes to these registers, it must first read the register and change only the non-reserved bits before writing back to the register.

Data

The following list defines data terminology:

- Units
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.

- Abbreviations—The following notation is used for bits and bytes:
  - Kilo—K, as in 4-Kbyte page (2^{10})
  - Mega—M, as in 4 Mbits / sec (2^{20})
  - Giga—G, as in 4 Gbytes of memory space (2^{30})

Acronyms

The following is a list of the acronyms used in this document and their definitions.

Abbreviation	Meaning
AGP	**Advanced Graphics Port**
ALI	Acer Laboratories, Inc.
AMD	**Advanced Micro Devices, Inc.**
APIC	Advanced Programmable Interrupt Controller
CE	**European Conforming**
CD	Compact Disk
COM	**Communications**
CPU	Central Processing Unit
cUL	**Canadian Underwriters Laboratory**
DDR	Double Data Rate
DIMM	**Dual Inline Memory Module**
DIP	Dual Inline Package
DQM	**Data Input/Output Mask**
ECC	Error Correction Code
EEPROM	**Electrically Erasable Programmable Read-only Memory**
EMI	Electromagnetic Interference
EPLD	**Electrically Programmable Logic Device**
FCC	Federal Communications Commission
FDD	**Floppy Disk Drive**
GART	Graphics Address Relocation Table
HDD	**Hard Disk Drive**
HSTL	High Speed Transceiver Logic
I^2C	**Inter-integrated Circuit**
ICS	Integrated Circuit Systems

Abbreviation	Meaning
ID	**Identification**
IDE	Integrated Device Electronics
I/O	**Input/Output**
IRQ	Interrupt Request
ISA	**Industry Standard Architecture**
JEDEC	Joint Electron Device Engineering Council
KBD	**Keyboard**
LED	Light Emitting Diode
MB	**Motherboard**
MUX	Multiplexer
NDA	**Non-disclosure Agreement**
NMI	Non-maskable Interrupt
NVRAM	**Nonvolatile Random Access Memory**
OEM	Original Equipment Manufacturer
OS	**Operating System**
PA	Physical Address
PAL	**Privileged Architecture Library**
PCB	Printed Circuit Board
PCI	**Peripheral Component Interconnect**
PME	Power Management
RAM	**Random Access Memory**
ROM	Read-only Memory
RTC	**Real-time Clock**
SDRAM	Synchronous Dynamic Random Access Memory
SM	**System Management**
SPD	Serial Presence Detect
SROM	**Serial Read-only Memory**
SRM	System Reference Manual
SSRAM	**Synchronous SRAM**
UART	Universal Asynchronous Receiver / Transmitter
UL	**Underwriters Laboratory**
USB	Universal Serial Bus
VID	**Voltage Identification**
VRM	Voltage Regulator Module

Chapter 1 Functional Description

This chapter describes the functional operation of the UP1100. It introduces the AMD-751 System Controller, and briefly describes its implementation with the M1535D PCI-ISA Bridge peripheral controller and Intel 21143 LAN Controller.

In this chapter, a description is also provided of the UP1100 subsystem structure and logic used.

1.1 System Components

The UP1100 is implemented in industry-standard parts and uses an Alpha 21264A Processor. The functional components of the UP1100 are shown in block diagram form in Figure 1-1.

Note: *Refer to the list of Acronyms on page x of the Preface for an explanation of terminology used in the block diagram.*

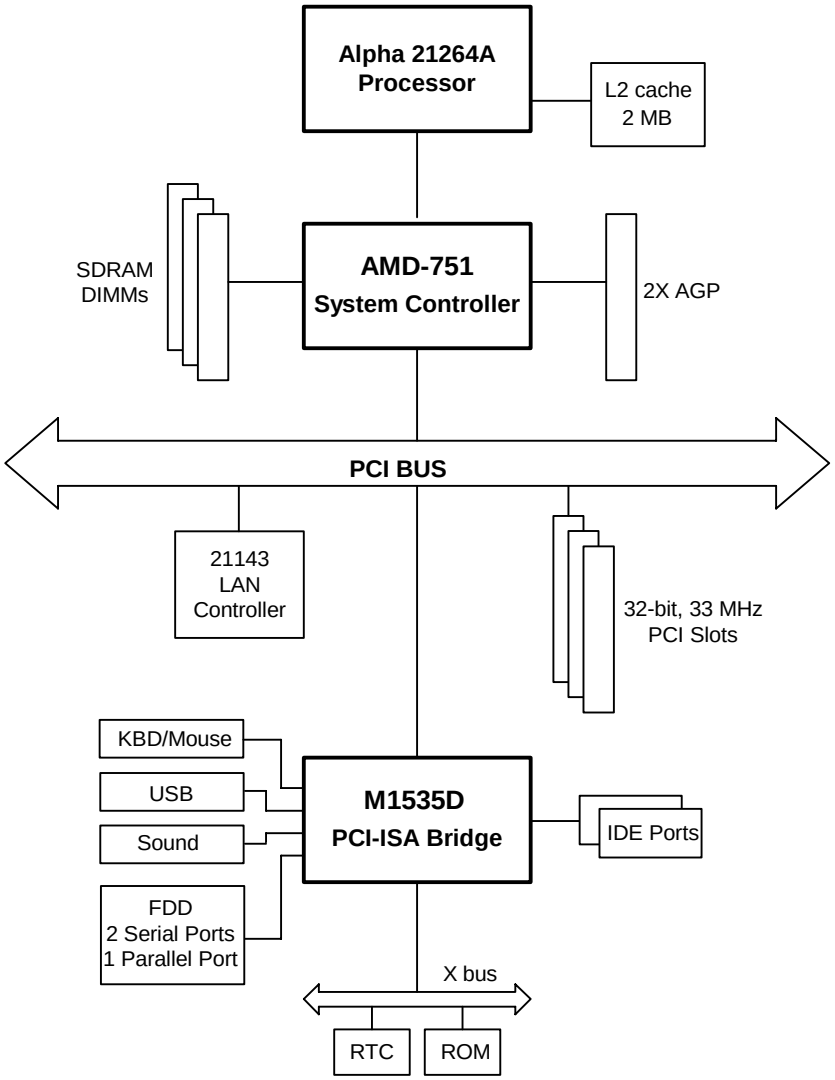

Figure 1-1 UP1100 Functional Block Diagram

1.2 AMD-751 System Controller

The AMD-751 System Controller is the intersection of four buses on the UP1100. These buses are as follows:

- System interface
- PC-100 SDRAM
- PCI
- AGP

The AMD-751 System Controller is responsible for receiving data, addresses, commands, and control signals from one bus domain and translating them into other bus domains. The following sections cover each of the AMD-751 System Controller's bus interfaces, and describe how it translates signals between bus domains.

1.2.1 System Interface

A system interface connects the Alpha 21264A Processor and the AMD-751 System Controller. The system interface contains the following signal groupings:

- SysAddOut
- SysAddIn
- SysData

All three signals groups are transmitted and received using a technique called clock forwarding. Clock forwarding requires the transmitting entity to send a clock with each data or address group. The receiving entity uses the clock to latch the data or address sent from the transmitting entity.

To determining the bus type, the system interface sends the bus cycle type with the address multiple transactions on the SysAddOut bus. This means that the AMD-751 System Controller must parse the SysAddOut packet and break it into physical address and bus type commands. The UP1100 is designed to run the system interface at a clock rate of 100 MHz. The system interface is able to send and receive on both edges of the clock, which means the interface can effectively run at a 200 MHz transfer rate.

1.2.2 Memory Interface

The SDRAM interface on the AMD-751 System Controller is a fully compliant PC-100 interface. The AMD-751 System Controller can accommodate three DIMM slots with each slot able to hold SDRAM modules ranging from 64 MB to 256 MB.

Registers in the AMD-751 System Controller set the physical address mapping for each DIMM slot. These registers are set by the SROM code and the SRM Console during system initialization. A complete description of the UP1100 memory subsystem is provided in Chapter 3, "System Memory and Address Mapping."

1.2.3 PCI Interface

The PCI bus interfaces through the AMD-751 System Controller to the system interface and the SDRAM bus. The AMD-751 System Controller

routes the PCI data to memory when the PCI needs to access the main memory.

The AMD-751 System Controller looks at the physical address (PA) and the command field of SysAddOut, then determines whether a PCI transaction is necessary. See section 3.2, “System Space Address Mapping,” for information on PCI address mapping.

The AMD-751 System Controller determines what type of cycle to place on the PCI bus by decoding the command field. The AMD-751 System Controller supports the following commands:

- WrByte
- WrLWds
- RdBytes
- RdLWds

The transaction command fields issued by the CPU handle legacy x86 special cycles. Special x86 bus cycles are transmitted with a PA of 801 F800 0000 and the WrLWs command. The AMD-751 System Controller then reads the data on the SysData bus to determine what type of special cycle is being transmitted, then places the appropriate action on the PCI bus. Table 1-1 describes the UP1100's legacy special cycles and their corresponding system interface SysData values.

Table 1-1 Special Cycle on the System Interface

Special Cycle	Data Value (SysData[31:0])
Shutdown	**0000 0000**
Halt	0000 0001
WB Invalidate	**0001 0002**
Invalidate	0002 0002
Flush Ack	**0003 0002**
Stopgrant	0012 0002

1.2.4 PCI Slots

The UP1100 has three PCI slots, with identification (ID) selects that are tied directly to the connectors. All unused features, such as JTAG, are pulled up or down. The new Power Management (PME) feature is supported on the PCI connectors. The PME pin is connected to all PCI connectors and

the AGP connector, and the signal is then routed to enable interrupt generation. Table 1-2 contains a list of PCI request and selection IDs for the UP1100.

Table 1-2 PCI Request and Selections for Slots and Devices

Device	IDsel	Req/Gnt Pair	IRQ-A	IRQ-B	IRQ-C	IRQ-D
PCI Slot 0	**AD19**	**0**	**Int A**	**Int B**	**Int C**	**Int D**
PCI Slot 1	AD20	1	Int B	Int C	Int D	Int A
PCI Slot 2	**AD21**	**2**	**Int C**	**Int D**	**Int A**	**Int B**
M1535D PCI-ISA Bridge	AD18	PREQ / PGNT	See Table 1-4.			
M1535D PCI-ISA Bridge	**AD28**	**PREQ/ PGNT**	**See Table 1-4.**			
M1535D PCI-ISA Bridge	AD31	PREQ / PGNT	See Table 1-4.			
AMD-751 System Controller	**AD11**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
AMD-751 System Controller (AGP)	AD12	N / A	IntA	IntB	N / A	N / A

1.2.5 AGP Interface

The AMD-751 System Controller implements a fully-compliant AGP bus, and provides a register for managing AGP memory. AGP registers used in the AMD-751 System Controller consist of the following:

- AGP Base Address
- Graphics Address Relocation Table (GART)
- Capability
- Status
- Command
- Virtual Address Size
- AGP / GART Mode

The Virtual Base Address register's value is the bottom address in the system interface domain were the AGP memory starts. The Virtual Address Size register summed with the AGP Base Address provides the top of the AGP address range on the system interface. GART translates the system interface PA to main memory.

1.2.6 Clock Generator

The UP1100 uses a two-chip clock solution from Integrated Circuit Systems (ICS). The first chip (ICS9248-64) generates the clocks for the CPU, AGP, and PCI. The second chip (ICS9179-06) is a zero-delay buffer which takes a reference clock from the AMD-751 System Controller and generates the SDRAM clocks.

1.3 M1535D PCI-ISA Bridge

The M1535D PCI-ISA Bridge works as a bridge between the PCI and ISA buses, providing fully PCI- and ISA-compatible functions. It also has a set of features to control legacy peripheral devices, with an integrated Super I/O and a keyboard controller. And it also contains Sound Blaster compatible sound controller logic.

1.3.1 IDE Interface

An on-chip IDE controller supports two separate IDE connectors for up to four IDE devices, providing an interface for IDE hard disk drives and CD ROM drives. UP1100 implements the Ultra Direct Memory Access (Ultra DMA) specification which supports a 33/66MB per second transfer rate.

1.3.2 Super I/O Interface

The on-chip Super I/O incorporates a floppy disk controller, one parallel port, and two UART ports. In the UP1100, COM1 and COM2 are implemented. A parallel port implements standard mode, enhanced mode, and high speed mode functions. It is compliant to SPP, PS/2, EPP, ECP, and 1284 standards. The floppy disk controller can support up to 1 Mbps data transfer rates and a three-mode 3.5 inch drive.

1.3.3 Sound Interface

The on-chip sound controller is fully compatible with Sound Blaster. It also supports AC-97 CODEC 2.2.

1.3.4 USB Interface

UP1100's M1535D PCI-ISA Bridge supports three USB ports. Two ports are dedicated external ports, and the third port is connected to the AGP.

1.3.5 SM Bus Interface

The M1535D PCI-ISA Bridge acts as the system management bus host. It communicates with system devices, such as the following:

- the temperature sensor beside the Alpha microprocessor that senses system power voltages and fan speeds
- DIMMs
- revision Electrically Erasable Programmable Read-only Memory (EEPROMs)

The UP1100 has one main SM bus and two sub-SM buses. Access to the sub-SM bus is controlled by a multiplexer (MUX) which sits on the main SM bus. The SM bus from the LM75 connects the first sub-SM bus; the DIMM EEPROMs are connected to the second sub-SM bus.

SM bus addresses for all UP1100 devices are provided in Table 1-3.

Table 1-3 SM Bus Address of Each Device

Device	Address
ADM 9240 (System Management Unit)	**0101 100X**
ICS9179-06 (Zero delay clock buffer)	1101 001X
PCF8574AT(I2C bus MUX controller)	**0111 010X**
PCF8582 (MB revision EEPROM)	1010 100X
LM75 (Thermal Detector for Alpha 21264A Processor)	**1001 111X**
DIMM0	1010 000X
DIMM1	**1010 001X**
DIMM2	1010 010X

1.3.6 IRQs

The M1535D PCI-ISA Bridge is a PC98 design which provides the functionality recommended to support Windows 95. Through internal configuration registers, each of the following are programmable:

- Logic device I/O address
- DMA channel
- Interrupt Requests (IRQs)

There are 128 I/O address location options, 12 IRQ options, and three

DMA channel options for each logical device except the keyboard. Two extra IRQ lines are provided, as well as an ISA IRQ which is steerable to any ISA IRQ. IRQs for the UP1100 are listed in Table 1-4.

Table 1-4 UP1100 IRQs

IRQ	Connection	IRQ	Connection
IRQ0	**PIT**	**IRQ8**	**Real-time Clock (RTC)**
IRQ1	Keyboard	IRQ9	
IRQ2	**Cascade of INT-CTRL2**	**IRQ10**	
IRQ3	COM2	IRQ11	
IRQ4	**COM1**	**IRQ12**	**Mouse**
IRQ5		IRQ13	
IRQ6	**FDD**	**IRQ14**	**Primary IDE**
IRQ7	LPT1	IRQ15	Secondary IDE

1.3.7 DMA

The M1535D PCI-ISA Bridge provides seven programmable DMA channels, four for an 8-bit data size, and three for a 16-bit data size. These seven DMA channels can be arbitrarily programmed as distributed channels.

1.4 Intel 21143 Ethernet Controller

21143 PCI/CardBus 10/100Mb/s Ethernet LAN Controller(21143) is a single chip device that supports direct memory access (DMA) and has direct interfaces to both the CardBus and the PCI local bus. The 21143 is optimized for low power PCI/CardBus based systems

1.5 Flash ROM

The UP1100 has a 2 MB Flash ROM. The M1535D PCI-ISA Bridge supports Flash ROM sizes only up to 512 KB. To use this 2 MB ROM, two general-purpose I/O pins of the M1535D are used to access the 2 MB ROMs as four blocks of 512 KB. This Flash ROM is connected to the ISA bus using only the lower 8-bit data lines.

Table 1-5 defines the flash ROM usage for the 2 MB ROMs.

Table 1-5 Flash ROM Usage

Address Range	Usage
0x0000–10000	**FSB**
50000–5FFFF	SRM Console Nonvolatile Random Access Memory (NVRAM)
60000–16FFFF	**SRM console**
170000–1FFFFF	Reserved

1.6 RTC

The M5819P RTC provides one hundred calendars, a programmable periodic interrupt with a periodic range from 122 ms to 500 ms, and 242 bytes of SRAM.

1.7 System Management Unit

System management (SM) on the UP1100 is implemented using I2C protocol, and is controlled through two devices:

- M1535D PCI-ISA Bridge
- ADM9240, SM device

The M1535D PCI-ISA Bridge acts as the central SM device. All system events are directed to the M1535D PCI-ISA Bridge and then onto the processor through interrupt. The processor then invokes an exception handler. The exception handler allows the M1535D PCI-ISA Bridge to get data from the system management device through the SM bus.

The SM device detects system power voltages and the processor fan speeds, and generates an interrupt when abnormal conditions occurs. A block diagram of the SM function is provided in Figure 1-1.

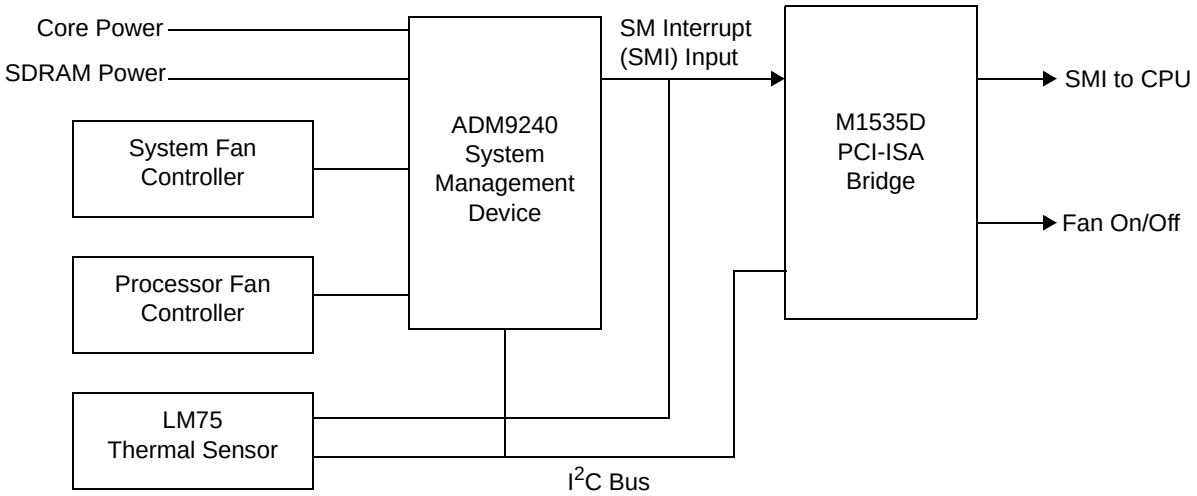

Figure 1-1 System Management Block Diagram

1.8 System Interface Termination Scheme

The UP1100 must terminate all system interface signals. This termination uses a 100Ω pull-up resistor, placed within 1 inch of the AMD-751 System Controller. The pull-up resistor must be placed within 1 inch of the Alpha 21264A Processor, and the serial resistor must be placed close to the pull-up resistor. This termination scheme is shown in Figure 1-2.

The pull-up is done with the VTERM voltage source which supplies the system interface Termination power. The VTERM voltage is 2V.

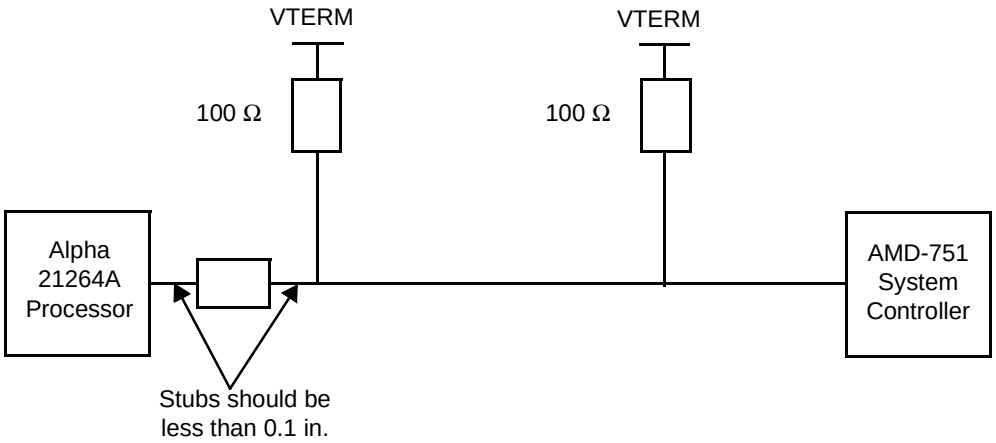

Figure 1-2 System Interface Termination Scheme

1.9 Clock Distribution and Termination

The UP1100 uses a two-chip clock solution, ICS 9248-64 and 9179-06, to generate the following system clocks:

- CPU
- PCI
- AGP
- SDRAM
- AMD-751 System Controller

The 9248-64 generates clocks for the CPU, AGP, PCI, and the AMD-751 System Controller. The 9179-06 is a zero-delay buffer that drives all SDRAM clocks. Processor SysClk and AMD-751 System Controller SysClk are differential clocks. Differential clocks require parallel routing of the positive (CLK_T) and negative (CLK_C) clocks. They also require a matched line-length between the clock high and clock low. In addition to the differential clocks, it is also necessary to match line-lengths of the SysClks to the CPU and the SysClk to the AMD-751 System Controller.

Due to the differential nature of the clock, a unique clock termination scheme is required. Termination resistors must be placed as close as possible to the 9248-64 chip. Figure 1-3 shows a diagram of the clock termination scheme.

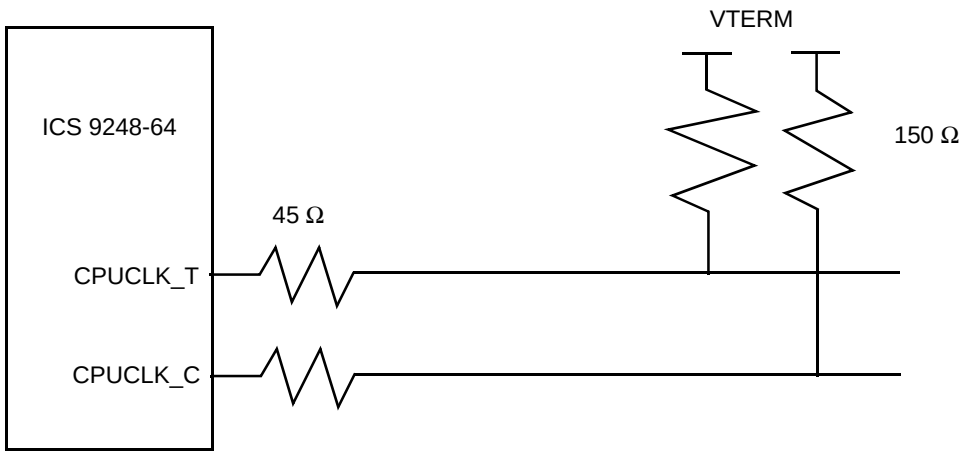

Figure 1-3 Clock Termination Scheme

1.9.1 System Clock

All the following clocks should be matched in length:

- System clocks
- Differential clocks to the processor
- Clock to the AMD-751 System Controller
- PCI clock
- AGP clock

On the UP1100, the differential clock to the processor, the AGP clock and PCI clocks are shorter than the system clock to the AMD-751 System Controller (length A). The compensation of the clock length is as follows:

length (A) = length (B) = length (C + C')

Refer to Figure 1-4 for an diagram of the system clock logic.

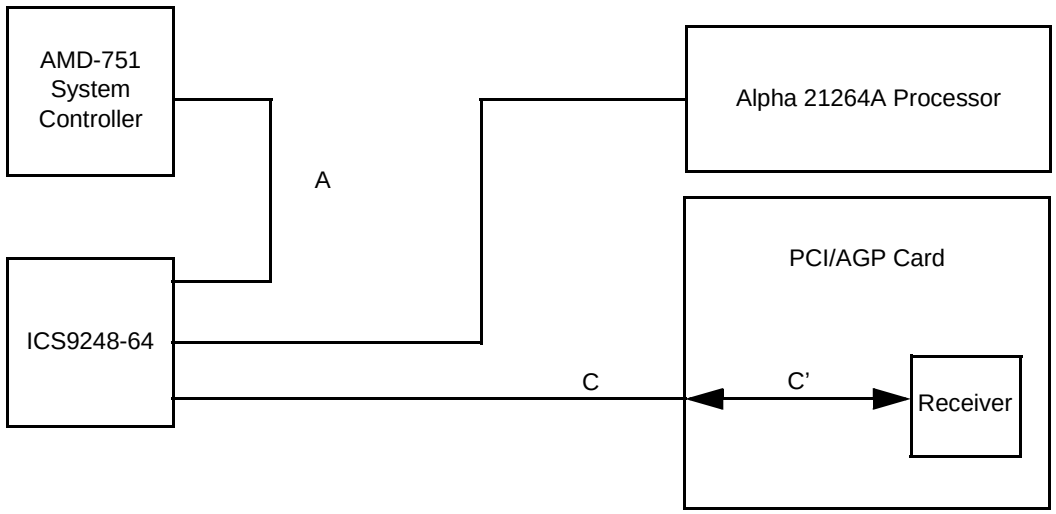

Figure 1-4 System Clock Logic

1.9.2 SDRAM Clock

The ICS9179-06 generates the 12 SDRAM clocks, taking the reference clock from the AMD-751 System Controller. The SDRAM clock tree must be balanced to synchronize the reference clock coming from the AMD-751 System Controller and the clock input pin on each SDRAM module, as follows:

length (Feedback) = length (Reference CLK) + length (SDRAM CLK)
+ length (CLK on DIMM module)

Figure 1-5 shows this logic in diagram form.

length (A) = length (B) + length (C + C')

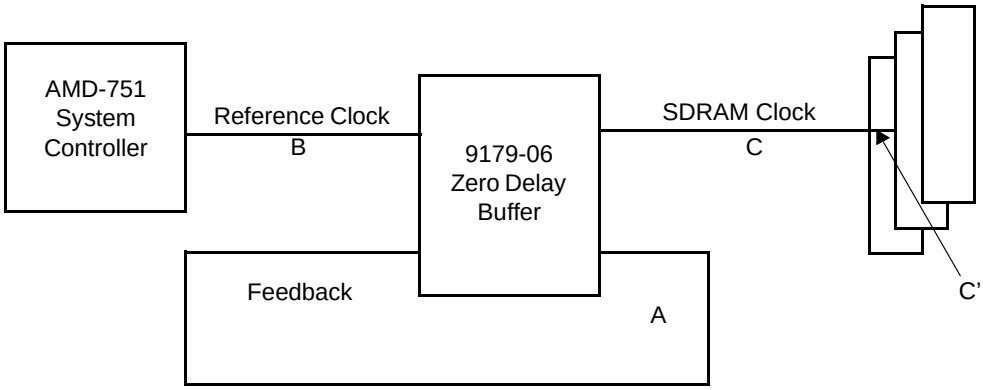

Figure 1-5 SDRAM Clock Logic

1.10 On-board LEDs

Two LEDs on the board indicates some user functionality:

- D24, the green LED, indicates that power to the Alpha 21264A Processor is good.
- D25, the red LED, indicates when SROM codes are loading.

The LEDs are located toward the lower-left edge of the UP1100, and are shown in Figure 1-6.

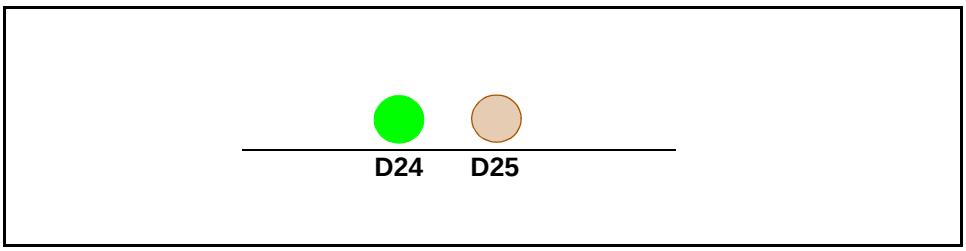

Figure 1-6 LED Status Indicators

Chapter 2 Firmware Platform

This chapter describes the UP1100 target operating system (OS), and the Reset PALcode, Fail Safe Booter (FSB) and System Reference Manual (SRM) Console firmware. A description is included of the order in which firmware loads and the OS boots.

The UP1100 supports the following firmware versions:

- Operating System—Linux kernel 2.2.14 or higher
- Reset PALcode (SROM code)—version X17.9 or higher
- FSB—Release 1.0 or higher
- SRM Console—version A5.6-3 or higher

2.1 Supported OS

The UP1100 supports all Linux kernel versions 2.2.14 and higher in order to boot from SRM A5.6-3 or higher.

Note: *Refer to product support at the Alpha Processor, Inc. web site for current information on specific OS distributors and versions supported by the UP1100.*

2.2 Reset PALcode

When the UP1100 is turned on or reset, Reset PALcode firmware automatically loads into instruction cache (Icache) in the CPU. This code performs the following activities:

1. Initialize CPU.
2. Detect CPU configuration and memory.
3. Initialize Bcache and set chipset CSRs according to configuration.
4. Initialize system memory.
5. Load the next level of firmware and pass control to that code. (See section 2.5, “Firmware Loading Order.”)

The following devices are tested by the Reset PALcode before loading the SRM Console firmware:

- Bcache
- System bus and memory controller
- Memory auto-sizing and initial tests
- Path to ROM via M1535D PCI-ISA Bridge

Note: *Due to constraints of the Reset PALcode module's execution environment, error reporting and interaction with these diagnostics are not user-friendly.*

2.3 FSB

The FSB provides an emergency recovery mechanism when the primary firmware image contained in flash memory is corrupted. When flash memory is corrupted, and no image can be loaded safely from the flash, you can run the FSB and boot another image from a diskette that is capable of reprogramming the flash.

2.4 SRM Console

SRM console is a Unix-style boot firmware for Alpha-based systems. SRM console provides the following service functions:

- Power-up diagnostics and initialization
- Operator interface
- Operating system bootstrap and restart

Booting Linux with the SRM console involves the following steps:

1. Reset PALcode loads and transfers control to SRM Console.
2. SRM Console loads and transfers control to the secondary bootstrap loader.
3. The secondary bootstrap loader sets up the environment for the Linux OS, reads the kernel image from a disk file system, and transfers control to the OS.

Note: *Refer to the* UP1100 User Manual*, P/N 51-0048, for detailed information on installing and booting the OS.*

2.5 Firmware Loading Order

UP1100 firmware loads in the following order:

1. Load Reset PALcode.
2. Load SRM Console firmware.
3. Run OS.

Chapter 3 System Memory and Address Mapping

The following sections describe the UP1100 system memory, and includes a list of valid memory configurations. Mapping information for system addresses is also provided.

3.1 Memory Subsystem

UP1100 memory consists of three 168-pin, PC 100-compliant DIMM sockets. The DIMM modules have an SM bus connection, which accesses a serial EEPROM on the module.

3.1.1 Memory Configurations

The AMD-751 System Controller can support the following size DIMMs:

- 64 MB
- 128 MB
- 256 MB

The UP1100 supports any combination of DIMMs between 64 MB and 768 MB, as shown in Table 3-1.

Table 3-1 UP1100 Memory Configurations

Total Memory	No. of DIMMs	DIMM 1	DIMM 2	DIMM 0
64 MB	**1**	**64 MB**		
128 MB	1	128 MB		
	2	**64 MB**	**64 MB**	
192 MB	2	128 MB	64 MB	
256 MB	**1**	**256 MB**		
	2	128 MB	128 MB	
	3	**128 MB**	**64 MB**	**64 MB**
320 MB	2	256 MB	64 MB	

Note: If only one DIMM module is installed, you must populate DIMM 1 slot first..

Table 3-1 UP1100 Memory Configurations (Continued)

Total Memory	No. of DIMMs	DIMM 1	DIMM 2	DIMM 0
384 MB	**2**	**256 MB**	**128 MB**	
	3	256 MB	64 MB	64 MB
512 MB	**2**	**256 MB**	**256 MB**	
	3	256 MB	128 MB	128 MB
576 MB	**3**	**256 MB**	**256 MB**	**64 MB**
640 MB	3	256 MB	256 MB	128 MB
768 MB	**3**	**256 MB**	**256 MB**	**256 MB**

Note: If only one DIMM module is installed, you must populate DIMM 1 slot first..

3.1.2 Memory Size Detection

The SROM detects the main memory size using a simple write and read procedure to the memory address space.

3.2 System Space Address Mapping

PA space on the system interface maps to PCI space when it is between 1 F800 0000h and 1 FEFF FFFFh. This address range is broken into the specific PCI mapping in Table 3-2.

Table 3-2 System Memory Mapping

Command	Starting Address	Ending Address	Description
Reserved (Masked)	**PA msb=0 and 1 FF00 0000**	**PA msb=0 and 3 FFFF FFFF**	**Reserved for use by the AMD-751 System Controller**
PCI Configuration Space (Masked)	PA msb=0 and 1 FE00 0000	PA msb=0 and 1 FEFF FFFF	This space is used to create PCI configuration cycles using WrBytes, WrLWs, BdBytes, and RdLWs commands only
PCI I/O Space (Masked)	**PA msb=0 and 1 FC00 0000**	**PA msb=0 and 1 FDFF FFFF**	**This space is used to create PCI I/O cycles using WrBytes, WrLWs, RdBytes, and RdLWs commands only.**

Table 3-2 System Memory Mapping (Continued)

Command	Starting Address	Ending Address	Description
PCI IACK / Special Cycle Generation (Masked)	PA msb=0 and 1 F800 0000	PA msb=0 and 1 FBFF FFFF	WrLWs commands to this space are used to create PCI special cycles. The lower 32 bits of the data are passed on to the PCI bus as both the address and data with the special-cycle PCI command. RdBytes commands to this space are used to create PCI IACK. The lower 16 bits of these addresses are passed on to the PCI unmodified with the IACK PCI command.
Reserved (Masked)	**PA msb=0 and 1 0000 0000**	**PA msb=0 and 1 F7FF FFFF**	**Reserved for use by the AMD-751 System Controller.**
PCI Memory Space (Masked)	PA msb=0 and 0 0000 0000	PA msb=0 and 0 FFFF FFFF	The lower 32 bits of these addresses are forwarded, unmodified, to the PCI and are accessed with Wr / RdBytes, Wr / RdLWs, or Wr / RdQWs only.
Normal Memory (Masked Writes)	**PA msb=1 and 0 0000 0000**	**PA msb=1 and 3 FFFF FFFF**	**DRAM, accessed with masked write commands WrBytes, WrLWs, and WrQWs only.**
Reserved (Masked Reads)	PA msb=1 and 0 0000 0000	PA msb=1 3 FFFF FFFF	The AMD-751 System Controller does not support masked reads to this address space.
Reserved (Blocks)	**PA msb=1 and 0 FF00 0000**	**PA msb=1 and 0 FFFF FFFF**	**This address space can be used by the AMD-751 System Controller for undefined purposes.**
Normal Memory (Blocks)	PA msb=0 and 0 0000 0000	PA msb=0 and 3 FFFF FFFF	DRAM accessed with read and write block commands. Note: The AMD-751 System Controller only uses 32 address bits internally and the address space wraps. Address 1 0000 0000 is treated the same as 0 0000 0000.

Appendix A

Signal Descriptions

This section describes all signals present on the UP1100, organized by function.

A.1 System Interface

Table A-1 System Interface Signals

Signal	Description
SYSDATA_N[63:0]	**The bidirectional interface to and from the processor and system for data movement. Data is skew-aligned with either the SDATAINCLK[3:0]# bus or SDATAOUTCLK[3: 0]# bus. Both rising and falling edges are used to transfer data.**
SYSCHECK_N[7:0]	Contains the ECC check bits for data transferred on the SDATA[63:0]# bus.
SYSADDIN_N[14:0]	**The unidirectional system Address/ command interface to the processor from the system. It is used to transfer probes or data movement commands into the processor. All probes and commands on the SADDIN[14:2]# bus are skew-aligned with the forward clock, SADDINCLK#.**
SYSADDOUT_N[14:0]	The unidirectional system address interface from the processor to the AMD-751 System Controller. The SADDOUT[14:2]# bus is used to transfer processor Commands or probe responses to the system. All commands on bus are skew-aligned with the forward clock, SADDOUTCLK#.
SYSDATAINCLK_N[4:0]	**The single-ended forwarded clock driven by the AMD-751 System Controller to transfer data on SDATA[63:0]#. Each 16-bit data word is skew-aligned with this clock. Both rising and falling edges are used to transfer data.**
SYSDATAOUTCLK_N[4:0]	The single-ended forwarded clock driven by the processor and is used to transfer data on the SDATA[63:0]# bus. Both rising and falling edges are used to transfer data.
SYSADDINCLK_N[4:0]	**The single-ended forwarded clock for the SADDIN[14:2]# bus that is driven by the AMD-751 System Controller. Both rising and falling edges are used to transfer addresses or commands (probes) to the processor.**
SYSADDOUTCLK_N[4:0]	The single-ended forwarded clock for the SADDOUT[14:2]# bus driven by the processor. Both rising and falling edges are used to transfer commands or probe responses.
CPUCLKIN_H	**Processor clock.**
CPUCLKIN_L	Processor clock.
FRAMECLK_N	**System Controller clock.**
CLKFWDRST_N	Resets the clock forward circuitry for the processor.
CONNECT_N	**Output from the AMD-751 System Controller, used for power management and clock-forward initialization at reset.**

Table A-1 System Interface Signals (Continued)

Signal	Description
SYSFILLVALID_N	Validate the current memory I/O transfer into the processor.
SYSDATAINVALID_N	**Driven by the AMD-751 System Controller, controls the flow of data into the processor. SDATAINVAL# can be used to introduce an arbitrary number of cycles between octawords (128 bits).**

A.2 AGP

Table A-2 AGP Signals

Signal	Description
AGPCLK1	**A_CLK receives a 66-MHz clock from the system clock generator. A_CLK is used by the AMD-751 System Controller logic in the AGP clock domain.**
AGP_AD[31:0]	In multiplexed mode, A_AD[31:0] contain an AGP address when PIPE# is sampled asserted, and data when PIPE# is sampled negated. In demultiplexed mode, A_AD[31:0] contain only AGP data, while AGP addresses are provided on the sideband address signals SBA[7:0].
AGP_AD_STB[1:0]	**In 2x mode, ADSTB0 provides timing for A_AD[15:0] and ADSTB1 provides timing for A_AD[31:16]. The graphics controller drives the strobes during AGP write operations, and the AMD-751 System Controller drives them during AGP read operations. ADSTB[1:0] serves as a source-synchronized strobe when transferring data in demultiplexed mode. This signal is essentially a copy of the clock that is synchronized to the data. This source-synchronized technique minimizes skew between the strobe and data and compensates for propagation delay. In 1x mode, ADSTB[1:0] is ignored while SYSCLK is used.**
AGP_SB_STB	This signal is used to strobe-in commands on the SBA bus to its request queue.
AGP_TRDY_N	**As an AGP target, the AMD-751 System Controller asserts A_TRDY# to signal the start of a read or write data block transfer. A block is the amount of data that can be passed in four SYSCLK cycles—four doublewords in 1x mode, eight doublewords in 2x mode. If a transfer is larger than one block, A_TRDY# must be reasserted for each block. Asserting A_TRDY# every four clock cycles completes the transfer without wait states. As an AGP initiator, the AMD-751 samples A_TRDY# to determine if data is ready to be transferred.**

Table A-2 AGP Signals (Continued)

Signal	Description
AGP_IRDY_N	AGP_IRDY_N indicates the initiator is ready to transfer a block. For an AGP write transfer, all data in the given transaction is sent without wait-states, so AGP_IRDY_N only needs to be sampled once in the entire transaction. An AGP read transfer can have wait-states, so the AMD-751 must sample AGP_IRDY_N asserted for each block of a read transfer.
AGP_REQ_N	**As the bus arbiter, the AMD-751 System Controller monitors A_REQ# to determine if the graphics controller requests access to the AGP bus. If A_REQ# is sampled asserted, the arbiter asserts A_GNT# as soon as the bus is available.**
AGP_GNT_N	As the AGP bus arbiter, the AMD-751 System Controller asserts A_GNT# in response to A_REQ from the initiator (graphics controller) to indicate to the initiator that it has been granted control of the bus. At the same time, the system controller provides status information on status signals ST[2:0] to indicate to the initiator if it is to supply or receive data in response to a previously queued request.
AGP_PAR	**A_PAR# is used for PCI transfers on the secondary PCI bus. Its function is the same as that of PAR# on the primary PCI bus.**
AGP_PERR_N	Asserted on AGP bus data parity error.
AGP_SERR_N	**Asserted when system error is detected.**
AGP_STOP_N	AGP_STOP_N is used for PCI transfers on the secondary PCI bus. Its function is the same as that of PCI_STOP# on the primary PCI bus. AGP_STOP_N is not used during AGP transfers.
AGP_FRAME_N	**A_FRAME# is used for PCI transfers on the secondary PCI bus. Its function is the same as that of FRAME# on the primary PCI bus.** **A_FRAME# is not used during AGP transfers.**
AGP_DEVSEL_N	A_DEVSEL# is used for PCI transfers on the secondary PCI bus. Its function is the same as that of DEVSEL# on the primary PCI bus. A_DEVSEL# is not used during AGP transfers.
AGP_PIPE_N	**The assertion of PIPE# indicates the beginning of a new bus cycle. The AMD-751 System Controller queues a request from the initiator on each rising clock edge on which it samples PIPE# asserted. When PIPE# is sampled negated, no new requests are queued.**
AGP_RBP_N	An AGP initiator asserts RBF# to indicate that its buffers are full. As an AGP target, the AMD-751 System Controller cannot commence a low priority data read to the initiator until it samples RBF# negated. RBF# does not apply to high-priority read data.
AGP_ST[2:0]	**As the AGP arbiter, the AMD-751 System Controller drives ST[2:0] when it asserts A_GNT# to inform the graphics controller of the type of data being returned or that the AMD-751 is ready to accept a command.**
AGP_USB_N	USB signal.
AGP_USB_P	**USB signal.**

Table A-2 AGP Signals (Continued)

Signal	Description
PCI_PME_N	Power management interrupt signal.
AGP_USBOVCR_N	**Over current detection signal.**
AGPUSB_PWR	USB power.

A.3 PCI

Table A-3 PCI Signals

Signal	Description
PCIRSTJ	**Reset the PCI bus.**
AD[31:0]	The AD[31:0] bus contains the standard, multiplexed PCI address and data lines. AD[31:0] contains a physical address during the first clock of a PCI transaction, and data during subsequent clocks. The address is driven when FRAME# is asserted, and data is driven or received in subsequent cycles. When the AMD-751 System Controller is the PCI initiator, these lines are outputs during the address and write data phases of a transaction, and inputs during read data phases. When the AMD-751 is the PCI target, these lines are inputs during the address and write data phases of a transaction, and outputs during read data phases.
CBEJ[3:0]	**C/BE[3:0]# contain the PCI command during the first clock cycle that FRAME# is asserted. These signals serve as a byte-enable signal for subsequent cycles.**
FRAMEJ	The AMD-751 System Controller asserts FRAME# at the beginning of a PCI cycle when it is the initiator, and holds it asserted until the beginning of the last data transfer in the cycle. If the AMD-751 is the targeted PCI device, it samples and latches the C/BE[3:0]# and AD[31:0] signals and asserts DEVSEL# at the first PCLK edge on which it samples FRAME# asserted.
TRDYJ	**As a PCI initiator, the AMD-751 System Controller samples TRDY# to determine when the target agent is able to complete the data phase of a transaction.** **As a PCI target, the AMD-751 asserts TRDY# to indicate that it has latched the data on AD[31:0] during a write phase or driven data on AD[31:0] during a read phase.**
IRDYJ	IRDY# indicates that a PCI initiator is ready to complete the current data phase of the transaction. During a read cycle, IRDY# asserted indicates the master is ready to accept the data. During a write cycle, IRDY# asserted indicates that write data is valid on AD[31:0]. Data is transferred on the PCI bus on each PCLK in which both IRDY# and TRDY# are asserted. Wait states are inserted on the bus until both IRDY# and TRDY# are asserted together.

Table A-3 PCI Signals (Continued)

Signal	Description
STOPJ	**This signal is asserted when the target device requires it to abort or retry a transaction.**
DEVSELJ	The AMD-751 System Controller samples DEVSEL# when it is the initiator in a PCI cycle to determine if the target device has responded. The AMD-751 drives DEVSEL# when it is the targeted device in a PCI cycle.
SERRJ	**The AMD-751 System Controller, as a PCI agent, asserts SERR# off the rising edge of PCLK one clock after it detects a system error. SERR# is an input to the AMD-756 peripheral bus controller, which can be programmed to generate a Non-maskable Interrupt (NMI).**
PAR	PAR indicates even parity. The AMD-751 System Controller drives PAR as a PCI initiator one clock after the address phase and each data write phase to generate even parity across AD[31:0] and C/BE[3:0]#. The AMD-751 drives PAR as a PCI target one clock after each data read phase. The AMD-751 does not support parity checking.
PHLDAJ	**Grant signal to the M1535D PCI-ISA Bridge for PCI bus master.**
INTAJ_MI	Interrupt signal.
INTBJS0	**Interrupt signal.**
INTCJS1	Interrupt signal.
INTDJS2	**Interrupt signal.**
PCI_PME_N	Power management interrupt signal.

A.4 IDE

Table A-4 IDE Signals

Signal	Description
RSTDRV	**IDE reset.**
HDDP[15:0]	Primary HDD date.
HDDRQP_N	**Primary HDD DMA request.**
HDIOWP_N	Primary HDD I/O write.
HDIORP_N	**Primary HDD I/O read.**
HDCHRDYP_N	Primary HDD ready.
HDDACKP_N	**Primary HDD DMA acknowledge.**
HDCS3P_N	IDE chip select 3 for primary HDD.

Table A-4 IDE Signals (Continued)

Signal	Description
HDAP[2:0]	**Primary IDE ATA address bus.**
HDACT_N	HDD activity led signal.
HDDS[15:0]	**Secondary HDD data.**
HDDRQS_N	Secondary HDD DMA request.
HDIOWS_N	**Secondary HDD I/O write.**
HDIORS_N	Secondary HDD I/O read.
HDCHRDYS_N	**Secondary HDD ready.**
HDDACKS_N	Secondary HDD DMA acknowledge.
HDCS3S_N	**IDE chip select 3 for secondary HDD.**
HDAS[2:0]	Secondary ATA address bus.

A.5 Floppy Disk Drive

Table A-5 FDD Signals

Signal	Description
DRVDEN(densel)	**Indicates whether a low (250/300 Kb/s) or high (500/1000 Kb/s) data rate has been selected.**
INDEX_N(index_n)	This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
MTR0_N(mot0_n)	**These active-low outputs select motor drives 0-1.**
DS1_N(drv1_n)	An additional Drive Select signals in PPM mode. Drive Select signal 0 and 1 are multiplexed with STROBJ and ACKJ.
DS0_N(drv0_n)	**Active low output select drives 0-1.**
MTR1_N(mot1_n)	Additional Motor On signals in PPM mode. Motor On 0 and 1 are multiplexed with PD[6] and BUSY.
DIR_N(dir_n)	**This active low output determines the direction of the head movement (low =step-in, high = step-out).**
STEP_N(step_n)	This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.
WDATA_N(wdata)	**This active low output is a write— precompensated serial detonate the selected disk drive. Each falling edge causes a flux change on the media to be written.**

Table A-5 FDD Signals (Continued)

Signal	Description
WGATE_N(wgate)	This active-low, high-drive output enables the write circuitry of the selected disk drive.
TR0_N(trk0_n)	**This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.**
WPROT_N(wprot_n)	This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write protected.
RDATA_N(rdata_n)	**The active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.**
HDSEL_N(hdsel_n)	This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
DSKCHG_N(dshchg_n)	**This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of location base+7.**

A.6 Front Panel

Table A-6 Front Panel Signals

Signal	Description
PWR	**Signal for multifunctional front button Power on/Sleep.**
SPKR	Speaker signal.
RST	**Reset signal (Optional).**
HDDACT	Hard disk activity indicator LED (Optional).
SPLED	**Power Indicator LED.**
KBINH	Keyboard lock.

Appendix B

Support,

Products and

Documentation

B.1 Customer Support

Alpha Processor, Inc. provides assistance for their products on their web page at `www.alpha-processor.com`.

Alpha Original Equipment Manufacturers (OEMs) provide the following web page resources for customer support:

URL	Description
`http://www.compaq.com`	**Contains links for the Alpha 21264A Processor.**
`http://www.amd.com`	Contains links for the AMD-751 System Controller.
`http://www.acerlabs.com`	**Contains links for the M1535D PCI-ISA Bridge.**
`http://www.intel.com`	Contains links for the 21143 LAN (Ethernet) controller

B.2 Supporting Products

Alpha Processor, Inc. maintains a Hardware Compatibility List on their web site for components and accessories that are not included with the UP1100. Compatibility for items such as memory, power supplies, and enclosure are listed.

Point your browser to `www.alpha-processor.com` and check the Product Information list for Peripherals.

B.3 Alpha Products

Alpha Processor, Inc. maintains information about other Alpha products on their web site. Point your browser to `www.alpha-processor.com` and check the Product Information list for Alpha products.

B.4 Documentation

B.4.1 Alpha Documentation

Title	Vendor
Alpha Architecture Reference Manual	**Digital Press order# EQ-W938E-DP.**
Alpha Architecture Handbook	Compaq Computer Corporation order# EC-QD2KC-TE, October, 1998.
Alpha 21264 Microprocessor Hardware Specification	**Digital Press**
UP1100 Quick Start Installation Guide (51-0047)	Alpha Processor, Inc.
UP1100 User Manual (51-0048)	**Alpha Processor, Inc.**

B.4.2 Related Documentation

You can order the following associated documentation directly from the vendor.

Title	Vendor
21143 PCI/CardBus 10/100 Mb/s Ethernet LAN Controller Datasheet	**Intel Corporation 2200 Mission College Blvd. Santa Clara, CA 95052-8119**
A*ccelerated Graphics Port Interface Specification* Revision 2.0	Intel Corporation 2200 Mission College Blvd. Santa Clara, CA 95052-8119 May, 1998
AlphaPC 264DP Technical Reference Manual	**Compaq Computer Corporation order# EC-RBODA-TE.**
AMD-751TM System Controller Data Sheet, Revision E	AMD Publication # 21910, March, 2000
Computer Architecture	**John L. Hennessy and David A. Patterson, Morgan Kaufman Publishers, San Mateo, CA, 1990.**

Title	Vendor
*EPM7064 Programmable Logic Device Family Data Shee*t	Altera Corporation, 101 Innovation Drive San Jose, CA 95134
ISA & EISA Theory and Operations	**Edward Solari, Annabooks Bookstore (http://www.annabooks.com/index.htm), ISBN 0-929392-15-9**
M1535D: PCI-to-ISA Bus Bridge with Super I/O & Fast IR Data Sheet, Ver. 1.20	ALI
• ***PCI Local Bus Specification, Revision 2.1*** • ***PCI Multimedia Design Guide, Revision 1.0*** • ***PCI System Design Guide*** • ***PCI-to-PCI Bridge Architecture Specification, Revision 0***	**PCI Special Interest Group** **U.S. 1-800-433-5177** **International1-503-797-4207** **FAX 1-503-234-6762**
• *PC SDRAM Specification, Revision 1.63* (October, 1998) • *PC SDRAM Unbuffered DIMM Specification, Revision 1.0* (February, 1998) • *PC SDRAM Serial Presence Detect (SPD) Specification, Revision 1.2A* (December, 1997)	Intel Corporation
The Indispensable PC Hardware Book 3E	**Hans-Peter Messamer, Addison-Wesley Pub. Co., ISBN 0-201-87697-3**
Universal Serial Bus Specification, Revision 1.1	USB Implementers Forum `http://www.usb.org/developers/docs.html` September, 1998

Index

Numerics

A

C

D

E

F

H

I

K

M

P

R

S

T

U

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