# UP1000
# Technical Reference Manual

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***Alpha Processor, Inc.***
A Samsung Company
130C Baker Avenue Extension
Concord, MA 01742
Tel: 978.318.1100
Fax: 978.371.3177

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# Revision History

| Date | Rev | Description |
|---|---|---|
| **08/27/99** | **51-0034-0A** | **UP1000 Technical Reference Manual initial release for the UP1000 Motherboard part number 40-0004-C.** |
| 10/06/99 | 51-0034-0B | Edited for Beta version of UP1000. |
| **10/21/99** | **51-0034-0C** | **Second edit for Beta version of UP1000.** |
| 12/23/99 | 51-0034-1A | First product release. This manual describes the Alpha Processor, Inc. parts numbered 90-0001-2C (beta test boards) and 90-0001-3A (first product release boards). |

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# Preface

## Overview

This manual describes the Alpha Processor, Inc. UP1000 product, including the UP1000 Motherboard used with the Alpha Slot B Module and the AMD-751 System Controller and the ALI M1543C PCI-ISA Bridge.

## Audience

This manual is intended for system designers and others who use the UP1000 to design or evaluate computer systems based on the Alpha Slot B Module and the AMD-751 System Controller and M1543C PCI-ISA Bridge controller chips.

## Scope

This manual describes the features, configuration, functional operation, and interfaces of the UP1000. This manual does not include specific details on industry standards (for example, on PCI or ISA bus specifications). Additional information is available in the appropriate vendor and IEEE specifications. See Appendix B for information on how to order related documentation and obtain additional technical support.

## Manual Organization

The UP1000 Technical Reference Manual is organized as follows:

- Chapter 1, “UP1000 Introduction,” lists the features of the UP1000. A functional block diagram of the UP1000 is included.
- Chapter 2, “System Configuration,” describes the UP1000 configuration options, including switch functions and settings. A board layout is provided, which identifies connector locations.
- In Chapter 3, “Electrical, Environmental and Physical Data,” a description is provided of the electrical and environmental requirements and physical board dimensions for the UP1000.
- A functional description of the UP1000 is provided in Chapter 4, “Functional Description.” This includes a description of the functional subsystems and firmware designs for the UP1000.

- Chapter 5, “System Memory and Address Mapping,” provides a description of the memory subsystem and address mapping for the UP1000.
- Pinouts for the Alpha Slot B Connector and all power connectors used in the UP1000 are provided in Appendix A, “Connectors, Pinouts, and Signals.” This appendix also contains a list of all other connectors used in the UP1000, which are industry standard parts, and a description of all signals, organized by function.
- Appendix B, “Support, Products and Documentation,” describes how to obtain technical information and support for the UP1000, and where to order parts and accessories for the UP1000. It includes information on how to obtain Alpha Processor, Inc. products and supporting literature.

# Conventions and Definitions

This section defines product-specific terminology, abbreviations, and other conventions used throughout this manual.

## Signals and Bits

- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by Alpha Processor, Inc. for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes to these registers, it must first read the register and change only the non-reserved bits before writing back to the register.

## Data

The following list defines data terminology:

- Units
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.

- Abbreviations—The following notation is used for bits and bytes:
  - Kilo—K, as in 4-Kbyte page ($2^{10}$)
  - Mega—M, as in 4 Mbits / sec ($2^{20}$)
  - Giga—G, as in 4 Gbytes of memory space ($2^{30}$)

## Acronyms

The following is a list of the acronyms used in this document and their definitions.

| Abbreviation | Meaning |
|---|---|
| **ADE** | **Alpha Diagnostic Environment** |
| AGP | Advanced Graphics Port |
| **ALI** | **Acer Laboratories, Inc.** |
| AMD | Advanced Micro Devices, Inc. |
| **APIC** | **Advanced Programmable Interrupt Controller** |
| BIOS | Basic Input / Output System |
| **CE** | **European Conforming** |
| CD | Compact Disk |
| **COM** | **Communications** |
| CPU | Central Processing Unit |
| **cUL** | **Canadian Underwriters Laboratory** |
| DDR | Double Data Rate |
| **DIMM** | **Dual Inline Memory Module** |
| DIP | Dual Inline package |
| **DQM** | **Data Input/Output Mask** |
| ECC | Error-correcting Code |
| **EEPROM** | **Electrically Erasable Programmable Read-only Memory** |
| EMI | Electromagnetic Interference |
| **EPLD** | **Electrically Programmable Logic Device** |
| FCC | Federal Communications Commission |
| **FDD** | **Floppy Disk Drive** |
| GART | Graphics Address Relocation Table |
| **HDD** | **Hard Disk Drive** |
| HSTL | High Speed Transceiver Logic |
| **I2C** | **Inter-integrated Circuit** |

| Abbreviation | Meaning |
|---|---|
| ICS | Integrated Circuit Systems |
| **ID** | **Identification** |
| IDE | Integrated Device Electronics |
| **I/O** | **Input/Output** |
| IRQ | Interrupt Request |
| **ISA** | **Industry Standard Architecture** |
| JEDEC | Joint Electron Device Engineering Council |
| **KBD** | **Keyboard** |
| LED | Light Emitting Diode |
| **MB** | **Motherboard** |
| MUX | Multiplexer |
| **NDA** | **Non-disclosure Agreement** |
| NMI | Non-maskable Interrupt |
| **NVRAM** | **Nonvolatile Random Access Memory** |
| OEM | Original Equipment Manufacturer |
| **OS** | **Operating System** |
| PA | Physical Address |
| **PAL** | **Privileged Architecture Library** |
| PCB | Printed Circuit Board |
| **PCI** | **Peripheral Component Interconnect** |
| PME | Power Management |
| **RAM** | **Random Access Memory** |
| ROM | Read-only Memory |
| **RTC** | **Real-time Clock** |
| SDRAM | Synchronous Direct Random Access Memory |
| **SM** | **System Management** |
| SPD | Serial Presence Detect |
| **SROM** | **Serial Read-only Memory** |
| SSRAM | Synchronous SRAM |
| **UART** | **Universal Asynchronous Receiver/Transmitter** |
| UL | Underwriters Laboratory |
| **USB** | **Universal Serial Bus** |
| VRM | Voltage Regulator Module |

# Chapter 1 UP1000 Introduction

This chapter provides an overview of the UP1000 product, including its components and features.

The UP1000 product consists of a UP1000 Motherboard which supports an Alpha Slot B Module and a Peripheral Component Interconnect (PCI) bus through the Advanced Micro Devices, Inc. (AMD) AMD-751 System Controller and the Acer Laboratories, Inc. (ALI) M1543C PCI-ISA Bridge, respectively. UP1000s are designed for use in uniprocessor workstation and low-end server platforms.

The Alpha Slot B Module contains one 21264 central processing unit (CPU), L2 cache and a Voltage Regulator Module (VRM).

## 1.1 Features

Table 1-1 provides a summary of the UP1000 product features.

**Table 1-1 UP1000 Product Features**

| Feature | Description | Manufacturer |
|---|---|---|
| **Physical Form Factor:** | **ATX (12" X 9.6")** | |
| Daughter Card Interface: | • One 600 MHz Alpha Slot B Module | Alpha Processor, Inc. |
| | • **External 2 or 4 MB Bcache, 128-bit Late Write Synchronous Static Random Access Memory (SSRAMs)** | |
| **Chipsets:** | • AMD-751 System Controller System Controller | AMD |
| | • **M1543C PCI-ISA Bridge** | **ALI** |
| Main Memory: | Three 168-pin, PC 100 Synchronous Direct Random Access Memory (SDRAM) unbuffered Serial Presence Detect (SPD) Dual Inline Memory Modules (DIMMs) of 64 MB, 128 MB, or 256 MB, providing 64 MB to 768 MB memory with Error-correcting Code (ECC) | |
| **Power Supply:** | • **Requires 400W ATX Power Supply** | |
| | • Uses ATX power connectors | |
| System Interface: | • **100 MHz clock with Double Data Rate (DDR) transfers** | |

**Table 1-1 UP1000 Product Features (Continued)**

| Feature | Description | Manufacturer |
|---|---|---|
| **On-board Input/Output (I/O):** | • Two Ultra DMA33 Integrated Device Electronics (IDE) connectors, driven by the dual-channel IDE controllers in the M1543C PCI-ISA Bridge | |
| | • **Inter-integrated Circuit (I2C) System Management (SM) bus** | |
| | • Two external Universal Serial Bus (USB) ports, driven by the USB controller in the M1543C PCI-ISA Bridge | |
| | • **Two serial Universal Asynchronous Receiver Transmitter (UART) ports, driven by the Super I/O controller in the M1543C PCI-ISA Bridge** | |
| | • One Enhanced Capabilities Port (ECP) / Enhanced Parallel Port (EPP) / SP parallel port, driven by the Super I/O controller in the M1543C PCI-ISA Bridge | |
| | • **One dual-drive capable Floppy Disk Drive (FDD) controller driven by the Super I/O controller in the M1543C PCI-ISA Bridge** | |
| | • PS/2 Keyboard and Mouse port | |
| I/O Slots: | • **One 2x Accelerated Graphics Port (AGP) slot, driven by the AGP controller in the AMD-751 System Controller** | |
| | • Four 33 MHz PCI slots, driven by the 32-bit PCI bus controller in the AMD-751 System Controller | |
| | • **Two Industry Standard Architecture (ISA) slots, driven by the M1543C PCI-ISA Bridge** | |
| **Operating System (OS):** | Linux | |

# 1.2 System Components

The UP1000 is implemented in industry-standard parts and uses Alpha Slot B Module. The functional components of the UP1000 are shown in block diagram form in Figure 1-1. A detailed description of system components is provided in Chapter 4, “Functional Description”.

***Note:*** *Refer to the list of Acronyms on page xii of the Preface for an explanation of terminology used in the block diagram.*

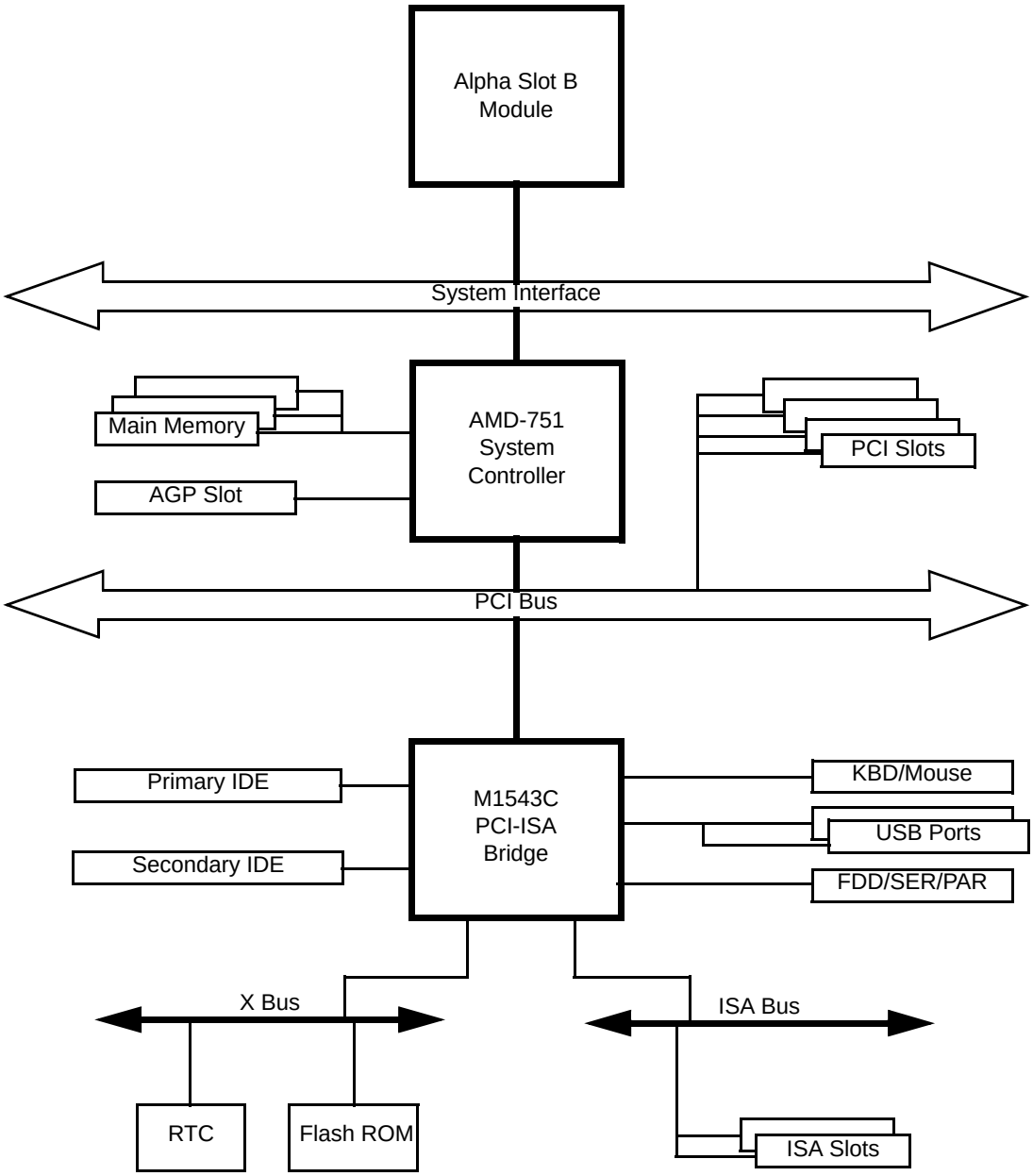



**Figure 1-1 UP1000 Functional Block Diagram**

# Chapter 2 System Configuration

This chapter describes the layout and configuration of the UP1000 Motherboard and the Alpha Slot B Module.

Jumpers and switch settings determine the UP1000 configuration. Some of these configuration settings are variable, as described in section 2.2, "Variable Configuration Settings." Other configuration settings are fixed; that is, the UP1000 only works with these configuration settings in the default positions as described in section 2.3, "Fixed Configuration Settings."

## 2.1 Board Layouts and Components

On-board connectors are provided for the following:

- Alpha Slot B Module
- AGP, PCI and ISA cards
- IDE and FDD devices
- USB devices
- Memory DIMMs
- Serial and parallel peripherals
- Power

These connectors and the configuration switches are shown in Figure 2-1, which depicts the UP1000 Motherboard and its components. Table 2-1 specifies the components as indicated in Figure 2-1.

Refer to Appendix A for a complete description of the connectors and pinouts used in the UP1000.

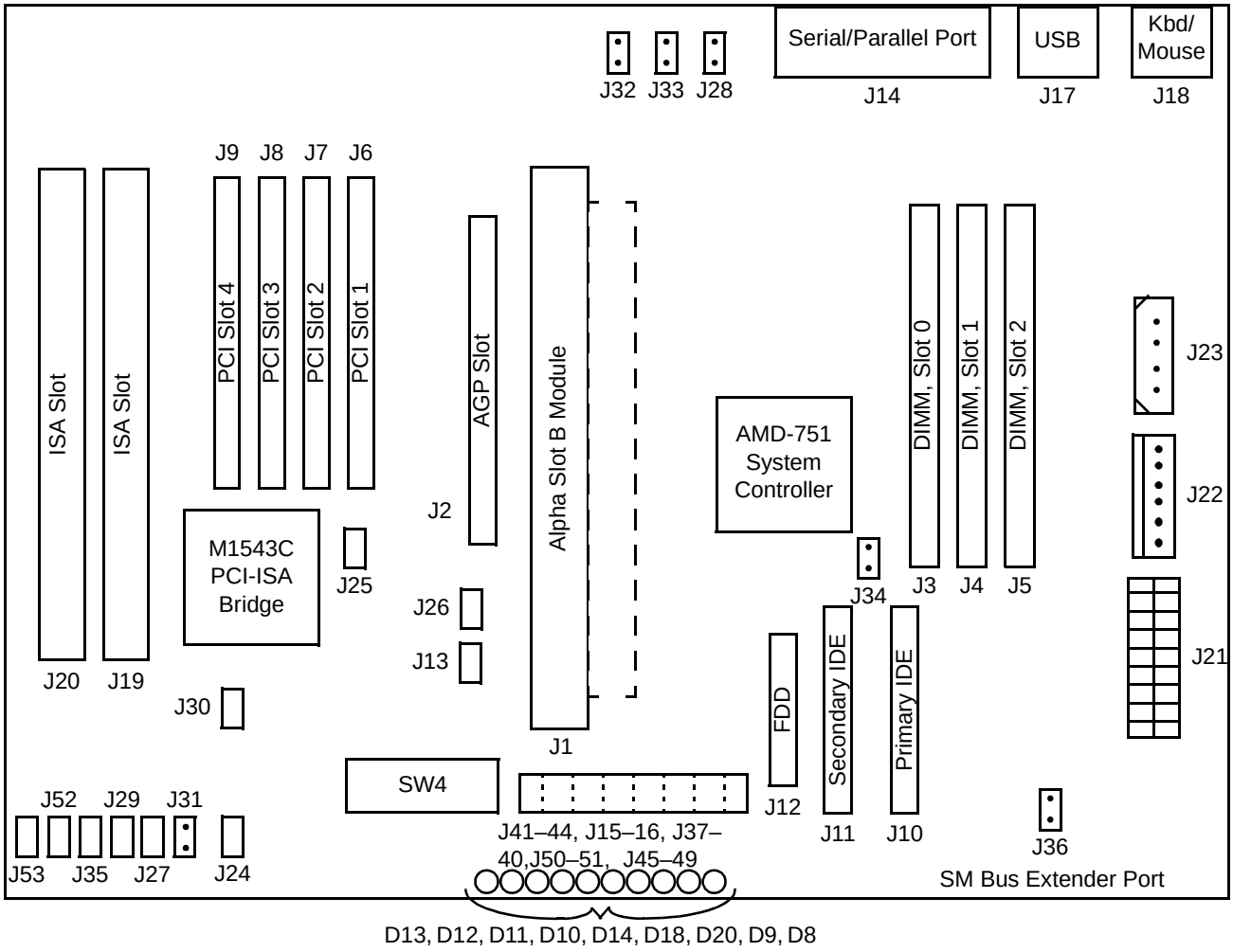



**Figure 2-1 UP1000 Motherboard Layout**

**Table 2-1 UP1000 Motherboard Jumper and Connector Component List**

| Comp. No. | Specification | Comp. No. | Specification |
|---|---|---|---|
| **J1** | **Alpha Slot B Connector** | **J2** | **AGP Connector** |
| J3 | 168-pin DIMM Socket, Slot 0 | J4 | 168-pin DIMM Socket, Slot 1 |
| **J5** | **168-pin DIMM Socket, Slot 2** | **J6** | **32-bit PCI Connector, Slot 1** |
| J7 | 32-bit PCI Connector, Slot 2 | J8 | 32-bit PCI Connector, Slot 3 |
| **J9** | **32-bit PCI Connector, Slot 4** | **J10** | **Primary IDE Connector** |
| J11 | Secondary IDE Connector | J12 | FDD Connector |

***Notes: * Pin orientation is important. Refer to the UP1000 User's Guide (51-0031-0A) for details.***
***** J28 is only present on the 90-0001-2C board.***

**Table 2-1 UP1000 Motherboard Jumper and Connector Component List (Continued)**

| Comp. No. | Specification | Comp. No. | Specification |
|---|---|---|---|
| **J13** | **Electrically Programmable Logic Device (EPLD) Program Port** | **J14** | **Serial/Parallel I/O Port** |
| J15 | Option Switch SW3 | J16 | Option Switch SW4 |
| **J17** | **USB Port** | **J18** | **Keyboard/Mouse Port** |
| J19 | ISA Connector | J20 | ISA Connector |
| **J21** | **ATX Power Connector** | **J22** | **Auxiliary ATX Power Connector** |
| J23 | System Power Connector | J24 | Reset Switch Cable Connector |
| **J25** | **Debug Port Connector** | **J26** | **System Voltage Monitor Chip Configuration Jumper (Not Used)** |
| J27 | Power Switch Cable Connector | J28 | Optional Fan Connector*, ** |
| **J29** | **Power Light Emitting Diode (LED) Connector*** | **J30** | **Speaker Cable Connector** |
| J31 | Chassis Fan Connector* | J32 | Alpha Slot B Module Fan Cable Connector* |
| **J33** | **Alpha Slot B Module Fan Cable Connector*** | **J34** | **Hard Disk Drive (HDD) Activity LED Connector*** |
| J35 | Keyboard Lock Cable Connector | J36 | SM Bus Extender Port |
| **J37** | **Option Switch SW5** | **J38** | **Serial Read-only Memory (SROM) Format Selection Jumper** |
| J39 | Bcache Enable / disable Jumper | J40 | Fail Safe Block Selection Jumper |
| **J41** | **Motherboard (MB) Bus Speed Selection Jumper** | **J42** | **Option Switch SW0** |
| J43 | Option Switch SW1 | J44 | Option Switch SW2 |
| **J45** | **Fixed Configuration Jumper** | **J46** | **Configuration Jumper (Not Used)** |
| J47 | Configuration Jumper (Not Used) | J48 | Configuration Jumper (Not Used) |
| **J49** | **Configuration Jumper (Not Used)** | **J50** | **Fixed Configuration Jumper** |
| J51 | Fixed Configuration Jumper | J52 | Flash Read-only memory (ROM) U31 Safety Block Update Jumper |
| **J53** | **Flash ROM U32 Safety Block Update Jumper** | **SW4** | **System Clock Generator Configuration Switch** |

***Notes: * Pin orientation is important. Refer to the UP1000 User's Guide (51-0031-0A) for details.***
***** J28 is only present on the 90-0001-2C board.***

***Note:*** *Alpha Processor, Inc. recommends the use of high-quality, shielded cables for all I/O.*

Figure 2-2 shows the Alpha Slot B Module located on the UP1000 Motherboard.

**Figure 2-2 Alpha Slot B Module**

# 2.2 Variable Configuration Settings

The UP1000 Motherboard has ten configuration jumpers which have selectable settings. These jumpers are all firmware-related, and are organized as follows:

- J15, J16, J37, J42–J44 (Option switches SW3–SW5 and SW0–SW2, respectively)—Diagnostics and flash recovery
- J39, J40—Alternate firmware selection
- J52, J53—Flash ROM safe block update

Locations of all configuration switches except J52 and J53 are shown in Figure 2-3. J52 and J53 are shown in Figure 2-1, and are located on the front left corner of the UP1000 Motherboard, below the ISA slots.

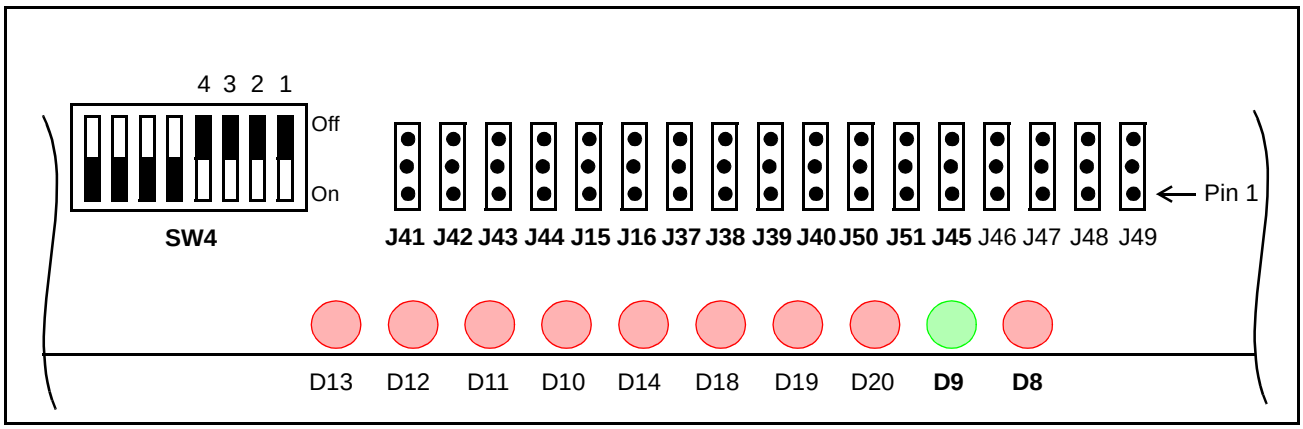



**Figure 2-3 LED Locations**

## 2.2.1 Diagnostics and Flash Recovery

Configuration of diagnostics and flash recovery is managed through setting of the jumpers J15 (SW3), J16 (SW4), J37 (SW5), J42 (SW0), J43 (SW1), and J44 (SW2). Table 2-2 shows the three possible configuration settings for these six jumpers. The default function is Boot to AlphaBIOS, with a shunt installed on pins 2 and 3 (0 position) of all six jumpers.

**Table 2-2 Diagnostics and Flash Recovery Configuration Settings (J15, J16, J37, J42–J44)**

| Function | J42 | J43 | J44 | J15 | J16 | J37 |
|---|---|---|---|---|---|---|
| **Boot to AlphaBIOS (using console)—Default** | **0** | **0** | **0** | **0** | **0** | **0** |
| Restore Factory Defaults (using console) | 1 | 0 | 0 | 0 | 0 | 0 |
| **Recover AlphaBIOS (using console)** | **0** | **1** | **0** | **0** | **0** | **0** |
| Reflash ADE (using console) | 1 | 1 | 0 | 0 | 0 | 0 |
| **Interactive ADE (using console)** | **0** | **0** | **1** | **0** | **0** | **0** |
| Interactive ADE (using J25, Debug Port) | 0 | 0 | 1 | 1 | 0 | 0 |
| **Interactive Reset PAL (using J25, Debug Port)** | **0** | **0** | **0** | **0** | **0** | **1** |

***Notes:*** ***1. Pin 1 is closest to the board edge, pin 3 is closest to the Alpha Slot B Modules.***
***0 = Shunt installed on pins 2 and 3.***
***1 = Shunt installed on pins 1 and 2.***
*2. The Debug Port (J25) defaults to 9600 baud. When using the Interactive Reset PAL function, type an uppercase* **U** *to set the interactive baud rate higher.*
*3. Refer to section 4.9.2 on page 4-14 for information on Reset PAL.*
*4. Refer to section 4.9.3 on page 4-15 for information on ADE.*

## 2.2.2 Alternate Firmware

Configuration of alternate firmware is managed through setting of the following jumpers:

- J39—Bcache enable / disable
- J40—Fail safe block selection

Jumper J39 actually forces the processor speed to 500 MHz when a shunt is installed on pins 2 and 3. In this configuration, there are two outcomes as follows, depending on the configuration of J40:

- If a shunt is installed on J40, pins 1 and 2, use 1 MB Bcache configuration (default firmware)
- If a shunt is installed on J40, pins 2 and 3, use no Bcache and disable ECC on the memory system (back-up firmware)

Table 2-3 shows the alternate firmware configuration settings. A shunt

installed on pins 1 and 2 is the default setting for both J39 and J40.

**Table 2-3 Alternate Firmware Configuration Settings (J39, J40)**

| Jumper | Shunt Installed on Pins 1 and 2 (Default) | Shunt Installed on Pins 2 and 3 |
|---|---|---|
| **J39** | **Bcache enabled** | **Bcache disabled** |
| J40 | Normal | Fail safe block selected |

*Note: Pin 1 is closest to the board edge, pin 3 is closest to the Alpha Slot B Modules.*

### 2.2.3 Flash ROM Safety Block Update

During normal operation, the safe block of the Flash ROM cannot be updated. To update the safe block of Flash ROM U31 or U32, a dedicated shunt must be installed in the update position at J52 and J53 (respectively), as described in Table 2-4.

By default, no jumper is installed on Flash ROM update jumpers J52 or J53. This is the normal operating mode.

**Table 2-4 Flash ROM Update Configuration Settings (J52, J53)**

| Jumper | Configuration |
|---|---|
| **J52** | **Install shunt to update Flash ROM safe block in U31** |
| J53 | Install shunt to update Flash ROM safe block in U32. |

## 2.3 Fixed Configuration Settings

The UP1000 Motherboard has six configuration switches which must remain in the default settings. These switches are organized as follows:

- J38—SROM format selection
- J41—MB bus speed selection
- J45, J50, J51—Hardware clocking selection
- SW4—System bus clock speed

Locations of these configuration switches are shown in Figure 2-3.

***Note:*** *The default settings for these fixed configuration switches must not be changed. The UP1000 may not operate correctly if these default settings are changed.*

## 2.3.1 UP1000 Motherboard

Configuration of the UP1000 Motherboard is managed through setting of the following jumpers:

- J41—MB bus speed selection
- J38—SROM format selection

Table 2-5 shows the configuration default settings.

**Table 2-5 UP1000 Motherboard Configuration Settings (J38, J41)**

| Jumper | Configuration |
|---|---|
| **J41** | **100 MHz—Shunt installed on pins 1 and 2.** |
| J38 | Option Block—Shunt installed on pins 2 and 3. |

*Note: Pin 1 is closest to the board edge, pin 3 is closest to the Alpha Slot B Modules.*

## 2.3.2 Hardware Clocking Settings

Jumpers J45, J50 and J51 configure selection of hardware clocking settings. These switches must be left in the default positions as shown in Table 2-6.

**Table 2-6 Hardware Clocking Selection Configuration Settings (J45, J50, J51)**

| Jumper | Configuration |
|---|---|
| **J50** | **Shunt installed on pins 1 and 2.** |
| J51 | Shunt installed on pins 2 and 3. |
| **J45** | **Shunt installed on pins 1 and 2.** |

*Note: Pin 1 is closest to the board edge, pin 3 is closest to the Alpha Slot B Modules.*

## 2.3.3 System Bus Clock

Clock speed is configured on the UP1000 Motherboard by the system clock generator configuration switch, SW4. Only a 100 MHz system bus speed (that is, CPU / SDRAM clock speeds) configuration is supported. 100 MHz is the default setting, as seen in Table 2-7.

***Note:*** *Pins 5 through 8 of SW4 are not used.*

**Table 2-7 System Clock Configuration Settings (SW4)**

| SW4 Settings | | | | Clock Configurations | | | |
|---|---|---|---|---|---|---|---|
| **Pin 1** | **Pin 2** | **Pin 3** | **Pin 4** | **CPU/SDRAM** | **PCI** | **AGP** | **USB** |
| **Off** | **Off** | **Off** | **Off** | **100 MHz** | **33.3 MHz** | **66.6 MHz** | **48 MHz** |

# Chapter 3 Electrical, Environmental and Physical Data

In this chapter, a description is provided of the UP1000 power requirements, environmental and enclosure specifications, and physical parameters.

## 3.1 Power Specifications

### 3.1.1 Power Consumption

The UP1000 Motherboard has a maximum total power consumption of 37W, excluding any disk drives. The Alpha Slot B Module has a maximum total power consumption of 166W.

Table 3-1 lists the current requirement for each direct current supply voltage (Vdc) for the UP1000 Motherboard. Table 3-2 lists the current requirement for each direct current supply voltage (Vdc) for the Alpha Slot B Module. All requirements are for fully populated products, with maximum usage applied.

***Note:*** *These tables do not include requirements for SDRAM, peripheral slots or disk drives. Be sure to allow for adequate additional current when selecting a power supply for the UP1000.*

**Table 3-1 Estimated Maximum Power Consumption– UP1000 Motherboard**

| $V_{DD}$ Source | Current | Power | Remarks |
|---|---|---|---|
| **3.3V** | **7.0A** | **23.1W** | |
| 5V | 2.0A | 10.0W | |
| **5V standby** | **0.8A** | | **Excluded in total power** |
| -5V | 0.05A | 0.25W | |
| **12V** | **0.2A** | **2.4W** | |
| -12V | 0.1A | 1.2W | Fans |
| **Total Power Consumption:** | | **37.0W** | |

*Note: Current rates are a combination of measured and calculated values.*

**Table 3-2 Estimated Power Consumption–Primary Alpha Slot B Module, 8 MB Bcache**

| $V_{DD}$ Source | Current | Power | Remarks |
|---|---|---|---|
| **3.3V** | **6.3A** | **20.8W** | |
| 5V | 0.2A | 1.0W | |
| **12V** | **12A** | **144W** | **VRM** |
| **Total Power Consumption:** | | **165.8W** | |

### 3.1.2 Power Supply

The UP1000 requires the use of a 400W ATX power supply, with at least 14A at the +12V rail.

### 3.1.3 Power Connectors

The power connectors on the UP1000 Motherboard consist of the following:

- ATX Standard: One 10 x 2 (20-pin)
- AUX ATX*: One 6 x 1 (6-pin)
- Alpha Slot B Module Power Supply: One 4 x 1 (4-pin)

12V is input to the L7571C VRM, which outputs the core voltage to the CPU. Because over 9A is required by the Alpha Slot B Module, one Alpha Slot B Module Power Supply 4 x 1 (4-pin) connector is added. To support 3.3V, the AUX ATX 6 x 1 (6-pin) connector can be used.

***Note:*** **Use the AUX ATX 6-pin connector when an additional 6-pin connection is included with the ATX Standard power connector.*

## 3.2 Environmental Specifications

The Alpha Slot B Module microprocessor is cooled by two small fans drawing air directly from the chip's heat sink. The UP1000 is designed to run efficiently using only these fan. Additional fans may be necessary depending upon cabinetry and requirements of plug-in cards.

The UP1000 Motherboard and Alpha Slot B Module are specified to run within the environment listed in Table 3-3.

**Table 3-3 Environmental Requirements**

| Parameter | Specification |
|---|---|
| **Operating temperature** | **+5 to +35° C (+41 to +95° F)** |
| Storage temperature | -35 to +85° C (-31 to +185° F) |
| **Relative Humidity** | **10% to 90%, with maximum wet bulb temperature of 35° C (95° F) and minimum dew point of 2° C (36° F)** |
| Rate of (dry bulb) temperature change | 11° C / hr. ±2° C / hr. (20° F / hr. ±4° F / hr.) |

## 3.2.1 Safety

The UP1000 Motherboard meets registered product-safety certification for the U.S. and Canadian Underwriters Laboratories (UL and cUL). It also meets the European Conforming (CE) standard EN 60950:1992 "Safety of Information Technology Equipment Including Electrical Business Equipment Incorporating Amendment Nos 1, 2, 3, 4." European Norm (EN) standards which conform to the relevant directives are published in the Official Journal of the European Community.

## 3.2.2 EMI

The UP1000 Motherboard meets electro-magnetic interference (EMI) emission certification for the following:

- EN 55022:1994 / A1:1958 / A2:1997 Class A ITE emissions requirements
- Federal Communications Commission (FCC) 47 CFR Part 15 Class A

It also meets the EMI immunity certification EN 50082-1:1992 "EMC Residential, Commercial and Light Industrial Generic Immunity Standard."

***Note:*** *Alpha Processor, Inc. recommends the use of high-quality, shielded cables for all I/O.*

## 3.2.3 Thermal

Figure 3-1 shows the location of thermally-sensitive components on the UP1000 Motherboard. A list of maximum allowable case temperatures for these components is provided in Table 3-4.

Case temperatures are a vital factor in determining airflow on a

motherboard. Variables which may affect a component's case temperature include the following:

- Operating temperature
- Operating frequency
- Current load

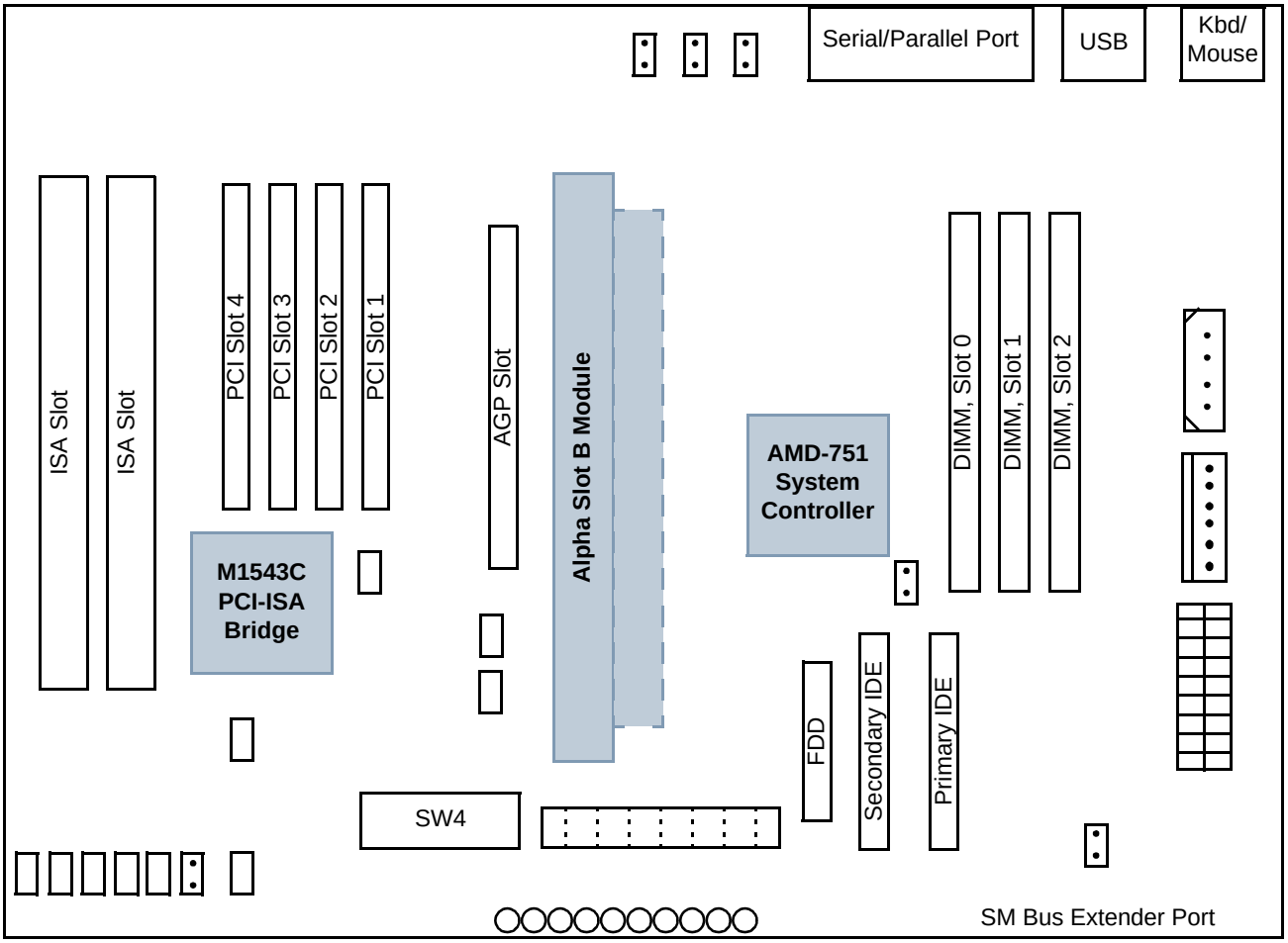



**Figure 3-1 Thermally-sensitive Components**

**Table 3-4 Maximum Component Case Temperatures**

| Component | Maximum Temperature |
|---|---|
| **Alpha Slot B Module** | **<70°C (158°F)** |
| AMD-751 System Controller | <70°C (158°F) |
| **M1543C PCI-ISA Bridge** | **TBD° (No heat sink)** |

A thermal test conducted by Alpha Processor, Inc. determined that these components remained within maximum specified temperatures. The test system configuration comprised the minimum configuration to boot the system OS, running in a 35°C chamber.

## 3.3 Enclosure Requirements

This product has been approved for use in the Axxion Group ATX Case, DL-17.

## 3.4 Physical Parameters

### 3.4.1 UP1000 Motherboard Parameters

The UP1000 Motherboard is a printed circuit board (PCB) with the dimensions specified in Table 3-5.

**Table 3-5 UP1000 Motherboard Physical Parameters**

| Dimension | Value |
|---|---|
| **Length** | **304.8 mm (12 in)** |
| Width | 243.8 mm (9.6 in) |
| **Height** | **132.1 mm (5.2 in)** |

### 3.4.2 Alpha Slot B Module Parameters

The Alpha Slot B Module is a PCB assembly with the dimensions specified in Table 3-6.

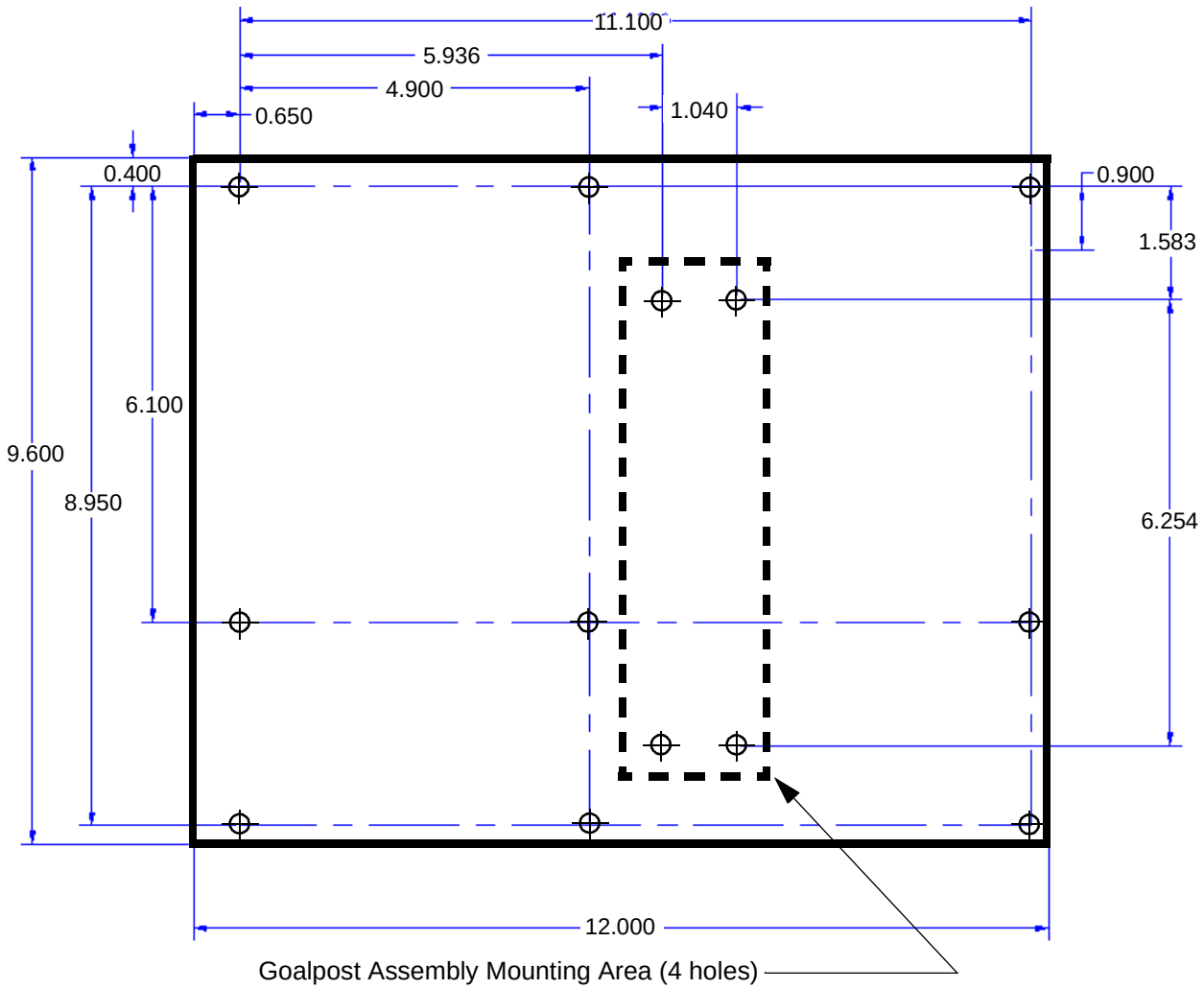
**Table 3-6 Alpha Slot B Module Physical Parameters**

| Dimension | Value |
|---|---|
| **Length** | **168.8 mm (6.6 in)** |
| Width | 47.8 mm (1.9 in) |
| **Height** | **114.3 mm (4.5 in)** |
| **Weight** | **1.2 kg (2.6 lb)** |

## 3.4.3 UP1000 Motherboard Mounting Hole Specification

The UP1000 Motherboard mounting hole specification is depicted in Figure 3-2.

***Note:*** *The Alpha Slot B Module goalpost assembly must be correctly installed on the UP1000 Motherboard and in the chassis enclosure. Incorrect installation or use of the goalpost assembly can result in severe distortion of the UP1000 Motherboard, and may void your warranty. Refer to the* ***UP1000 Quick Start Installation Guide*** *(Alpha Processor, Inc. part number 51-0035-0A) for complete mechanical installation details.*




*Note: All dimensions are in inches.*

**Figure 3-2 UP1000 Motherboard Mounting Hole Specification**

# Chapter 4 Functional Description

This chapter describes the functional operation of the UP1000. It introduces the AMD-751 System Controller, and briefly describes its implementation with the M1543C PCI-ISA Bridge peripheral controller.

In this chapter, descriptions are also provided of the UP1000 subsystem structure, and the logic and firmware used.

## 4.1 AMD-751 System Controller

AMD's System Controller is the intersection of four buses on the UP1000. These buses are as follows:

- System interface
- PC-100 SDRAM
- PCI
- AGP

The System Controller is responsible for receiving data, addresses, commands, and control signals from one bus domain and translating them into other bus domains. The following sections cover each of the System Controller's bus interfaces, and describe how it translates signals between bus domains.

### 4.1.1 System Interface

A system interface connects the Alpha Slot B Module and the AMD-751 System Controller. The system interface contains the following signal groupings:

- SysAddOut
- SysAddIn
- SysData

All three signals groups are transmitted and received using a technique called *clock forwarding*. Clock forwarding requires the transmitting entity to send a clock with each data or address group. The receiving entity uses the clock to latch the data or address sent from the transmitting entity.

To determining the bus type, the system interface sends the bus cycle type with the address using multiple transactions on the SysAddOut bus. This means that the System Controller must parse the SysAddOut packet and

break it into physical address and bus type commands.

The UP1000 is designed to run the system interface at a clock rate of 100 MHz. The system interface is able to send and receive on both edges of the clock, which means the interface can effectively run at a 200 MHz transfer rate.

### 4.1.2 Memory Interface

The SDRAM interface on the System Controller is a fully compliant PC-100 interface. The System Controller can accommodate three DIMM slots with each slot able to hold SDRAM modules raging from 64 MB to 256 MB.

Registers in the System Controller set the physical address mapping for each DIMM slot. These registers are set by the BIOS during system initialization.

A complete description of the UP1000 memory subsystem is provided in Chapter 5, “System Memory and Address Mapping.”

### 4.1.3 PCI Interface

The PCI bus interfaces through the System Controller to the system interface and the SDRAM bus. The System Controller routes the PCI data to memory when the PCI needs to access the main memory.

The System Controller looks at the physical address (PA) and the command field of SysAddOut, then determines whether a PCI transaction is necessary. See 5.2, “System Space Address Mapping,” on page 5-2 for information on PCI address mapping.

The System Controller determines what type of cycle to place on the PCI bus by decoding the command field. The System Controller supports the following commands:

- WrByte
- WrLWds
- RdBytes
- RdLWds

The transaction command fields issued by the CPU handle legacy x86 special cycles. Special x86 bus cycles are transmitted with a PA of 1 F800 0000 and the WrLWs command. The System Controller then reads the data on the SysData bus to determine what type of special cycle is being transmitted, then places the appropriate action on the PCI bus. Table 4-1 describes the UP1000’s legacy special cycles and their corresponding

system interface SysData values.

**Table 4-1 Special Cycle on the System Interface**

| Special Cycle | Data Value (SysData(31:0)) |
|---|---|
| **Shutdown** | **0000 0000** |
| Halt | 0000 0001 |
| **WB Invalidate** | **0001 0002** |
| Invalidate | 0002 0002 |
| **Flush Ack** | **0003 0002** |
| Stopgrant | 0012 0002 |

To access the System Controller's functional registers, write to PCI configuration registers 0CF8 and 0CFC.

## 4.1.4 PCI Slots

The UP1000 has four PCI slots, with identification (ID) selects that are tied directly to the connectors. All unused features, such as JTAG, are pulled up or down.

The new Power Management (PME) feature is supported on the PCI connectors. The PME pin is connected to all PCI connectors and the AGP connector, and the signal is then routed to enable interrupt generation.

Table 4-2 contains a list of PCI request and selection IDs for the UP1000.

**Table 4-2 PCI Request and Selections for Slots and Devices**

| Device | IDsel | Req/Gnt Pair | IRQ-A | IRQ-B | IRQ-C | IRQ-D |
|---|---|---|---|---|---|---|
| **PCI Slot 1** | **AD19** | **0** | **Int A** | **Int B** | **Int C** | **Int D** |
| PCI Slot 2 | AD20 | 1 | Int D | Int A | Int B | Int C |
| **PCI Slot 3** | **AD21** | **2** | **Int C** | **Int D** | **Int A** | **Int B** |
| PCI Slot 4 | AD22 | 3 | Int B | Int C | Int D | Int A |

**Table 4-2 PCI Request and Selections for Slots and Devices**

| Device | IDsel | Req/Gnt Pair | IRQ-A | IRQ-B | IRQ-C | IRQ-D |
|---|---|---|---|---|---|---|
| **M1543C PCI-ISA Bridge** | **AD18** | **PREQ/ PGNT** | **See Table 4-4.** | | | |
| M1543C PCI-ISA Bridge | AD28 | PREQ / PGNT | See Table 4-4. | | | |
| **M1543C PCI-ISA Bridge** | **AD31** | **PREQ/ PGNT** | **See Table 4-4.** | | | |
| AMD-751 System Controller | AD11 | N / A | N / A | N / A | N / A | N / A |
| **AMD-751 System Controller (AGP)** | **AD12** | **N/A** | **IntA** | **IntB** | **N/A** | **N/A** |

## 4.1.5 AGP Interface

The System Controller implements a fully-compliant AGP bus, and provides a register for managing AGP memory. AGP registers used in the System Controller consist of the following:

- AGP Base Address
- Graphics Address Relocation Table (GART)
- Capability
- Status
- Command
- Virtual Address Size
- AGP / GART Mode

The Virtual Base Address register's value is the bottom address in the system interface domain were the AGP memory starts. The Virtual Address Size register summed with the AGP Base Address provides the top of the AGP address range on the system interface. GART translates the system interface PA to main memory.

## 4.1.6 Clock Generator

The UP1000 uses a two-chip clock solution from Integrated Circuit Systems (ICS). The first chip (ICS9248-64) generates the clocks for the CPU, AGP, and PCI. The second chip (ICS9179-06) is a zero-delay buffer which takes a reference clock from the System Controller and generates the SDRAM clocks.

# 4.2 M1543C PCI-ISA Bridge

The ALI M1543C PCI-ISA Bridge works as a bridge between the PCI and ISA buses, providing fully PCI- and ISA-compatible functions. It also has a set of features to control legacy peripheral devices, with an integrated Super I/O and a keyboard controller.

## 4.2.1 IDE Interface

An on-chip IDE controller supports two separate IDE connectors for up to four IDE devices, providing an interface for IDE hard disk drives and CD ROM drives. UP1000 implements the Ultra Direct Memory Access (DMA) specification which supports a 33 MB per second transfer rate.

## 4.2.2 Super I/O Interface

The on-chip Super I/O incorporates a floppy disk controller, and one parallel and two UART ports. In the UP1000, COM1 and COM2 are implemented.

A parallel port implements standard mode, enhanced mode, and high speed mode functions. It is compliant to SPP, PS/2. EPP, ECP, and 1284 standards.

The floppy disk controller can support up to 1 Mbps data transfer rates and a three-mode drive.

## 4.2.3 USB Interface

UP1000's M1543C PCI-ISA Bridge supports three USB ports. Two ports are dedicated external ports, and the third port is connected to the AGP.

## 4.2.4 SM Bus Interface

The M1543C PCI-ISA Bridge acts as the system management bus host. It communicates with system devices, such as the following:

- the temperature sensor on the Alpha Slot B Module that senses system power voltages and fan speeds
- DIMMs
- revision Electrically Erasable Programmable Read-only Memory (EEPROMs)

The UP1000 has one main SM bus and two sub-SM buses. Access to the sub-SM bus is controlled by a multiplexer (MUX) which sits on the main SM bus.

The SM bus from the Alpha Slot B Module connects the first sub-SM bus; the DIMM EEPROMs are connected to the second sub-SM bus.

SM bus addresses for all UP1000 devices are provided in Table 4-3.

**Table 4-3 SM Bus Address of Each Device**

| Device | Address |
|---|---|
| **ADM 9240 (System Management Unit)** | **0101 100X** |
| ICS9179-06 (Zero delay clock buffer) | 1011 001X |
| **PCF8574AT (LED controller)** | **1010 001X** |
| PCF8574AT(I2C bus MUX controller) | 1010 010X |
| **PCF8582 (MB revision EEPROM)** | **1010 001X** |
| Revision EEPROM on Alpha Slot B Module | 1010 000X |
| **LM79 (Thermal Detector on Alpha Slot B Module)** | **0101 111X** |
| DIMM0 | 1010 000X |
| **DIMM1** | **1010 001X** |
| DIMM2 | 1010 010X |

## 4.2.5 IRQs

The M1543C PCI-ISA Bridge is a PC98 design which provides the functionality recommended to support Windows 95. Through internal configuration registers, each of the following are programmable:

- logic device I/O address
- DMA channel
- Interrupt Requests (IRQs)

There are 128 I/O address location options, 12 IRQ options, and three DMA channel options for each logical device except the keyboard.

Two extra IRQ lines are provided, as well as an ISA IRQ which is steerable to any ISA IRQ. IRQs for the UP1000 are listed in Table 4-4.

**Table 4-4 UP1000 IRQs**

| IRQ | Connection |
|---|---|
| **IRQ0** | **PIT** |
| IRQ1 | Keyboard |
| **IRQ2** | **Cascade of INT-CTRL2** |
| IRQ3 | COM2 |
| **IRQ4** | **COM1** |
| IRQ5 | |
| **IRQ6** | **FDD** |
| IRQ7 | LPT1 |
| **IRQ8** | **Real-time Clock (RTC)** |
| IRQ9 | |
| **IRQ10** | |
| IRQ11 | |
| **IRQ12** | **Mouse** |
| IRQ13 | |
| **IRQ14** | **Primary IDE** |
| IRQ15 | Secondary IDE |

### 4.2.6 DMA

The M1543C PCI-ISA Bridge provides seven programmable DMA channels, four for an 8-bit data size, and three for a 16-bit data size. These seven DMA channels can be arbitrarily programmed as distributed channels.

## 4.3 Flash ROM

The UP1000 has two1 MB Flash ROMs. Both Flash ROMs must be populated. The M1543C PCI-ISA Bridge supports Flash ROM sizes only up to 256 KB. To use these 1 MB ROMs, three general-purpose I/O pins of the M1543C are used to access the 1 MB ROMs as eight blocks of 256 KB.

These Flash parts are connected to the ISA bus using only the lower 8-bit data lines.

Table 4-5 defines the flash ROM usage for the 1 MB ROMs.

**Table 4-5 Flash ROM Usage**

| Address Range | Usage |
|---|---|
| **00_0000–07_FFFF** | **Reset PAL code** |
| 08_0000–0B_FFFF | Alpha Processor, Inc. Alpha Diagnostic Environment (ADE) |
| **0C_0000–1F_BFFF** | **BIOS and BIOS extensions** |
| 1F_A000–1F_BFFF | BIOS Nonvolatile Random Access Memory (NVRAM) |
| **1F_C000–1F_FFFF** | **Reserved** |

## 4.4 RTC

The M5819P RTC provides one hundred calendars, a programmable periodic interrupt with a periodic range from 122 µs to 500 ms, and 242 bytes of static Random Access Memory (RAM).

## 4.5 System Management Unit

System management (SM) on the UP1000 is implemented using I2C protocol, and is controlled through two devices:

- M1543C PCI-ISA Bridge
- ADM9240, SM device

The M1543C PCI-ISA Bridge acts as the central SM device. All system events are directed to the M1543C PCI-ISA Bridge and then onto the processor through interrupt. The processor then invokes an exception handler. During the exception, the M1543C PCI-ISA Bridge can get data from the system management device through the SM bus.

The SM device detects system power voltages and the processor fan speeds, and generates an interrupt when abnormal conditions occurs.

A block diagram of the SM function is provided in Figure 4-1.

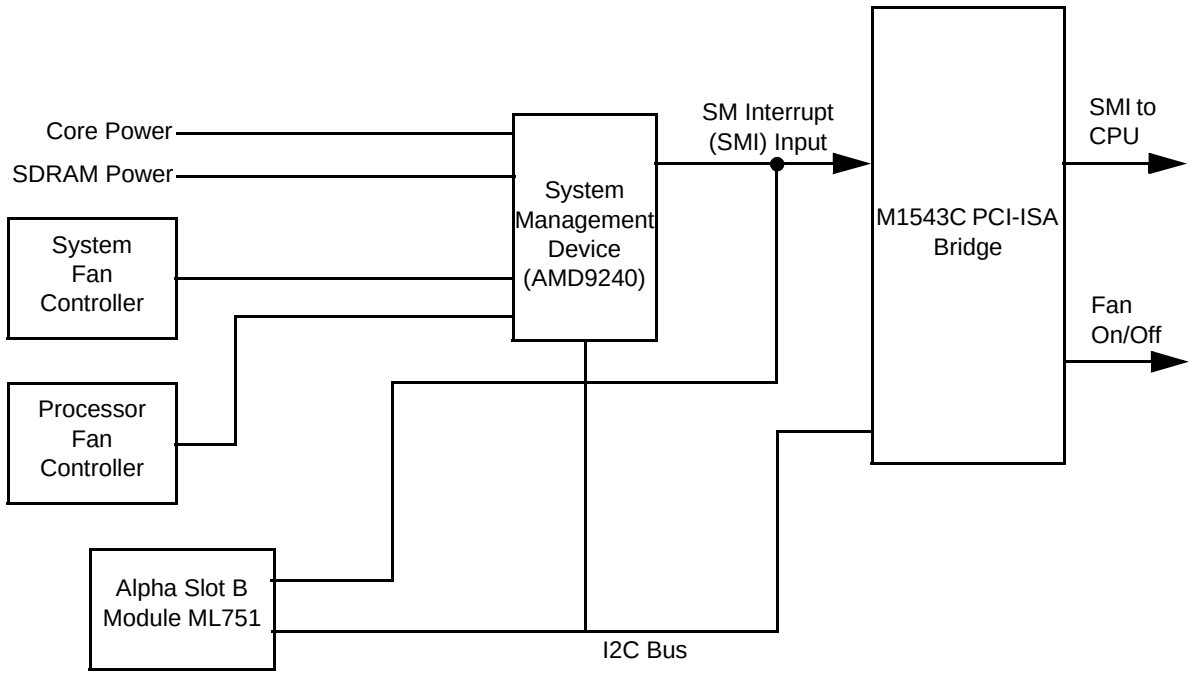



**Figure 4-1 System Management Block Diagram**

## 4.6 System Interface Termination Scheme

The UP1000 must terminate all system interface signals. This termination uses a 100 Ω pull-up resistor, placed within 1 inch of the AMD-751 System Controller, and a 20 Ω serial resistor placed after the pull-up resistor. The pull-up resistor must be placed within 1 inch of the AMD-751 System Controller, and the serial resister must be placed close to the pull-up resistor. The UP1000 has pull-up resistors on the top layer and serial resistors on the bottom layer.

This termination scheme is shown in Figure 4-2.

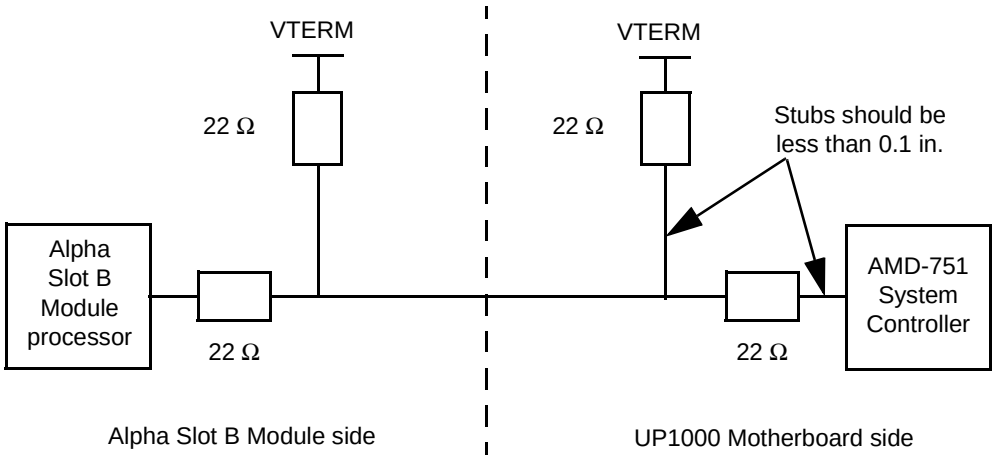



**Figure 4-2 System Interface Termination Scheme**

The pull-up is done with the VTERM voltage source which supplies the system interface termination power. The VTERM voltage is 2V.

## 4.7 Clock Distribution and Termination

The UP1000 uses a two-chip clock solution, ICS 9248-64 and 9179-06, to generate the following system clocks:

- CPU
- PCI
- AGP
- SDRAM
- AMD-751 System Controller

The 9248-64 generates clocks for the CPU, AGP, PCI, and the System Controller, and the reference clock that drives the 9179-06. The 9179-06 is a zero-delay buffer that drives all SDRAM clocks.

Processor SysClk and System Controller SysClk are differential clocks. Differential clocks require parallel routing of the positive (CLK_T) and negative (CLK_C) clocks. They also require a matched line-length between the clock high and clock low.

In addition to the differential clocks, it is also necessary to match line-lengths of the SysClks to the Alpha Slot B Module and the SysClk to the AMD-751 System Controller.

Due to the differential nature of the clock, a unique clock termination

scheme is required. Termination resistors must be placed as near as possible to the 9248-64 chip. Figure 4-3 shows a diagram of the clock termination scheme.

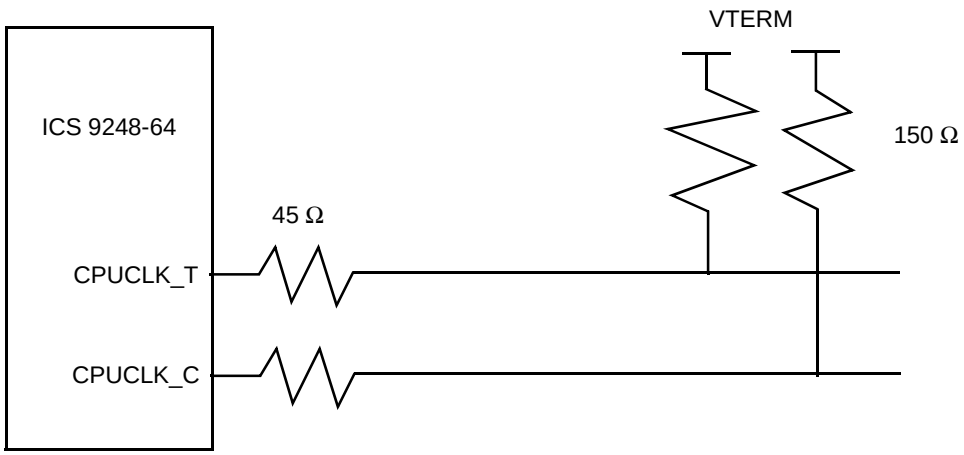



**Figure 4-3 Clock Termination Scheme**

## 4.7.1 System Clock

All the following clocks should be matched in length:

- system clocks
- differential clocks to the processor
- clock to the System Controller
- PCI clock
- AGP clock

On the UP1000 Motherboard, the differential clock to the processor, the AGP clock and PCI clocks are shorter than the system clock to the System Controller (length A). This compensates for the clock length in the Alpha Slot B Module (length B), and the length in the AGP and PCI cards (length C), as follows:

length (A) = length (B + B') = length (C + C')

Refer to Figure 4-4 for an diagram of the system clock logic.

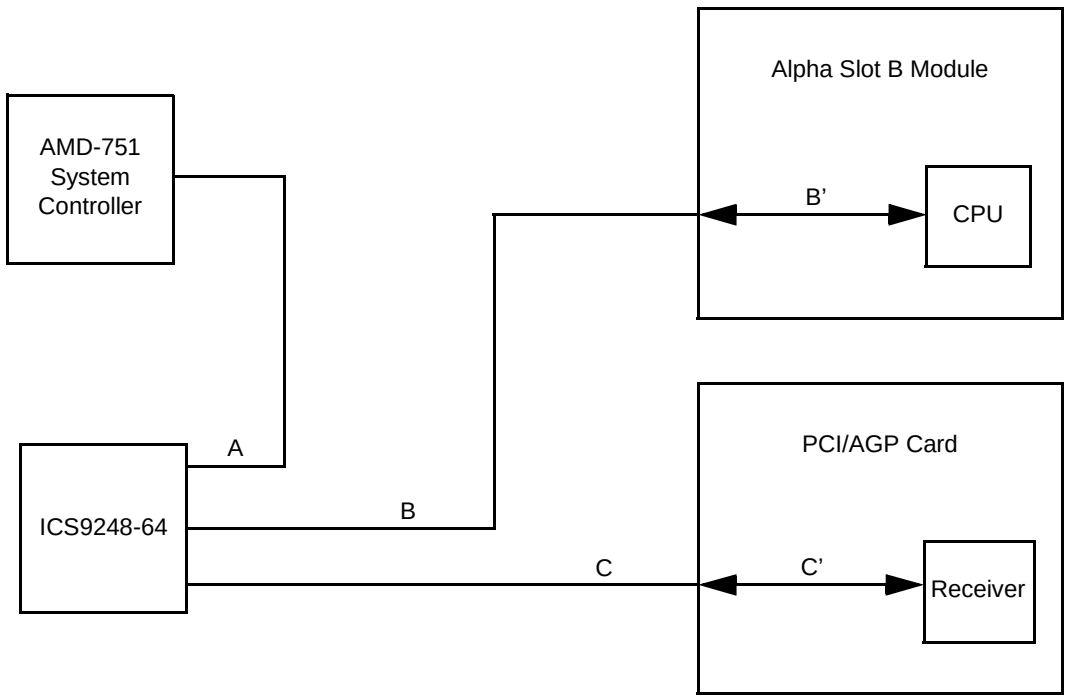



**Figure 4-4 System Clock Logic**

## 4.7.2 SDRAM Clock

The ICS9179-06 generates the 12 SDRAM clocks, taking the reference clock from the AMD-751 System Controller. The SDRAM clock tree must be balanced to synchronize the reference clock coming from the System Controller and the clock input pin on each SDRAM module, as follows:

length (Feedback) = length (Reference CLK) + length (SDRAM CLK) + length (CLK on DIMM module)

Figure 4-5 shows this logic in diagram form.

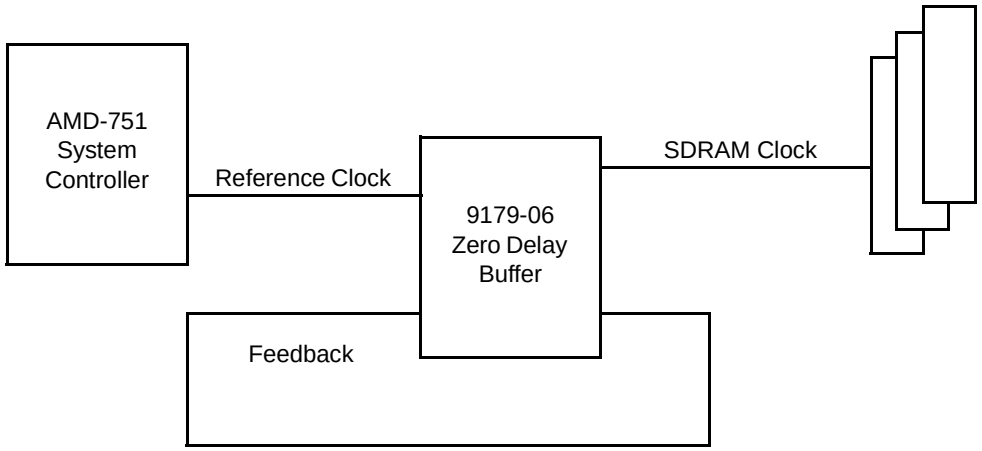



**Figure 4-5 SDRAM Clock Logic**

## 4.8 On-board LEDs

LEDs provide diagnostic information about the UP1000. Of the ten LEDs on the board, only two indicate some user functionality:

- D8, the right-most LED, indicates when Reset PAL codes are loading.
- D9, the green LED, indicates that power to the Alpha Slot B Module is good.

All remaining LEDs are used internally by Alpha Processor, Inc. for diagnostics.

All LEDs are located at the center of the lower edge of the UP1000 Motherboard, below the Alpha Slot B Module and to the right of the I/O connector area. Their organization is shown in Figure 4-6.

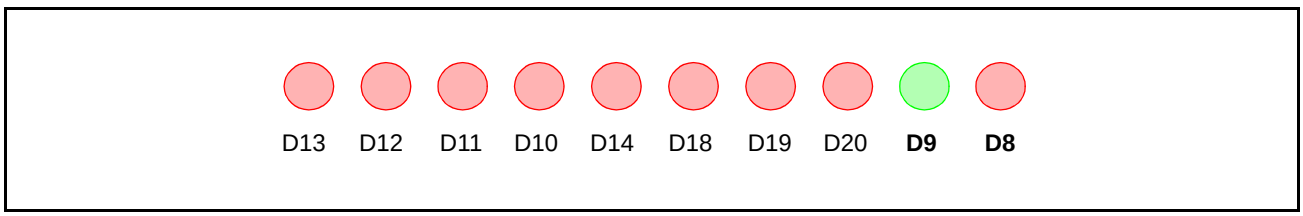



**Figure 4-6 LED Locations**

# 4.9 Firmware

This section describes the UP1000 target OS, and the Reset PAL, ADE and AlphaBIOS firmware. A description is included of the order in which firmware loads and the OS boots.

The UP1000 supports the following firmware versions:

- Reset PAL code—version 17.21 or higher
- ADE—Beta release 1.1 or higher
- AlphaBIOS—version 5.70 or higher
- APB OS loader—Beta release 1.0.0 or higher

The two system ROM images with these firmware versions are contained in Alpha Processor, Inc. parts numbered as follows:

- 90-0001-2C boards—versions 64-0006-2A and 64-0007-2A or higher
- 90-0001-3A boards—versions 64-0006-5A and 64-0007-5A or higher

## 4.9.1 Supported OS

The UP1000 supports all Linux kernel versions from releases 2.0, 2.2 and higher.

***Note:*** *Refer to product support at the Alpha Processor, Inc. web site for current information on specific distributors and versions of Linux supported by the UP1000.*

## 4.9.2 Reset PAL Code

When the UP1000 is turned on or reset, firmware code automatically loads into instruction cache (Icache) in the CPU. This code performs the following:

1. Initialize CPU.
2. Detect configuration jumpers, CPU configuration setting, and memory.
3. Initialize Bcache and set chipset CSRs according to configuration.
4. Initialize system memory.
5. Load the next level of firmware and pass control to that code. (See 4.9.6, "Firmware Loading Order.")

The following devices are tested by the Reset PAL code before loading the ADE firmware:

- Bcache
- System bus and memory controller

- Memory auto-sizing and initial tests
- Path to ROM via M1543C PCI-ISA Bridge

***Note:*** *Due to constraints of the Reset PAL module's execution environment, error reporting and interaction with these diagnostics are not user-friendly.*

### 4.9.3 ADE

The ADE firmware is used internally by Alpha Processor, Inc. for diagnostic purposes.

Native mode diagnostics depends on various system components to be functioning correctly. When Reset PAL code determines that the UP1000 is capable of supporting the higher level environment, it fetches this image from the firmware and transfers control to it.

An Alpha Slot B Module using an 21264 processor implements a serial communications link directly connected to the processor. This link, called the Debug Port, can be used for reporting and interacting in the earliest stages of system initialization, after execution passes from PAL mode. It is accessed through J25 on the UP1000 Motherboard (see Figure 2-1 on page 2-2).

The ADE diagnostics includes the following tests:

- Interrupt handling—Raise interrupts with a known response
- UP1000 Motherboard components—chipset, Flash ROM integrity, on-board devices
- Memory—stress test
- ISA cards
- PCI bus—Initialization, stressing and interrupts
- SM timer support and EEPROMs
- FDD and IDE disks—DMA

If the ADE detects a working keyboard and video console, it displays a graphical interface containing a menu of diagnostics. This is the Console interface to the ADE. If the ADE does not detect a video console, the ADE diagnostics uses the Debug Port interface.

### 4.9.4 AlphaBIOS

AlphaBIOS first establishes the environment in which the APB OS Loader can execute. This environment supports memory management and software PAL commands.

AlphaBIOS uses an ARC call-back routine to provide configuration-dependent services to the OS Loader. It sets up the configuration database, and includes such data as the AlphaBIOS device specification and memory size.

After the OS Loader environment is established and the configuration database exists, AlphaBIOS reads the OS Loader from disk and executes the loading process.

### 4.9.5 APB OS Loader

Alpha Processor, Inc.'s APB OS Loader firmware is a bootstrap loader for Alpha processor-based systems which use AlphaBIOS firmware. It is primarily intended to boot the Linux OS, though it may also be used to load other free BSD derived systems.

Booting Linux with the APB OS Loader involves the following steps:

1. AlphaBIOS loads and transfers control to the APB OS Loader.
2. APB is called with an argument specifying from which device to read the Linux kernel. Additional arguments are passed on to the kernel.
3. APB sets up the environment for Linux, including loading and switching to the correct PAL code, copying kernel arguments to the right location in memory, and more.
4. APB reads the Linux kernel image into memory from the specified device and transfers control to the OS.

### 4.9.6 Firmware Loading Order

UP1000 firmware loads in the following order:

1. Load Reset PAL firmware.
2. Load ADE firmware.
3. Load AlphaBIOS firmware.
4. Run APB Linux OS loader.
5. Run OS.

# Chapter 5 System Memory and Address Mapping

The following sections describe the UP1000 system memory, and includes a list of valid memory configurations. Mapping information for system addresses is also provided.

## 5.1 Memory Subsystem

UP1000 memory consists of three 168-pin, PC 100-compliant DIMM sockets. The DIMM modules have an SM bus connection, which accesses a serial EEPROM on the module.

### 5.1.1 Memory Configurations

The AMD-751 System Controller can support the following size DIMMs:

- 64M
- 128M
- 256M

The UP1000 supports any combination of DIMMs between 64 MB and 768 MB, as shown in Table 5-1.

**Table 5-1 UP1000 Memory Configurations**

| Total Memory | No. of DIMMs | DIMM 2 | DIMM 1 | DIMM 0 |
|---|---|---|---|---|
| **64 MB** | **1** | **64 MB** | | |
| 128 MB | 1 | 128 MB | | |
| | **2** | **64 MB** | **64 MB** | |
| **192 MB** | 2 | 128 MB | 64 MB | |
| 256 MB | **1** | **256 MB** | | |
| | 2 | 128 MB | 128 MB | |
| | **3** | **128 MB** | **64 MB** | **64 MB** |
| **320 MB** | 2 | 256 MB | 64 MB | |

*Note: If only one DIMM is used, it must be installed in the DIMM 2 slot. If multiple DIMMs are used, the modules can be installed in any DIMM slots.*

**Table 5-1 UP1000 Memory Configurations (Continued)**

| Total Memory | No. of DIMMs | DIMM 2 | DIMM 1 | DIMM 0 |
|---|---|---|---|---|
| 384 MB | **2** | **256 MB** | **128 MB** | |
| | 3 | 256 MB | 64 MB | 64 MB |
| **512 MB** | **2** | **256 MB** | **256 MB** | |
| | 3 | 256 MB | 128 MB | 128 MB |
| 576 MB | **3** | **256 MB** | **256 MB** | **64 MB** |
| **640 MB** | 3 | 256 MB | 256 MB | 128 MB |
| 768 MB | **3** | **256 MB** | **256 MB** | **256 MB** |

*Note: If only one DIMM is used, it must be installed in the DIMM 2 slot. If multiple DIMMs are used, the modules can be installed in any DIMM slots.*

### 5.1.2 Memory SM Bus Interface

DIMM modules contain a Serial Presence Detect (SPD) connected to the SM bus. The SPD contains 128-Bytes of data and is stored in serial ROM. The data stored consists of the following:

- Type of module
- Memory size
- Refresh rate
- Operation voltage

Joint Electron Device Engineering Council (JEDEC) standard 21C defines each of the 128 Bytes in the SPD.

## 5.2 System Space Address Mapping

PA space on the system interface maps to PCI space when it is between 1 F800 0000h and 1 FEFF FFFFh. This address range is broken into the specific PCI mapping in Table 5-2.

**Table 5-2 PCI Address Space Mapping**

| PCI Space | Starting Address (PA[34:0]) | Ending Address |
|---|---|---|
| **PCI Configuration** | **1 FE00 0000** | **1 FEFF FFFF** |
| PCI I/O | 1 FC00 0000 | 1 FDFF FFFF |
| **PCI IACK/Special Cycles** | **1 F800 0000** | **1 FBFF FFFF** |
| PCI Memory* | 0 0000 0000 | 0 FFFF FFFF |

***Notes:***

1. *These addresses do not apply if a block memory command is sent with the above address. The command will be a memory access.*
2. *The most-significant bit of the PA is not used for addressing. It is used to distinguish between memory and PCI cycles.*

# Appendix A

## Connectors, Pinouts, and Signals

This appendix describes the connectors and pinouts used on the UP1000 Motherboard. Refer to Figure 2-1 in Chapter 2 for connector locations.

# A.1 Alpha Slot B Connector Pinouts

Table A-1 describes the pinouts of the Alpha Slot B Connector, which is a standard Molex 74191-0002 part.

**Table A-1 Alpha Slot B Connector Pinouts (J1)**

| Pin | Signal (12V) | Signal (12V) | Pin |
|---|---|---|---|
| **A1** | **VTERM** | **VTERM** | **B1** |
| A2 | CONNECT | RESET_L | B2 |
| **A3** | **GND** | **GND** | **B3** |
| A4 | SysDataInClk_L_0 | SysDataOutClk_L_0 | B4 |
| **A5** | **VTERM** | **VTERM** | **B5** |
| A6 | SysData_L_0 | SysCheck_L_0 | B6 |
| **A7** | **GND** | **GND** | **B7** |
| A8 | SysData_L_2 | SysData_L_1 | B8 |
| **A9** | **VTERM** | **VTERM** | **B9** |
| A10 | SysData_L_4 | SysData_L_3 | B10 |
| **A11** | **GND** | **GND** | **B11** |
| A12 | SysData_L_6 | SysData_L_5 | B12 |
| **A13** | **VTERM** | **VTERM** | **B13** |
| A14 | SysCheck_L_1 | SysData_L_7 | B14 |
| **A15** | **GND** | **GND** | **B15** |
| A16 | SysDataInClk_L_1 | SysDataOutClk_L_1 | B16 |
| **A17** | **VTERM** | **VTERM** | **B17** |
| A18 | SysData_L_9 | SysData_L_8 | B18 |
| **A19** | **GND** | **GND** | **B19** |
| A20 | SysData_L_11 | SysData_L_10 | B20 |
| **A21** | **VTERM** | **VTERM** | **B21** |
| A22 | SysData_L_13 | SysData_L_12 | B22 |
| **A23** | **GND** | **GND** | **B23** |
| A24 | SysData_L_15 | SysData_L_14 | B24 |
| **A25** | **VTERM** | **VTERM** | **B25** |
| A26 | SysDataInClk_L_2 | SysDataOutClk_L_2 | B26 |

**Table A-1 Alpha Slot B Connector Pinouts (J1) (Continued)**

| Pin | Signal (12V) | Signal (12V) | Pin |
|---|---|---|---|
| **A27** | **GND** | **GND** | **B27** |
| A28 | SysData_L_16 | SysCheck_L_2 | B28 |
| **A29** | **VTERM** | **VTERM** | **B29** |
| A30 | SysData_L_18 | SysData_L_17 | B30 |
| **A31** | **GND** | **GND** | **B31** |
| A32 | SysData_L_20 | SysData_L_19 | B32 |
| **A33** | **VTERM** | **VTERM** | **B33** |
| A34 | SysData_L_22 | SysData_L_21 | B34 |
| **A35** | **GND** | **GND** | **B35** |
| A36 | SysCheck_L_3 | SysData_L_23 | B36 |
| **A37** | **VTERM** | **VTERM** | **B37** |
| A38 | SysDataInClk_L_3 | SysDataOutClk_L_3 | B38 |
| **A39** | **GND** | **GND** | **B39** |
| A40 | SysData_L_25 | SysData_L_24 | B40 |
| **A41** | **VTERM** | **VTERM** | **B41** |
| A42 | SysData_L_27 | SysData_L_26 | B42 |
| **A43** | **GND** | **GND** | **B43** |
| A44 | SysData_L_29 | SysData_L_28 | B44 |
| **A45** | **VTERM** | **VTERM** | **B45** |
| A46 | SysData_L_31 | SysData_L_30 | B46 |
| **A47** | **GND** | **GND** | **B47** |
| A48 | ClkIn_H | ClkIn_L | B48 |
| **A49** | **VTERM** | **VTERM** | **B49** |
| A50 | FrameClk_H | FrameClk_L | B50 |
| **A51** | **GND** | **GND** | **B51** |
| A52 | SysDataInValid_L | SysDataOutValid_L | B52 |
| **A53** | **VTERM** | **VTERM** | **B53** |
| A54 | SysFillValid_L | ClkFwdRst_H | B54 |
| **A55** | **GND** | **GND** | **B55** |
| A56 | PWROK | PROCRDY / Srom_OE_L | B56 |
| **A57** | **VTERM** | **VTERM** | **B57** |
| A58 | SysAddIn_L_14 | SysAddIn_L_13 | B58 |
| **A59** | **GND** | **GND** | **B59** |
| A60 | SysAddIn_L_12 | SysAddIn_L_11 | B60 |

**Table A-1 Alpha Slot B Connector Pinouts (J1) (Continued)**

| Pin | Signal (12V) | Signal (12V) | Pin |
|---|---|---|---|
| **A61** | **VTERM** | **VTERM** | **B61** |
| A62 | SysAddIn_L_10 | SysAddIn_L_9 | B62 |
| **A63** | **GND** | **GND** | **B63** |
| A64 | SysAddIn_L_8 | SysAddIn_L_7 | B64 |
| **A65** | **VTERM** | **VTERM** | **B65** |
| A66 | SysAddInClk_L | SysAddIn_L_6 | B66 |
| **A67** | **GND** | **GND** | **B67** |
| A68 | SysAddIn_L_5 | SysAddIn_L_4 | B68 |
| **A69** | **VTERM** | **VTERM** | **B69** |
| A70 | SysAddIn_L_3 | SysAddIn_L_2 | B70 |
| **A71** | **GND** | **GND** | **B71** |
| A72 | SysAddIn_L_1 | SysAddIn_L_0 | B72 |
| **A73** | **VTERM** | **VTERM** | **B73** |
| A74 | SysAddOut_L_14 | SysAddOut_L_13 | B74 |
| **A75** | **GND** | **GND** | **B75** |
| A76 | SysAddOut_L_12 | SysAddOut_L_11 | B76 |
| **A77** | **VTERM** | **VTERM** | **B77** |
| A78 | SysAddOut_L_10 | SysAddOut_L_9 | B78 |
| **A79** | **GND** | **GND** | **B79** |
| A80 | SysAddOut_L_8 | SysAddOut_L_7 | B80 |
| **A81** | **VTERM** | **VTERM** | **B81** |
| A82 | SysAddOutClk_L | SysAddOut_L_6 | B82 |
| **A83** | **GND** | **GND** | **B83** |
| A84 | SysAddOut_L_5 | SysAddOut_L_4 | B84 |
| **A85** | **VTERM** | **VTERM** | **B85** |
| A86 | SysAddOut_L_3 | SysAddOut_L_2 | B86 |
| **A87** | **GND** | **GND** | **B87** |
| A88 | SysAddOut_L_1 | SysAddOut_L_0 | B88 |
| **A89** | **VTERM** | **VTERM** | **B89** |
| A90 | SysData_L_63 | SysData_L_62 | B90 |
| **A91** | **GND** | **GND** | **B91** |
| A92 | SysData_L_61 | SysData_L_60 | B92 |
| **A93** | **VTERM** | **VTERM** | **B93** |
| A94 | SysData_L_59 | SysData_L_58 | B94 |

**Table A-1 Alpha Slot B Connector Pinouts (J1) (Continued)**

| Pin | Signal (12V) | Signal (12V) | Pin |
|---|---|---|---|
| **A95** | **GND** | **GND** | **B95** |
| A96 | SysData_L_57 | SysData_L_56 | B96 |
| **A97** | **VTERM** | **VTERM** | **B97** |
| A98 | SysDataInClk_L_7 | SysDataOutClk_L_7 | B98 |
| **A99** | **GND** | **GND** | **B99** |
| A100 | SysCheck_L_7 | SysData_L_55 | B100 |
| **A101** | **VTERM** | **VTERM** | **B101** |
| A102 | SysData_L_54 | SysData_L_53 | B102 |
| **A103** | **GND** | **GND** | **B103** |
| A104 | SysData_L_52 | SysData_L_51 | B104 |
| **A105** | **VTERM** | **VTERM** | **B105** |
| A106 | SysData_L_50 | SysData_L_49 | B106 |
| **A107** | **GND** | **GND** | **B107** |
| A108 | SysData_L_48 | SysCheck_L_6 | B108 |
| **A109** | **VTERM** | **VTERM** | **B109** |
| A110 | SysDataInClk_L_6 | SysDataOutClk_L_6 | B110 |
| **A111** | **GND** | **GND** | **B111** |
| A112 | SysData_L_47 | SysData_L_46 | B112 |
| **A113** | **VTERM** | **VTERM** | **B113** |
| A114 | SysData_L_45 | SysData_L_44 | B114 |
| **A115** | **GND** | **GND** | **B115** |
| A116 | SysData_L_43 | SysData_L_42 | B116 |
| **A117** | **VCC_CORE** | **VCC_CORE** | **B117** |
| A118 | SramPowerLevel | Core_PowerGood | B118 |
| **A119** | **GND** | **GND** | **B119** |
| A120 | SysData_L_41 | SysData_L_40 | B120 |
| **A121** | **VCC** | **VCC** | **B121** |
| A122 | SysDataInClk_L_5 | SysDataOutClk_L_5 | B122 |
| **A123** | **GND** | **GND** | **B123** |
| A124 | SysCheck_L_5 | SysData_L_39 | B124 |
| **A125** | **VCC_SRAM** | **VCC_SRAM** | **B125** |
| A126 | SysData_L_38 | SysData_L_37 | B126 |
| **A127** | **GND** | **GND** | **B127** |
| A128 | SysData_L_36 | SysData_L_35 | B128 |

**Table A-1 Alpha Slot B Connector Pinouts (J1) (Continued)**

| Pin | Signal (12V) | Signal (12V) | Pin |
|---|---|---|---|
| **A129** | **V33** | **V33** | **B129** |
| A130 | SysData_L_34 | SysData_L_33 | B130 |
| **A131** | **GND** | **GND** | **B131** |
| A132 | SysData_L_32 | SysCheck_L_4 | B132 |
| **A133** | **V33** | **V33** | **B133** |
| A134 | SysDataInClk_L_4 | SysDataOutClk_L_4 | B134 |
| **A135** | **GND** | **GND** | **B135** |
| A136 | SromClk_H | SromData_H | B136 |
| **A137** | **V33** | **V33** | **B137** |
| A138 | SRAM_ZZ | CORE_PWREN | B138 |
| **A139** | **GND** | **GND** | **B139** |
| A140 | FIDSEL_L_0 | FIDSEL_L_1 | B140 |
| **A141** | **V33** | **V33** | **B141** |
| A142 | APIC_CLK | APIC_DATA_0 | B142 |
| **A143** | **VP12** | **VP12** | **B143** |
| A144 | APIC_DATA_1 | FERR | B144 |
| **A145** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B145** |
| A146 | ALPHA_H/K7_L | CPU_Present | B146 |
| **A147** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B147** |
| A148 | FID_0 | FID_1 | B148 |
| **A149** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B149** |
| A150 | FID_2 | FID_3 | B150 |
| **A151** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B151** |
| A152 | I2C_ADDR_0 | I2C_ADDR_1 | B152 |
| **A153** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B153** |
| A154 | I2C_ADDR_2 | I2C_INTR_L | B154 |
| **A155** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B155** |
| A156 | I2C_SCLK | I2C_SDA | B156 |
| **A157** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B157** |
| A158 | INIT_L | IGNNE_L | B158 |
| **A159** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B159** |
| A160 | IRQ_H_0/NMI | IRQ_H_1/INTR | B160 |
| **A161** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B161** |
| A162 | IRQ_H_2/SMI_L | IRQ_H_3/STPCLK_L | B162 |

**Table A-1 Alpha Slot B Connector Pinouts (J1) (Continued)**

| Pin | Signal (12V) | Signal (12V) | Pin |
|---|---|---|---|
| **A163** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B163** |
| A164 | IRQ_H_4/SCIINT_L | IRQ_H_5/A20M_L | B164 |
| **A165** | **VRM_SOURCE_POWER (12 V)** | **VRM_SOURCE_POWER (12 V)** | **B165** |

# A.2 Power Connector Pinouts

Pinouts for J21, the ATX power connector, are shown in Table A-2. J21 is a standard Molex 39-29-9202 connector.

**Table A-2 ATX Power Connector Pinouts (J21)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| **1** | **+3.3 VDC** | **11** | **+3.3 VDC** |
| 2 | +3.3 VDC | 12 | -12 VDC |
| **3** | **GND** | **13** | **GND** |
| 4 | +5 VDC | 14 | PS_ON |
| **5** | **GND** | **15** | **GND** |
| 6 | +5 VDC | 16 | GND |
| **7** | **GND** | **17** | **GND** |
| 8 | P_DCOK | 18 | -5 VDC |
| **9** | **5V SB** | **19** | **+5 VDC** |
| 10 | +12 VDC | 20 | +5 VDC |

Table A-3 shows the pinouts for J22, an AUX ATX +3V power connector (PSCONN6). This part is a Molex 15-48-0412 connector.

**Table A-3 AUX ATX Power Connector (PSCONN6) Pinouts (J22)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| **1** | **GND** | **4** | **+3.3 VDC** |
| 2 | GND | 5 | +3.3 VDC |
| **3** | **GND** | **6** | **+5 VDC** |

Pinouts for J23, the Alpha Slot B Module +12V power connector (PSCONN4), are shown in Table A-4. J23 is a Molex 15-24-4345 connector.

**Table A-4 Alpha Slot B Module Power Connector (PSCONN4) Pinouts (J23)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| **1** | **+12 VDC** | **3** | **GND** |
| 2 | GND | 4 | +5 VDC |

# A.3 Nonstandard Connections

Pinouts for J13, the EPLD program port, are shown in Table A-5. J13 is a Molex 87256-1011 connector.

***Note:*** *For specific information on the EPLD device used in the UP1000, refer to Altera Corporation's Max 7000 Programmable Logic Device Family Data Sheet, Document #A-DS-M7000-05.03.*

**Table A-5 PLD Program Port Connector Pinouts (J13)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| **1** | **TCK** | **6** | **No Connect (NC)** |
| 2 | GND | 7 | NC |
| **3** | **TDO** | **8** | **NC** |
| 4 | VCC | 9 | TDI |
| **5** | **TMS** | **10** | **GND** |

Pinouts for J25, the Debug port, are shown in Table A-6. J25 is an AMP 103240-3 connector.

**Table A-6 Debug Port Connector Pinouts (J25)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| **1** | **NC** | **4** | **NC** |
| 2 | TxD | 5 | RxD |
| **3** | **GND** | **6** | **NC** |

Pinouts for J30, the Speaker cable, are shown in Table A-7. J30 is an AMP 103239-4 connector.

**Table A-7 Speaker Cable Connector Pinouts (J30)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| **1** | **VCC** | **3** | **GND** |
| 2 | GND | 4 | GND |

Pinouts for J36, the SM bus extender port, are shown in Table A-8. J36 is a Molex 22-23-2031 connector.

**Table A-8 SM Bus Extender Port Connector Pinouts (J36)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| **1** | **SMbus_clock** | **3** | **SMbus_data** |
| 2 | GND | | |

# A.4 Standard Connectors

Industry standard parts are used for most of the connections in the UP1000. Refer to Table A-9 for a list of the connectors used and their functions.

**Table A-9 UP1000 Standard Connectors**

| Connector | Function | Part Number |
|---|---|---|
| **J2** | **AGP** | **Molex 71796-0008 or AMP 145263-1** |
| J3–J5 | SDRAM DIMMs | Molex 71251-0012 |
| **J6–J9** | **32-bit PCI bus** | **AMP 145154-4** |
| J10, J11 | IDE drive bus | Molex 87256-4011 or AMP 103308-8 |
| **J12** | **FDD** | **Molex 87256-3411 or AMP 103308-7** |
| J14 | Parallel bus and COM1/COM2 serial line | Foxconn DM11351-Z5 |
| **J17** | **USB** | **AMP 787617-1** |
| J18 | Keyboard and mouse | Foxconn MH11067-D2 or AMP 84405-1 or 84376-1 |
| **J19, J20** | **ISA expansion bus** | **AMP 645169-3** |
| J24 | Reset switch cable | AMP 103239-2 |
| **J27** | **System power switch cable** | **AMP 103239-2** |
| J28 | Optional fan* | Molex 22-23-2031 |
| **J29** | **Power LED** | **AMP 103239-5** |
| J31 | Chassis fan | Molex 22-23-2031 |
| **J32, J33** | **Alpha Slot B Module fan power cable** | **Molex 22-23-2031** |
| J35 | Keyboard lock cable | AMP 103239-2 |

*Note: * J28 is only present on the 90-0001-2C board.*

# A.5 Signal Descriptions

This section describes all signals present on the UP1000 Motherboard, organized by function.

## A.5.1 System Interface

**Table A-10 System Interface Signals**

| Signal | Description |
|---|---|
| **SYSDATA_N[63:0]** | **The bidirectional interface to and from the processor and system for data movement. Data is skew-aligned with either the SDATAINCLK[3:0]# bus or SDATAOUTCLK[3: 0]# bus. Both rising and falling edges are used to transfer data.** |
| SYSCHECK_N[7:0] | Contains the ECC check bits for data transferred on the SDATA[63:0]# bus. |
| **SYSADDIN_N[14:0]** | **The unidirectional system Address/ command interface to the processor from the system. It is used to transfer probes or data movement commands into the processor. All probes and commands on the SADDIN[14:2]# bus are skew-aligned with the forward clock, SADDINCLK#.** |
| SYSADDOUT_N[14:0] | The unidirectional system address interface from the processor to the AMD-751 system controller.<br>The SADDOUT[14:2]# bus is used to transfer processor Commands or probe responses to the system. All commands on bus are skew-aligned with the forward clock, SADDOUTCLK#. |
| **SYSDATAINCLK_N[4:0]** | **The single-ended forwarded clock driven by the AMD-751 system controller to transfer data on SDATA[63:0]#. Each 16-bit data word is skew-aligned with this clock. Both rising and falling edges are used to transfer data.** |
| SYSDATAOUTCLK_N[4:0] | The single-ended forwarded clock driven by the processor and is used to transfer data on the SDATA[63:0]# bus. Both rising and falling edges are used to transfer data. |
| **SYSADDINCLK_N[4:0]** | **The single-ended forwarded clock for the SADDIN[14:2]# bus that is driven by the AMD-751 system controller. Both rising and falling edges are used to transfer addresses or commands (probes) to the processor.** |
| SYSADDOUTCLK_N[4:0] | The single-ended forwarded clock for the SADDOUT[14:2]# bus driven by the processor. Both rising and falling edges are used to transfer commands or probe responses. |
| **CPUCLKIN_H** | **Processor clock.** |
| CPUCLKIN_L | Processor clock. |
| **FRAMECLK_N** | **System Controller clock.** |
| CLKFWDRST_N | Resets the clock forward circuitry for the processor. |
| **CONNECT_N** | **Output from the AMD-751 system controller, used for power management and clock-forward initialization at reset.** |
| SYSFILLVALID_N | Validate the current memory I/O transfer into the processor. |
| **SYSDATAINVALID_N** | **Driven by the AMD-751 system controller, controls the flow of data into the processor. SDATAINVAL# can be used to introduce an arbitrary number of cycles between octawords (128 bits).** |

## A.5.2 AGP

**Table A-11 AGP Signals**

| Signal | Description |
|---|---|
| **AGPCLK1** | **A_CLK receives a 66-MHz clock from the system clock generator. A_CLK is used by the AMD-751 system controller logic in the AGP clock domain.** |
| AGP_AD[32:0] | In multiplexed mode, A_AD[31:0] contain an AGP address when PIPE# is sampled asserted and data when PIPE# is sampled negated. In demultiplexed mode, A_AD[31:0] contain only AGP data, while AGP addresses are provided on the sideband address signals SBA[7:0]. |
| **AGP_AD_STB[1:0]** | **In 2x mode, ADSTB0 provides timing for A_AD[15:0] and ADSTB1 provides timing for A_AD[31:16]. The graphics controller drives the strobes during AGP write operations, and the AMD-751 system controller drives them during AGP read operations. ADSTB[1:0] serves as a source-synchronized strobe when transferring data in demultiplexed mode. This signal is essentially a copy of the clock that is synchronized to the data. This source-synchronized technique minimizes skew between the strobe and data and compensates for propagation delay. In 1x mode, ADSTB[1:0] is ignored while SYSCLK is used.** |
| AGP_SB_STB | This signal is used to strobe-in commands on the SBA bus to its request queue. |
| **AGP_TRDY_N** | **As an AGP target, the AMD-751 system controller asserts A_TRDY# to signal the start of a read or write data block transfer. A block is the amount of data that can be passed in four SYSCLK cycles—four doublewords in 1x mode, eight doublewords in 2x mode. If a transfer is larger than one block, A_TRDY# must be reasserted for each block. Asserting A_TRDY# every four clock cycles completes the transfer without wait states. As an AGP initiator, the AMD-751 samples A_TRDY# to Determine if data is ready to be transferred.** |
| AGP_IRDY_N | AGP_IRDY_N indicates the initiator is ready to transfer a block. For an AGP write transfer, all data in the given transaction is sent without wait-states, so AGP_IRDY_N only needs to be sampled once in the entire transaction.. An AGP read transfer can have wait-states, so the AMD-751 must sample AGP_IRDY_N asserted for each block of a read transfer. |
| **AGP_REQ_N** | **As the bus arbiter, the AMD-751 system controller monitors A_REQ# to determine if the graphics controller requests access to the AGP bus. If A_REQ# is sampled asserted, the arbiter asserts A_GNT# as soon as the bus is available.** |

**Table A-11 AGP Signals (Continued)**

| Signal | Description |
|---|---|
| AGP_GNT_N | As the AGP bus arbiter, the AMD-751 system controller asserts A_GNT# in response to A_REQ from the initiator (graphics controller) to indicate to the initiator that it has been granted control of the bus. At the same time, the system controller provides status information on status signals ST[2:0] to Indicate to the initiator if it is to supply data or receive data in response to a previously queued request. |
| **AGP_PAR** | **A_PAR# is used for PCI transfers on the secondary PCI bus. Its function is the same as that of PAR# on the primary PCI bus.** |
| AGP_PERR_N | Asserted when AGP bus data parity error. |
| **AGP_SERR_N** | **Asserted when system error is detected.** |
| AGP_STOP_N | AGP_STOP_N is used for PCI transfers on the secondary PCI bus. Its function is the same as that of PCI_STOP# on the primary PCI bus.<br>AGP_STOP_N is not used during AGP transfers. |
| **AGP_FRAME_N** | **A_FRAME# is used for PCI transfers on the secondary PCI bus. Its function is the same as that of FRAME# on the primary PCI bus. A_FRAME# is not used during AGP transfers.** |
| AGP_DEVSEL_N | A_DEVSEL# is used for PCI transfers on the secondary PCI bus. Its function is the same as that of DEVSEL# on the primary PCI bus. A_DEVSEL# is not used during AGP transfers. |
| **AGP_PIPE_N** | **The assertion of PIPE# indicates the beginning of a new bus cycle. The AMD-751 system controller queues a request from the initiator on each rising clock edge on which it samples PIPE# asserted. When PIPE# is sampled negated, no new requests are queued.** |
| AGP_RBP_N | An AGP initiator asserts RBF# to indicate that its buffers are full. As an AGP target, the AMD-751 system controller cannot commence a low priority data read to the initiator until it samples RBF# negated. RBF# does not apply to high-priority read data. |
| **AGP_ST[2:0]** | **As the AGP arbiter, the AMD-751 system controller drives ST[2:0] when it asserts A_GNT# to inform the graphics Controller of the type of data being returned or that the AMD-751 is ready to accept a command.** |
| AGP_USB_N | USB signal. |
| **AGP_USB_P** | **USB signal.** |
| PCI_PME_N | Power management interrupt signal. |
| **AGP_USBOVCR_N** | **Over current detection signal.** |
| AGPUSB_PWR | USB power. |

## A.5.3 PCI

**Table A-12 PCI Signals**

| Signal | Description |
|---|---|
| **PCIRSTJ** | **Reset the PCI bus.** |
| AD[31:0] | The AD[31:0] bus contains the standard, multiplexed PCI address and data lines. AD[31:0] contains a physical address during the first clock of a PCI transaction, and data during subsequent clocks. The address is driven when FRAME# is asserted, and data is driven or received in subsequent cycles. When the AMD-751 system controller is the PCI initiator, these lines are outputs during the address and write data phases of a transaction, and inputs during read data phases. When the AMD-751 is the PCI target, these lines are inputs during the address and write data phases of a transaction, and outputs during read data phases. |
| **CBEJ[3:0]** | **C/BE[3:0]# contain the PCI command during the first clock cycle that FRAME# is asserted. These signals serve as a byte-enable signal for subsequent cycles.** |
| FRAMEJ | The AMD-751 system controller asserts FRAME# at the beginning of a PCI cycle when it is the initiator, and holds it asserted until the beginning of the last data transfer in the cycle. If the AMD-751 is the targeted PCI device, it samples and latches the C/BE[3:0]# and AD[31:0] signals and asserts DEVSEL# at the first PCLK edge on which it samples FRAME# asserted. |
| **TRDYJ** | **As a PCI initiator, the AMD-751 system controller samples TRDY# to determine when the target agent is able to complete the data phase of a transaction.**<br>**As a PCI target, the AMD-751 asserts TRDY# to indicate that it has latched the data on AD[31:0] during a write phase or Driven data on AD[31:0] during a read phase.** |
| IRDYJ | IRDY# indicates that a PCI initiator is ready to complete the Current data phase of the transaction. During a read cycle, IRDY# asserted indicates the master is ready to accept the Data. During a write cycle, IRDY# asserted indicates that write Data is valid on AD[31:0]. Data is transferred on the PCI bus on each PCLK in which both IRDY# and TRDY# are asserted. Wait states are inserted on the bus until both IRDY# and TRDY# are asserted together. |
| **STOPJ** | **This signal is asserted when the target device requires it to abort or retry a transaction.** |
| DEVSELJ | The AMD-751 system controller samples DEVSEL# when it is the initiator in a PCI cycle to determine if the target device has responded. The AMD-751 drives DEVSEL# when it is the targeted device in a PCI cycle. |

**Table A-12 PCI Signals (Continued)**

| Signal | Description |
|---|---|
| **SERRJ** | **The AMD-751 system controller, as a PCI agent, asserts SERR# off the rising edge of PCLK one clock after it detects a system error. SERR# is an input to the AMD-756 peripheral bus controller, which can be programmed to generate a Non-maskable Interrupt (NMI).** |
| PAR | PAR indicates even parity. The AMD-751 system controller Drives PAR as a PCI initiator one clock after the address phase and each data write phase to generate even parity across AD[31:0] and C/BE[3:0]#. The AMD-751 drives PAR as a PCI target one clock after each data read phase. The AMD-751 does not support parity checking. |
| **PHLDAJ** | **Grant signal to the M1543C PCI-ISA Bridge for PCI bus master.** |
| INTAJ_MI | Interrupt signal. |
| **INTBJS0** | **Interrupt signal.** |
| INTCJS1 | Interrupt signal. |
| **INTDJS2** | **Interrupt signal.** |
| PCI_PME_N | Power management interrupt signal. |

## A.5.4 ISA

**Table A-13 ISA Signals**

| Signal | Description |
|---|---|
| **RSTDRV** | **This output is used to reset the ISA Bus and the system device. This pin will be active if the system reset is needed.** |
| SA[19:0] | These pins should connect to the ISA System Address Bus. |
| **LA[23:17]** | **They are inputs during ISA master cycle and should connect to ISA Slot Latch Address Bus.** |
| SD[15:0] | ISA DATA bus. |
| **DRQ[7:0]** | **DMA request signals.** |
| DACK[7:0] | DMA Acknowledge signals. |
| **IOCHCK_N** | **ISA bus parity error check signal. The M1543C PCI-ISA Bridge generates NMI when this signal is asserted.** |
| IOCHRDY_N | ISA system ready signal. |
| **AEN** | **ISA I/O address enable. This signal will become active high during DMA cycle to prevent I/O device to decode DMA cycles as valid I/O cycles.** |

**Table A-13 ISA Signals (Continued)**

| Signal | Description |
|---|---|
| SBHE_N | ISA byte high enable. |
| **MEMR_N** | **ISA memory read.** |
| MEMW_N | ISA memory write. |
| **MASTER_N** | **Indicates an ISA master cycle.** |
| IOCS16_N | ISA 16 bit I/O device indicator. |
| **MEMCS16_N** | **ISA 16 bit memory device indicator.** |
| OSC | ISA system clock. |
| **BALE** | **BALE will be asserted throughout DMA, ISA master, and the Refresh cycles. Otherwise, it will only assert half the SYSCLK before the ISA command is asserted.** |
| TC | DMA end of process. |
| **REFRESH_N** | **ISA refresh signal.** |
| IOR_N | ISA I/O read. |
| **IOW_N** | **ISA I/O write.** |
| SMEMR_N | ISA system memory read. This signal indicates that the memory read command is below 1 MB address. |
| **SMEMW_N** | **ISA system memory write. This signal indicates that the memory write command is below 1 MB address.** |
| NOWS_N | This signal terminates the CPU-to-ISA command instantly. |
| **IRQ[15:0]** | **Interrupt signals.** |

## A.5.5 IDE

**Table A-14 IDE Signals**

| Signal | Description |
|---|---|
| **RSTDRV** | **IDE reset.** |
| HDDP[15:0] | Primary Hard Disk Drive (HDD) date. |
| **HDDRQP_N** | **Primary HDD DMA request.** |
| HDIOWP_N | Primary HDD I/O write. |
| **HDIORP_N** | **Primary HDD I/O read.** |
| HDCHRDYP_N | Primary HDD ready. |
| **HDDACKP_N** | **Primary HDD DMA acknowledge.** |
| HDCS3P_N | IDE chip select 3 for primary HDD. |

**Table A-14 IDE Signals (Continued)**

| Signal | Description |
|---|---|
| **HDAP[2:0]** | **Primary IDE ATA address bus.** |
| HDACT_N | HDD activity led signal. |
| **HDDS[15:0]** | **Secondary HDD data.** |
| HDDRQS_N | Secondary HDD DMA request. |
| **HDIOWS_N** | **Secondary HDD I/O write.** |
| HDIORS_N | Secondary HDD I/O read. |
| **HDCHRDYS_N** | **Secondary HDD ready.** |
| HDDACKS_N | Secondary HDD DMA acknowledge. |
| **HDCS3S_N** | **IDE chip select 3 for secondary HDD.** |
| HDAS[2:0] | Secondary ATA address bus. |

## A.5.6 Floppy Disk Drive

**Table A-15 FDD Signals**

| Signal | Description |
|---|---|
| **DRVDEN(densel)** | **Indicates whether a low (250/300 Kb/s) or high (500/1000 Kb/s) data rate has been selected.** |
| INDEX_N(index_n) | This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole. |
| **MTR0_N(mot0_n)** | **These active-low outputs select motor drives 0-1.** |
| DS1_N(drv1_n) | An additional Drive Select signals in PPM mode. Drive Select signal 0 and 1 are multiplexed with STROBJ and ACKJ. |
| **DS0_N(drv0_n)** | **Active low output select drives 0-1.** |
| MTR1_N(mot1_n) | Additional Motor On signals in PPM mode. Motor On 0 and 1 are multiplexed with PD[6] and BUSY. |
| **DIR_N(dir_n)** | **This active low output determines the direction of the head movement (low =step-in, high = step-out).** |
| STEP_N(step_n) | This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation. |
| **WDATA_N(wdata)** | **This active low output is a write- pre compensated serial detonate the selected disk drive. Each falling edge causes a flux change on the media. to be written.** |
| WGATE_N(wgate) | This active-low, high-drive output enables the write circuitry of the selected disk drive. |

**Table A-15 FDD Signals (Continued)**

| Signal | Description |
|---|---|
| **TR0_N(trk0_n)** | **This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.** |
| WPROT_N(wprot_n) | This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write protected. |
| **RDATA_N(rdata_n)** | **The active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.** |
| HDSEL_N(hdsel_n) | This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1. |
| **DSKCHG_N(dshchg_n)** | **This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of location base+7.** |

## A.5.7 Front Panel

**Table A-16 Front Panel Signals**

| Signal | Description |
|---|---|
| **PWR** | **Signal for multifunctional front switch Power on/Sleep.** |
| SPKR | Speaker signal. |
| **RST** | **Reset signal (Optional).** |
| HDDACT | Hard disk activity indicator LED (Optional). |
| **PWRLED** | **Power Indicator LED.** |

# Appendix B

## Support,

## Products and

## Documentation

# B.1 Customer Support

Alpha Processor, Inc. provides assistance for their products on their web page at www.alpha-processor.com.

Alpha OEMs provide the following web page resources for customer support:

| URL | Description |
|---|---|
| **http://www.compaq.com** | **Contains links for the Alpha Slot B Module CPU.** |
| http://www.amd.com | Contains links for the AMD-751 System Controller. |
| **http://www.acerlabs.com** | **Contains links for the M1543C PCI-ISA Bridge.** |

# B.2 Supporting Products

Alpha Processor, Inc. maintains a Hardware Compatibility List on their web site for components and accessories that are not included with the UP1000. Compatibility for items such as memory, power supplies, and enclosure are listed.

Point your browser to www.alpha-processor.com and check the Product Information list for Peripherals.

# B.3 Alpha Products

Alpha Processor, Inc. maintains information about other Alpha products on their web site. Point your browser to www.alpha-processor.com and check the Product Information list for Alpha products.

# B.4 Documentation

## B.4.1 Alpha Documentation

| Title | Vendor |
|---|---|
| ***Alpha Architecture Reference Manual*** | **Digital Press order# EQ-W938E-DP.** |
| *Alpha Architecture Handbook* | Compaq Computer Corporation order# EC-QD2KC-TE, October, 1998. |
| ***Alpha 21264 Microprocessor Hardware Specification*** | **Digital Press** |
| *UP1000 Quick Start Installation Guide (51-0030-0A)* | Alpha Processor, Inc. |
| ***UP1000 User Guide (51-0031-0A)*** | **Alpha Processor, Inc.** |

## B.4.2 Related Documentation

You can order the following associated documentation directly from the vendor.

| Title | Vendor |
|---|---|
| ***Accelerated Graphics Port Interface Specification Revision 2.0*** | **Intel Corporation 2200 Mission College Blvd. Santa Clara, CA 95052-8119 May, 1998** |
| *AlphaPC 264DP Technical Reference Manual* | Compaq Computer Corporation order# EC-RBODA-TE. |
| ***AMD-751$^{TM}$ System Controller Data Sheet*, Revision D** | **AMD Publication # 21910, August, 1999** |
| *Computer Architecture* | John L. Hennessy and David A. Patterson, Morgan Kaufman Publishers, San Mateo, CA, 1990. |
| **ISA & EISA Theory and Operations** | **Edward Solari, Annabooks Bookstore (http://www.annabooks.com/index.htm), ISBN 0-929392-15-9** |

| Title | Vendor |
|---|---|
| *M1543C: PCI-to-ISA Bus Bridge with Super I/O & Fast IR Data Sheet*, Ver. 1.20 | ALI Document Number 1543DSC2.doc |
| ***Max 7000 Programmable Logic Device Family Data Sheet*, Version 5.03** | **Altera Corporation, 101 Innovation Drive San Jose, CA 95134 Document #A-DS-M7000-05.03 July, 1998** |
| • *PCI Local Bus Specification, Revision 2.1*<br>• *PCI Multimedia Design Guide, Revision 1.0*<br>• *PCI System Design Guide*<br>• *PCI-to-PCI Bridge Architecture Specification, Revision 0*<br>• *PCI BIOS Specification, Revision 2.1* | PCI Special Interest Group<br>U.S. 1-800-433-5177<br>International1-503-797-4207<br>FAX 1-503-234-6762 |
| • ***PC SDRAM Specification, Revision 1.63* (October, 1998)**<br>• ***PC SDRAM Unbuffered DIMM Specification, Revision 1.0* (February, 1998)**<br>• ***PC SDRAM Serial Presence Detect (SPD) Specification, Revision 1.2A* (December, 1997)** | **Intel Corporation** |
| *The Indispensable PC Hardware Book 3E* | Hans-Peter Messamer, Addison-Wesley Pub. Co., ISBN 0-201-87697-3 |
| ***Universal Serial Bus Specification, Revision 1.1*** | **USB Implementers Forum http://www.usb.org/ developers/docs.html September, 1998** |

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